WP 3.5: A 200MHz 15mW BiCMOS Sample-and-Hold Amplifier with 3V Supply

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This sample-and-hold amplifier for the front end of high-speed low-power A/D converters with 10b resolution has 1.5V swing in a 3.3V system with negligible sacrifice in speed, linearity, or power dissipation. Fabricated in a 1μm 20GHz BiCMOS process, the circuit operates at twice the speed of previous 3V SHAs [1].

The SHA architecture in Figure 1 consists of identical BiCMOS switches S_1-S_3, equal capacitors C_{H1} and C_{H2}, amplifier A_1, and a switch driver circuit that interfaces the input clock with S_1 and S_2. Switch S_3 is always off. Its role will be explained later. Amplifier outputs X and Y differ by V_{BE}≈0.8V, but are otherwise identical.

In sampling mode, S_1 and S_2 are on, the voltage across C_{H1} tracks V_{in}, and A_1 is configured as a unity-gain amplifier. In transition to the hold mode, S_1 and S_2 turn off and C_{H2} maintains a unity-gain loop around A_1. In this topology, both charge injection of S_1 and S_2 and hold-mode droop appear as a common-mode voltage at the inputs of A_1, allowing smaller values for C_{H1} and C_{H2} than in a single-ended case.

Note that with a 3V supply, S_1-S_3 in Figure 1 cannot be easily implemented using only MOS devices. This is because the bias voltage at *E* and *F* is typically around half of the supply voltage, leaving a small gate-source overdrive for MOS switches connected to these nodes and hence slowing acquisition. This problem is especially acute if low-threshold MOSFETs are not available.

The sampling switches used here use bipolar devices in the signal path. A critical issue in such a design is hold-mode feedthrough because the junction capacitance of bipolar transistors can conduct appreciably even when these devices are off. This translates into a direct trade-off between size of the sampling capacitor(s) and magnitude of the feedthrough signal, limiting the speed. In the architecture of Figure 1, this limitation is overcome by allowing S_1 and S_3 to conduct equal feedthrough signals to both inputs of the amplifier during hold mode. This remains effective as long as the output impedance at node X is sufficiently small. Simulations indicate the net feedthrough is 60dB below the analog input for frequencies to 100MHz.

Implementation of S_1-S_3 is evolved from the conventional diode bridge, as illustrated in Figure 2. To increase the dynamic range, the upper diodes are removed and the emitter-coupled pair is replaced with a single-ended current switch (Figure 2(b)). This technique increases maximum allowable voltage swings by approximately 1.3V, but it necessitates turning off both I_1 and I_2 at the end of the acquisition mode.

Since it is difficult to guarantee simultaneous switching of I_1 and I_2, consider two cases. First, suppose I_1 turns off *before* I_2; then, while I_2 remains on, V_{out} tracks V_{in} if the input slew rate is negative, but does not if it is positive. This effect gives rise to input-dependent sampling instants and hence harmonic distortion. Now, suppose I_1 turns off *after* I_2; then the diodes immediately turn off but the held value of V_{out} experiences a small offset as I_1 continues to charge C_H. This effect is cancelled in the architecture of Figure 1 if S_1-S_2 and C_{H1}-C_{H2} are identical pairs. The latter case is chosen with proper timing in the design of the switch driver. An interesting point of contrast between the conventional bridge and the sampling switch of Figure 2(b) relates to their pedestal error. In the former circuit, transition from acquisition mode to hold mode introduces nonlinearity unless bootstrapping is employed, a remedy that may increase the hold-mode settling time [2, 3, 4]. In the latter circuit, on the other hand, there is no such effect and charge injection due to I_1 and I_2 - relatively independent of the analog input - is cancelled by the architecture of Figure 1.

In Figure 2(b), diode D_2 can be replaced with an emitter follower to reduce transient currents drawn from the input and switched current source I_1 can be realized as shown in Figure 2(c). However, the small transconductance of M_2 and the large capacitance at node X yield a time constant greater than 1ns, considerably slowing switching. This is resolved in Figure 2(d), where turn-off is aided by emitter follower Q_2 and turn-on is enhanced by an additional impulse of current pulled from M_2 on the proper clock edge. The switched-current source I_2 is accompanied with such an impulse to match the initial surge in the drain current of M_1. Note that Q_2, M_2, and associated current sources can be shared among several sampling switches.

The switch driver and its interface with the BiCMOS sampling switch S_1 are shown in Figure 3. The driver consists of: an input differential pair providing complementary clocks for Q_2 and Q_6; a slow/fast network R_3,R_4, C_1, C_2, Q_7, and Q_8; and Q_3 and Q_9 operating as switched current sources. Capacitors C_1 and C_2 couple the logic transitions at the emitter of Q_6 to bases of Q_8 and Q_9, respectively, producing impulses 0.3ns wide in I_{C3} and I_{C9}. Final current levels are set primarily by collector current of Q_8 and sizing of Q_3 and Q_9.

Amplifier A_1 in Figure 1 must efficiently drive the input capacitance of the following A/D converter. While it is desirable to employ MOS devices at the input of A_1 for low droop rate, the low open-loop gain and high closed-loop output impedance of such implementation severely limit the output settling speed and increase the hold-mode feedthrough. Figure 4 illustrates the evolution of the amplifier topology. Figure4(a) is a BiCMOS unity-gain stage with level shifting diode D_1 to allow larger voltage swings. The circuit comprising Q_3, D_1, I_{A1}, and I_{A2} happens to be the same as the sampling switch of Figure 2(c) and can operate as such. To maintain feedback after this switch turns off, another emitter follower Q_4 and a capacitor C_{H2} are added as shown in Figure 4(b). The measured output at 200MHz sampling rate with a 50MHz input sinewave is shown in Figure 5. The droop rate is approximately 40mV/μs and the hold-mode feedthrough is about -52dB, including ground feedthrough in the setup. The pedestal error is 8mV.

The sampled waveform has been examined for harmonic distortion. Figure 6 shows the spectrum with 200MHz sampling rate and10MHz analog input, indicating distortion <-65 dB. This includes the output slewing during the acquisition mode, a substantial source of nonlinearity. It is expected that if only the held values are considered, much lower distortion will be observed.

References

[1] Razavi, B. "A 100-MHz 10-mW All-NPN Sample-and-Hold Circuit with 3V Supply, "Proc. European Solid-State Circuits Conf., pp. 192-195, Sept., 1994.

[2] Poulton, K., et al., "A 1-GHz 6-Bit ADC System," IEEE J. Solid-State Circuits, vol. SC-22, pp. 962-970, Dec., 1987.

[3] Razavi, B., *Principles of Data Conversion System Design*, Ch. 2, IEEE Press, New York, 1995.

[4] Colleran, W. T., A. A. Abidi, "A 10-b 75-MHz Two-Step Pipelined Bipolar A/D Converter," IEEE J. Solid-State Circuits, vol. SC-28, pp. 1187-1199, Dec., 1993.

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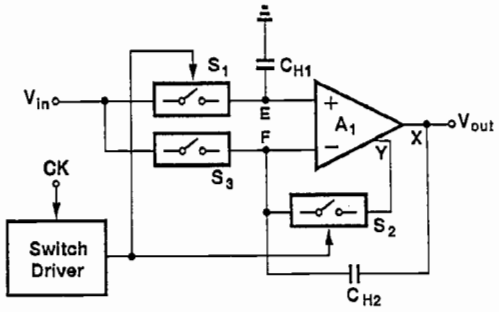

Figure 1: SHA architecture.

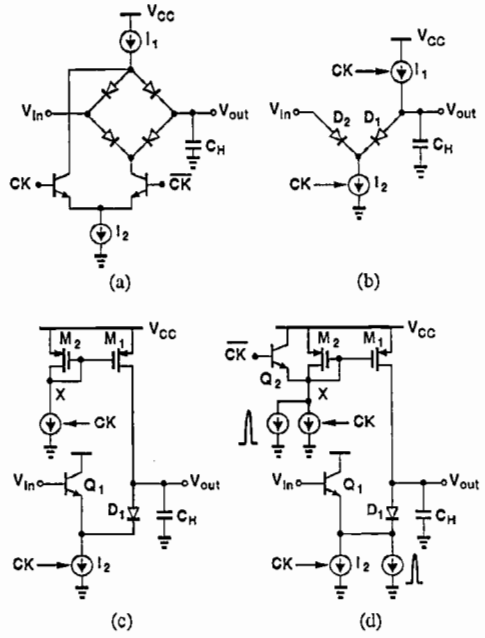

Figure 2: Evolution of BiCMOS sampling switch.

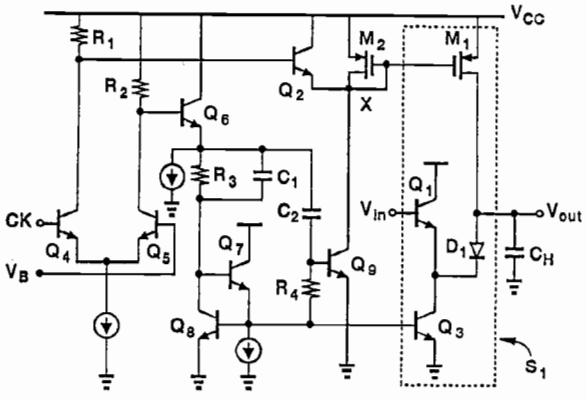

Figure 3: Switch driver.

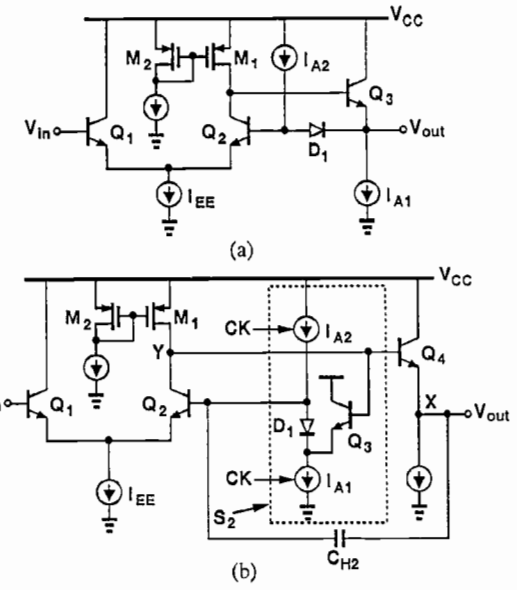

Figure 4: Evolution of output buffer.

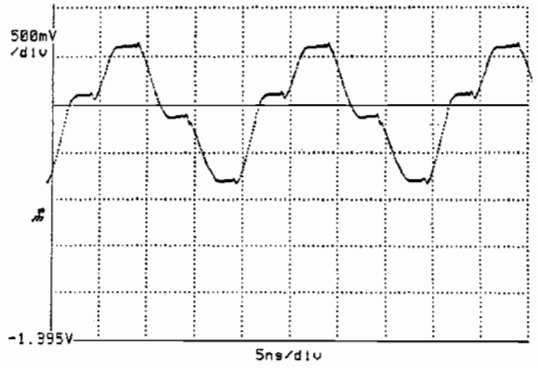

Figure 5: Sampled output at 200MHz with 50MHz input.

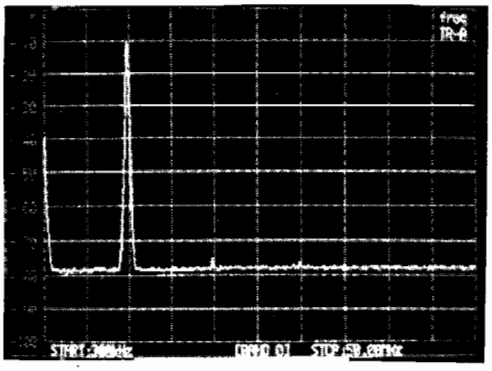

Figure 6: Output spectrum (horiz. 5MHz/div., vert. 10dB/div.).