A 2.5-Gb/sec 15-mW BiCMOS Clock Recovery Circuit

Behzad Razavi and James Sung
AT&T Bell Laboratories, Holmdel, NJ 07733, USA

High-speed low-power clock recovery circuits find wide application in high-performance communication systems [1]. This paper describes the design of a 2.5-Gb/sec 15-mW clock recovery circuit (CRC) fabricated in a 20-GHz 1-μm BiCMOS technology [2]. Employing a modified version of the "quadricorrelator" architecture [3, 4], the circuit extracts the clock from a non-return-to-zero (NRZ) data sequence using both phase and frequency detection.

Shown in Fig. 1, the original quadricorrelator architecture consists of a front-end operator (differentiator and full-wave rectifier) followed by a phase/frequency-locked loop including in-phase and quadrature mixers and a voltage-controlled oscillator (VCO) with quadrature outputs. The combination of Loop 1 and Loop 2 serves as a frequency-locked loop while Loop 3 functions as a phase-locked loop. The circuit operates as follows. The front-end operator creates a frequency component at $\omega_1 = 2.5$ GHz from an NRZ sequence at 2.5 Gb/sec. This component is mixed with the VCO outputs and low-pass filtered, yielding quadrature signals $\sin(\omega_1 - \omega_2)t$ and $\cos(\omega_1 - \omega_2)t$. One of these signals is differentiated and mixed with the other and the result is low-pass filtered, thereby producing a dc signal whose magnitude and polarity correspond to those of $\omega_1 - \omega_2$. This signal drives ω_2 closer to ω_1, and when $\omega_1 - \omega_2$ is sufficiently small, Loop 3 begins to dominate, thus acquiring the phase lock.

To obtain a compact, low-power implementation, the quadricorrelator architecture can be modified as shown in Fig. 2. Here, the front-end operator is moved to each arm such that it can be merged with the subsequent mixer and low-pass filter. The resulting circuit performs differentiation, rectification, mixing, and low-pass filtering, and is denoted as DRML. Similarly, the second differentiator, mixer, and low-pass filter can be combined (DML in Fig. 2). Note that the high-speed path now includes only three blocks, allowing significant savings in power dissipation. The architecture is fully differential to suppress common-mode noise and provide robust operation from a 3-V supply.

The DRML implementation is depicted in Fig. 3. A capacitively-degenerated differential pair, Q_3-Q_4, approximates the differentiator, and two Gilbert multipliers, Q_5-Q_8 and Q_9-Q_{12}, perform full-wave rectification and mixing, respectively. The circuit operates as follows. When D_{in} goes high, Q_4 turns off momentarily, disabling Q_7 and Q_8. At the same time, Q_6 and Q_{11}-Q_{12} are also off. Thus, the entire tail current $I_{BE1} + I_{BE2}$ flows from Q_3, Q_5, and Q_9-Q_{10}, and is therefore multiplied by the VCO output. Due to symmetry, the same result is obtained when D_{in} goes low. Consequently, on every data transition the instantaneous value of the VCO output is sampled and deposited as charge on C_1.

The interface between the VCO and the DRML circuit entails an important issue: the feedthrough of data transitions from the input of DRML to the output of the VCO. Illustrated in Fig. 4, this effect originates from the capacitive path between these two ports and disturbs the VCO whenever D_{in} changes. While differential operation reduces the feedthrough, capacitance nonlinearities still require that the VCO internal circuit be isolated from this disturbance.

The VCO is realized as a two-stage ring oscillator so as to provide quadrature outputs (Fig. 5). We note that each stage in the ring must drive three circuits: the other stage, a mixer, and an output buffer. (Both stages are loaded with buffers to maintain symmetry.) In the VCO of Fig. 5, these outputs are taken from different ports to distribute the loading as well as ensure isolation of the VCO from the feedthrough noise.

Since a simple two-stage ECL ring oscillator suffers from both small-amplitude oscillations due to insufficient phase shift and narrow tuning range due to limited gain, the VCO of Fig. 5 incorporates additional phase/gain elements. Shown in Fig. 6 is the implementation of each stage, consisting of emitter followers Q_1-Q_2, a cross-coupled pair Q_3-Q_4, and two differential pairs Q_5-Q_6 and Q_7-Q_8. At high frequencies, the total capacitance seen at nodes X and Y allows the cross-coupled pair to contribute substantial gain (even at low bias currents) and phase shift. As a result, the VCO center frequency can be varied by approximately 1 GHz with little degradation in the voltage swings.

The signal driving each mixer is taken from the *collectors* of Q_1 and Q_2 and buffered by the pair Q_7-Q_8. At 2.5 GHz, the voltage gain from V_{in} to nodes M and N is approximately equal to the total capacitance seen at X and Y divided by that at M and N - roughly unity. This technique effectively isolates the internal VCO signal path from the DRML feedthrough noise.

All the current sources in the CRC are implemented with NMOS devices. For the current levels used here, NMOSFETs introduce less capacitance and less thermal noise and consume less voltage headroom than their bipolar counterparts.

The fabricated prototype has been tested on wafer with a 3-V supply. The circuit (excluding the I/O buffers) dissipates 15 mW. Fig. 7 shows the measured input and output waveforms of the CRC for a 2.5-Gb/sec pseudorandom NRZ sequence of length $2^{20} - 1$. The rms jitter is 9.5 psec and the capture range is 300 MHz. Fig. 8 depicts the output spectrum. The circuit exhibits a phase noise of -80 dBc/Hz at 50 kHz offset.

References

[1] M. Soyuer, "A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology," *IEEE Journal of Solid-State Circuits*, vol. SC-28, pp. 1310-1313, Dec. 1993.

[2] J. Sung *et al*, "BEST2 - A High Performance Super Self-Aligned 3V/5V BiCMOS Technology with Extremely Low Parasitics for Low-Power Mixed-Signal Applications," *Proc. IEEE CICC*, pp. 15-18, May 1994.

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[4] J. A. Bellisio, "A New Phase-Locked Loop Timing Recovery Method for Digital Regenerators," *IEEE Int. Conference Rec.*, vol.1, June 1976, pp. 10-17.

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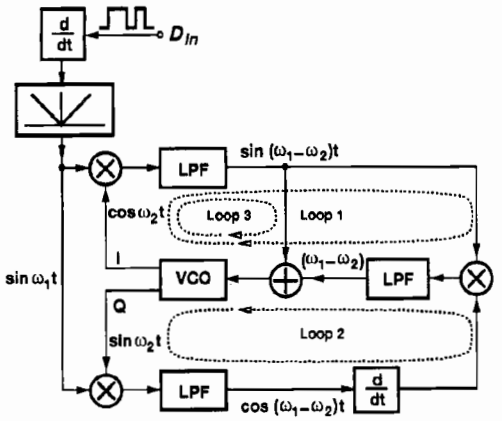

Fig. 1. Operation of quadricorrelator.

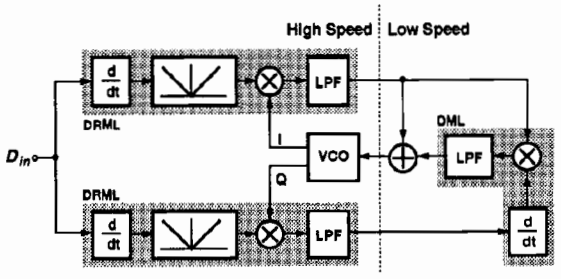

Fig. 2. Clock recovery architecture.

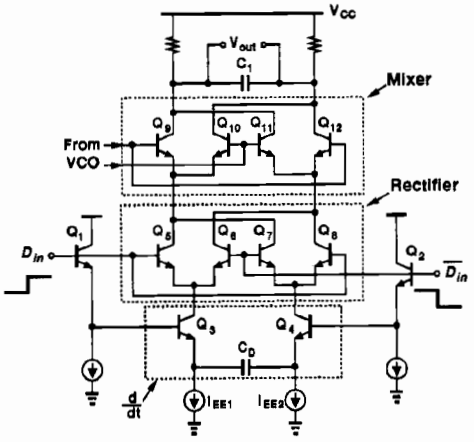

Fig. 3. Differentiator, rectifier, mixer, and LPF.

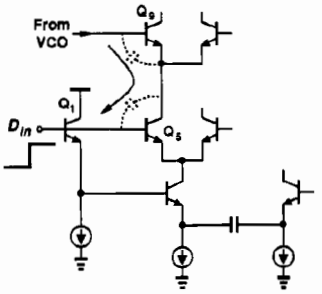

Fig. 4. Feedthrough from D_{in} to VCO.

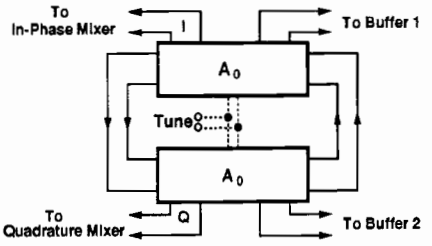

Fig. 5. VCO block diagram.

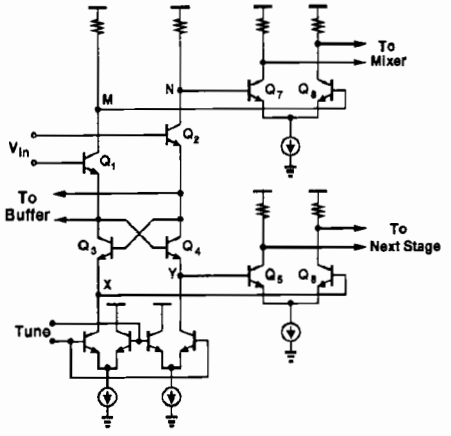

Fig. 6. Implementation of one stage of VCO.

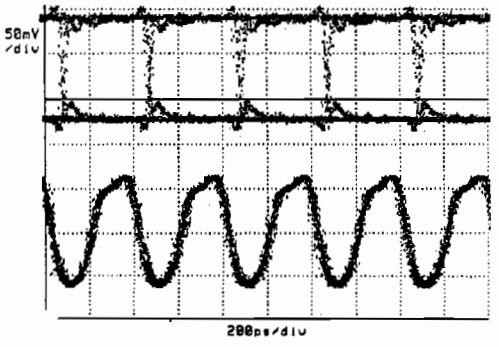

Fig. 7. Measured input/output waveforms.

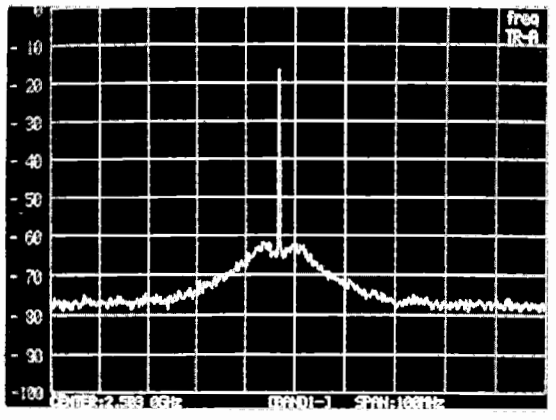

Fig. 8. Output spectrum (Horiz. 10 MHz/div., Vert. 10 dB/div.)