A 12-Bit 10-MHz BiCMOS Comparator *

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Abstract

The design of a self-calibrating BiCMOS comparator is presented. The circuit employs a preamplifier followed by two regenerative stages to achieve an input offset of 200 μV at a conversion rate of 10 MHz. The comparator has an input range of 3 V and dissipates 1.7 mW from a 5-volt supply.

Introduction

In high-speed analog-to-digital converters (ADCs), comparator design plays a crucial role in the overall system performance that can be achieved. ADC architectures that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraints on their delay, resolution, power dissipation, input voltage range, and input impedance. In low-voltage, scaled technologies, limited input range and large device mismatch necessitate some means of comparator offset cancellation if a wide dynamic range is required.

In CMOS technology, comparator offset can be reduced using the topology shown in Figure 1(a). In this approach, a preamplifier is utilized to overcome the offset of the subsequent latch, which can exceed 50 mV. The preamplifier must provide enough gain to attain a low input-referred offset, facing severe trade-offs in speed, power, and input capacitance.

This paper describes a self-calibrating comparator with the architecture shown in Figure 1(b) that exploits the attributes of BiCMOS technology to achieve an input offset of less than 200 μV at comparison rates above 10 MHz while dissipating 1.7 mW from a 5-V supply. This is accomplished through the use of a low-offset bipolar latch interposed between a preamplifier and a CMOS output latch. The comparator was designed for use in 12-bit half-flash ADC systems and performs offset cancellation during overdrive recovery in every cycle, thereby eliminating flicker noise.

Circuit Description

The comparator in Figure 1(b) comprises a preamplifier, offset storage capacitors, a bipolar latch, and a CMOS latch. Controlled by two nonoverlapping clocks $\Phi 1$ and $\Phi 2$, the circuit operates as follows. In the calibration mode, S1 and S2 are off, and S3-S6 are on, grounding the inputs of the preamplifier and the bipolar latch. The preamplifier input offset is thus amplified and stored on C1 and C2. In this mode, the two latches are also reset. In the comparison mode, first S3-S5 turn off while S1 and S2 turn on; the input voltage V_i is thereby sensed and amplified, generating a differential voltage at the bipolar latch input. Next, the two latches are strobed sequentially to produce CMOS levels at the output. The residual input offset of this configuration is determined by the bipolar latch offset divided by the preamplifier gain and can be maintained below 200 μV. In order to generate 5-V CMOS levels at the output from a 200-μV input, the comparator must provide an equivalent gain of 25,000, a constraint that demands careful gain allocation among the three stages.

The preamplifier circuit is shown in Figure 2. It comprises source followers M1 and M2, the differential pair Q1 and Q2, and emitter followers Q3 and Q4. The preamplifier provides a gain of 20 that is stabilized against temperature variations by using bias currents proportional to absolute temperature. By virtue of the large transconductance of bipolar transistors, the differential amplifier can attain this gain while achieving a bandwidth of more than 100 MHz with a power dissipation of only 0.5 mW. The emitter followers buffer the outputs and, together with D1 and D2, shift the output voltage down to establish sufficient bias across C1 and C2, which are simply large NMOS transistors in this implementation.

A combined circuit diagram of the bipolar and CMOS latches is shown in Figure 3. The bipolar latch consists of cross-coupled devices Q5 and Q6, and a charge-pumping circuit, M11, M12, and C3. The coupling capacitors C1 and C2 act as both offset-storage elements and load devices for the bipolar latch. During calibration, $\Phi 1$ is low, grounding the nodes X1 and Y1, and $\Phi 2$ is high, discharging C3 to V_{EE}. During comparison, $\Phi 1$ goes high and, after the preamplifier has sensed the input and a differential voltage is developed at X1 and Y1, $\Phi 2$ goes low, turning M5 on and transferring charge through the bipolar pair. In a fashion similar to that described in [1], the voltage difference between nodes X1 and Y1 is regeneratively amplified until C3 charges up and the tail current falls to zero. This operation, which can be viewed as charge-sharing between C3 and the combination of C1 and C2, exhibits a high speed because of the positive feedback around Q5 and Q6 and the large transconductance of these devices. The latch produces a differential voltage of several hundred millivolts in less than 5 nsec.

Since the bipolar latch steers charge, rather than current, it has two advantages over conventional current-steering bipolar latches: 1) it draws no input current during calibration and can therefore be directly coupled to C1 and C2 without input bias

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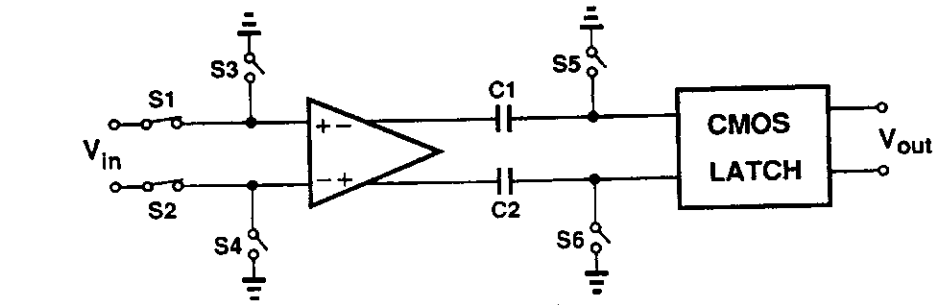
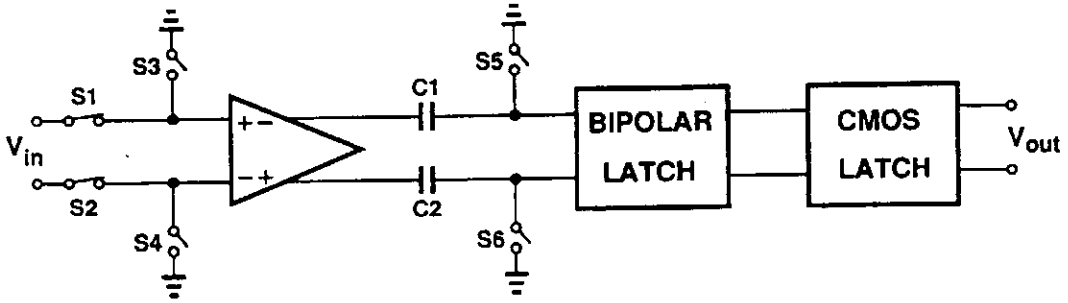


(a)



(b)

Figure 1. (a) Conventional CMOS comparator block diagram, (b) BiCMOS comparator block diagram.

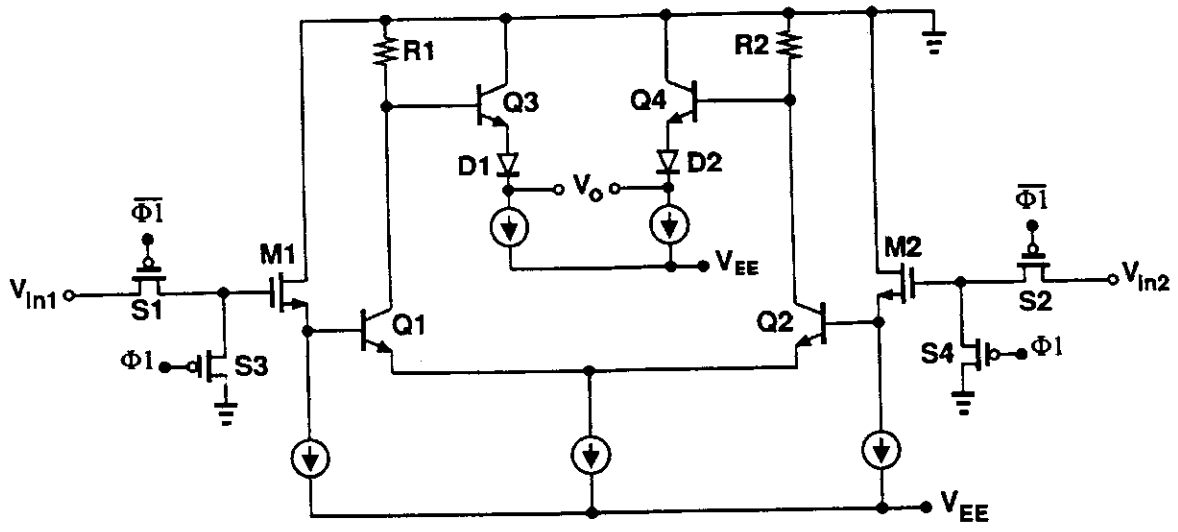


Figure 2. BiCMOS preamplifier.

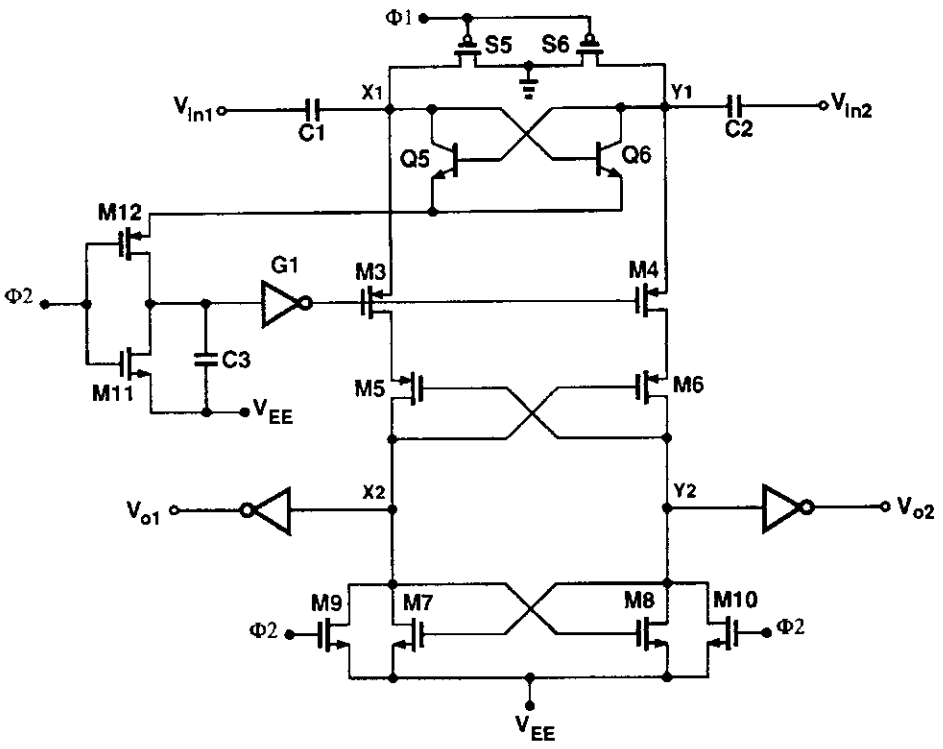
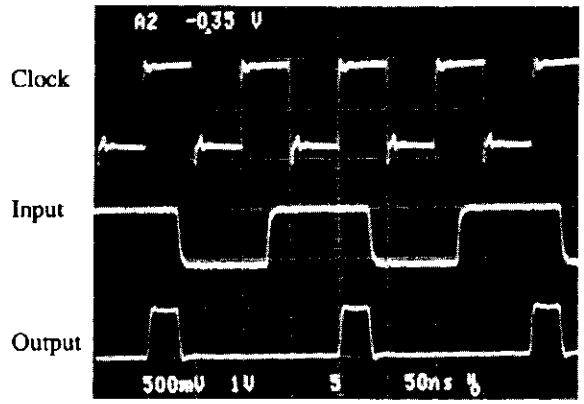
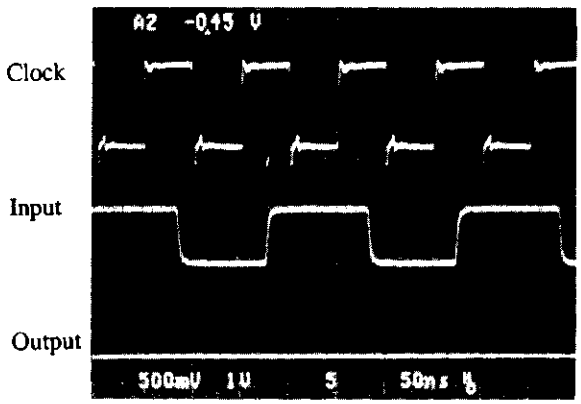


Figure 3. Combined circuit of bipolar and CMOS latches.



(a)



(b)

Figure 5. Overdrive recovery test for (a) $V_{in1} - V_{in2} = +300\ \mu V$, and (b) $V_{in1} - V_{in2} = -300\ \mu V$.

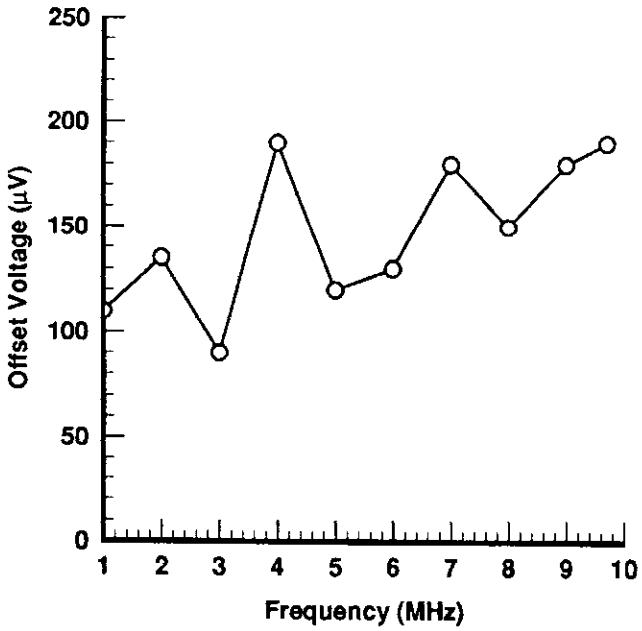


Figure 4. Comparator input offset voltage as a function of clock frequency.

current cancellation, and 2) it has zero static power dissipation. Also, in this application the preamplifier need only reduce the input offset resulting from the V_{BE} mismatch of the two bipolar transistors Q5 and Q6, rather than the larger V_{GS} mismatch of two MOS devices which would be necessary if a CMOS latch were used. Unlike current-steering configurations, this latch has a finite gain because of the limited charge available for its regeneration. Nonetheless, for typical values of C1, C2, and C3, the equivalent gain exceeds several thousand.

The last stage of the comparator is a CMOS latch that is used to generate CMOS levels from the output of the bipolar latch. It consists of sense transistors M3 and M4, cross-coupled devices M5-M8, reset elements M9 and M10, and a clock delay inverter G1. The operation of this latch is based on charge-sharing between C1 and the capacitance at the node X2, and between C2 and the capacitance at the node Y2. However, C1 and C2 (approximately 0.55 pF each) experience negligible discharge because they are much larger than the parasitics at X2 and Y2. As a result, the X2 and Y2 voltages can closely approach the supply rails.

The CMOS latch operates as follows. In the calibration mode, when $\Phi 2$ is high, M3 and M4 are off, and M9 and M10 discharge X2 and Y2 to V_{EE}. In the comparison mode, $\Phi 2$ goes low to strobe the bipolar latch and turn off M9 and M10. Then, following a delay controlled by C3, transistors M3 and M4 turn on, coupling the voltage difference between X1 and Y1 to the sources of M5 and M6 and initiating regeneration at nodes X2 and Y2. The regeneration continues until X2 or Y2 reach the voltage at X1 or Y1, while the other has returned to V_{EE}. Designed with short-channel devices for fast response, this latch can exhibit input offsets as high as 50 mV and thus must be strobed only after the bipolar latch has generated a sufficient differential voltage at X1 and Y1. This is accomplished by setting the switching point of G1 above -3 V, so that its output does not go low until C3 has charged up by at least 2 volts. Because C3 is approximately one-fifth of C1 and C2, a 2-volt change in its voltage corresponds to at least 200 mV of potential difference between X1 and Y1.

In order to prevent degradation of the X1 and Y1 common-mode voltage, M3 and M4, which remain on as long as $\Phi 2$ is low, are followed by cross-coupled devices M5 and M6. For example, when X2 is low and Y2 is high, M5 turns off, isolating X1 from M7, which would otherwise discharge X1 to one PMOS threshold voltage above V_{EE}.

Experimental Results

The comparator has been fabricated in the Stanford 2-μm BiCMOS process in an area of 100 μm $\times$ 250 μm. The performance of this experimental prototype was evaluated for both dc and time-varying inputs. Figure 4 plots the input offset voltage measured for dc inputs as a function of clock frequency. The offset remains below 200 μV up to 10 MHz. The sharp variations in offset are attributed to ringing and clock coupling in the package and the test setup.

In order to demonstrate the effectiveness of the offset cancellation, as well as the overdrive recovery at 10 MHz, the comparator response was examined in two different tests. In the first test, one input is stepped from -1 V to 0 V in consecutive clock cycles, while the other input is held at -300 μV. In the second test, one input is stepped from -1 V to -300 μV while the other input is held at 0 V. The oscillographs in Figures 5(a) and (b) show that the comparator indeed accomplishes full offset cancellation and overdrive recovery, yielding an output of one when $V_{in1} - V_{in2}' = +300$ μV, and zero when $V_{in1} - V_{in2} = -300$ μV. Table I summarizes the comparator performance.

Conclusion

The availability of bipolar and CMOS devices on the same substrate can be exploited to design high performance, compact analog circuits. In particular, the high speed and low offset of bipolar transistors together with zero-offset switching and rail-to-rail swing capabilities of CMOS devices allow the implementation of fast amplifiers, sensitive latches, and low-power level translators. Employing these attributes, a 10-MHz BiCMOS comparator with more than 12 bits of dynamic range and a power dissipation of 1.7 mW has been designed.

Acknowledgement

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Reference

[1] P. J. Lim, B. A. Wooley, "An 8-bit 200-MHz BiCMOS comparator," *IEEE J. Solid-State Circuits*, vol. SC-23, pp. 192-199; Feb. 1990.

Input Offset	**200 μV**
Comparison Rate	**10 MHz**
Input Range	**3 V**
Power	**1.7 mW**
Power Supply	**5 V**
Input Capacitance	**40 fF**
Area	**100 x 250 μm^2**

Table I. BiCMOS comparator performance.