Design of Sample-and-Hold Amplifiers for High-Speed Low-Voltage A/D Converters

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Abstract

Multi-step analog-to-digital converters typically employ a sample-and-hold amplifier at the front end that must achieve high speed and high linearity with low power dissipation. Furthermore, sampling circuits can be used to alleviate the timing and bandwidth limitations of one-step converters such as flash and interpolative architectures.

This paper describes design techniques for sample-and-hold circuits utilized in high-speed low-voltage data converters. Following a review of the role of sampling in various converter architectures, two broad categories of sampling techniques are introduced and properties of basic analog switches are summarized. Next, conventional sampling architectures are discussed, design methods for CMOS, bipolar, and BiCMOS implementations are studied, and several examples embodying these methods are presented. Finally, characterization of high-speed sampling circuits is described.

I. Introduction

Sample-and-hold amplifiers (SHAs) play a crucial role in the design of data acquisition interfaces, particularly analog-to-digital converters (ADCs). Front-end SHAs are fundamentally difficult to design because they must operate at the extreme corner of the performance envelope, achieving simultaneously high linearity, high speed, large voltage swings, high drive capability, and low power dissipation. In low-voltage systems, analog sampling becomes more challenging because the limited headroom further tightens the trade-offs among the performance parameters.

This paper describes design techniques for high-speed low-voltage sample-and-hold circuits suited fro use at the front end of monolithic ADCs. In Section II, we consider the role of SHAs in one-step, multi-step, and interleaved A/D converters and review aspects of the SHA performance that are critical in each environment. In Section III, we describe basic sampling techniques and in Section IV, conventional SHA architectures. Examples of the state of the art are presented in Section V, and the problem of SHA characterization is addressed in Section VI.

II. SHAs in ADCs

The use of front-end sampling circuits is greatly beneficial in some ADCs and indispensable in some others. We consider three common applications here.

A. One-Step and Multi-Step ADCs

One-step A/D converters such as flash, folding, and interpolative architectures employ "distributed' sampling in the bank of comparators, in principle obviating the need for an explicit front-end SHA. However, various timing imperfections in these topologies degrade the effective number of bits (ENOB) at high analog input frequencies, typically by three to five under Nyquist-rate operation.

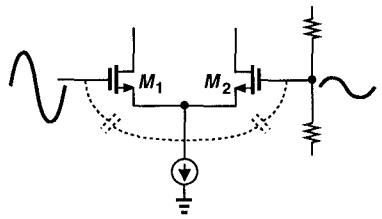

Fig. 1. Feedthrough of input to ladder in a flash ADC.

Several mechanisms account for this degradation [1]. First, as shown in Fig. 1, capacitive feedthrough from the analog input to the resistor ladder disturbs the reference tap voltages, in essence introducing an input-dependent offset in each comparator. Second, as depicted in Fig. 2, the *nonlinear* input capacitance arising from a large number of comparators together

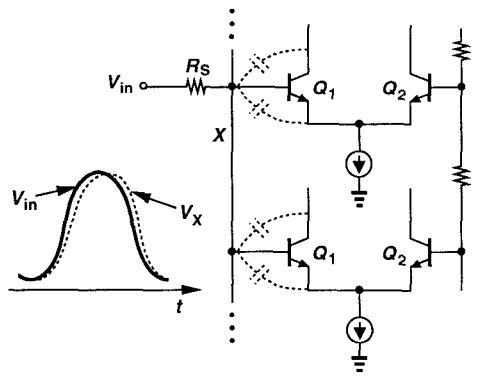

Fig. 2. Nonlinear input capacitance in a flash ADC.

with the source impedance results in an input-dependent phase shift and hence harmonic distortion. Third, as illustrated in Fig. 3, mismatches between the sampling instants of adjacent comparators at high frequencies yield bubbles (sparkles) in the thermometer code. Fourth, since the analog signal and the sampling clock in an ADC chip must travel long distances

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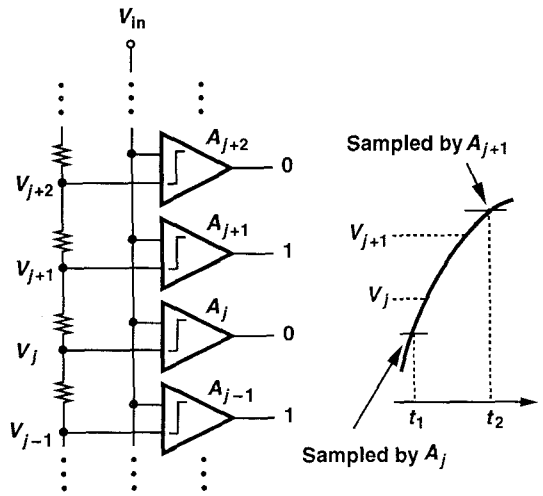


Fig. 3. Sparkles resulting from timing mismatch.

and feed a large number of devices, they experience different delays due to different loading, i.e., the exact time difference between the analog input and the clock edge varies across the chip.

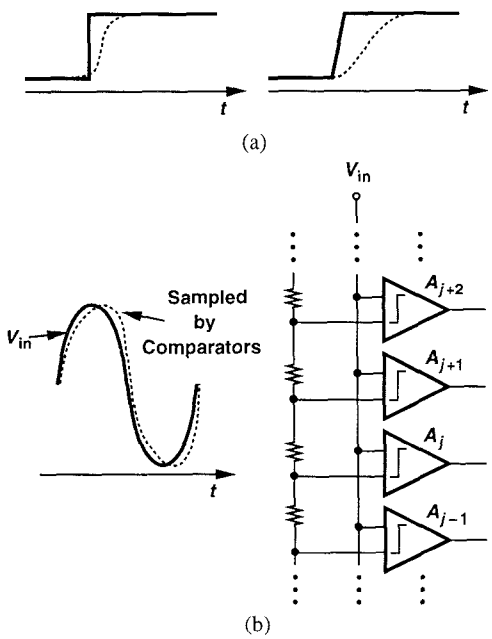


Fig. 4. (a) Slew-dependent delay in a nonlinear stage, (b) effect in a flash ADC.

Another important distortion mechanism that merits particular attention arises in nonlinear stages with limited bandwidth [2]. Shown in Fig. 4, the signal delay in a nonlinear amplifier (e.g., the input stage of a comparator) depends on the input slew rate if the circuit has a finite bandwidth [2]. When digitizing a full-scale high-frequency signal, a bank of comparators samples the points near the peaks with greater delay than the points near the midrange, thus distorting the sampled waveform. It has been shown [2] that for bipolar differential pairs and a full scale of 1 V, if the amplifier bandwidth is ten times the input signal frequency, then a third-order distortion of approximately −55 dB results.

All of the above effects can be suppressed through the use of a front-end SHA. In today's technology, even a delay of a few hundred picoseconds interposed between the end of acquisition and the beginning of quantization can significantly lower these timing errors.

In one-step converters, the following parameters of the SHA are critical: acquisition and hold settling times, linearity, jitter, hold-mode feedthrough, and common-mode compatibility with the ADC. On the other hand, parameters such as gain error, droop rate, offset, and pedestal are less important.

In multi-step ADCs, the front-end SHA is an integral part of the system because the input signal must be held until a number of operations (e.g., coarse quantization, D/A conversion, and subtraction) are completed. In these systems, the kickback noise immunity of the front-end SHA is also of concern. If the first conversion step generates substantial kickback noise, the SHA must recover from such disturbance by the time its output is sampled for the next conversion step.

B. Interleaved ADCs

Interleaved architectures incorporate a number of subconverters so as to achieve a higher speed than is possible in one-step configurations (Fig. 5). The key to this approach is that the acquisition of the signal by each SHA must be faster

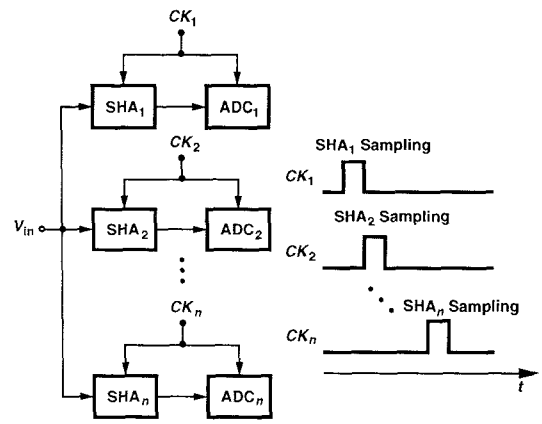


Fig. 5. Interleaved ADC.

than the A/D conversion by the each subconverter.

In addition to the parameters mentioned above, the *matching* between SHAs is also critical in an interleaved system. Mismatches in the gain, offset, and aperture delay translate to a higher noise floor [3, 4].

III. Sampling Techniques

Sampling techniques can be broadly classified as depicted in Fig. 6. In the circuit of Fig. 6(a) (called Method I here), the sampling capacitor is *in parallel* with the signal, and the input and the output are dc-coupled. In the circuit of Fig. 6(b) (called Method II here), the sampling capacitor is *in series* with the signal, thereby isolating the common-mode (CM) levels of the input and the output. In Fig. 6(b), during the acquisition mode, S_2 and S_3 are on and in the transition to the hold mode,

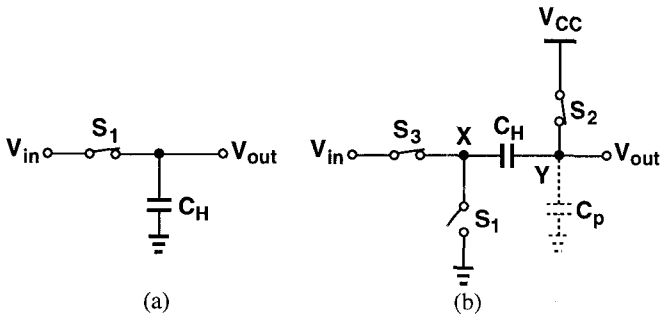


Fig. 6. (a) Parallel sampling, (b) series sampling.

first node Y is released from V_{CC} and subsequently node X is shorted to ground, producing a voltage change at the output equal to the instantaneous value of the input.

In addition to isolated input and output CM levels, Method II offers another advantage over Method I. While parallel sampling suffers from input-dependent charge injection of S_1, series sampling does not exhibit such behavior because S_2 turns off before S_3, thus injecting a *constant* charge onto node Y, an error that can be eliminated through differential operation.

Another point of contrast between the two sampling techniques lies in their hold-mode feedthrough behavior. In Method I, C_H forms an attenuator with the feedthrough capacitance of the sampling switch, whereas in Method II, C_H has little effect on the feedthrough signal. This point is especially critical in bipolar sampling circuits because the junction capacitances of bipolar devices conduct appreciably in the hold mode.

Method II has two other disadvantages with respect to Method I. The nonlinearity of the parasitic capacitance C_P at node Y introduces distortion in the sampled value, mandating that C_H be sufficiently greater than C_P. Moreover, the hold settling time in series sampling is quite longer than in parallel sampling because in the former the output voltage must always begin from a reset value whereas in the latter, V_{out} begins from a level close to its final value.

The foregoing sampling techniques can be implemented with various types of switches. While MOS transistors require low complexity and simple drive circuitry, they exhibit two sources of dynamic errors in addition to channel charge injection and clock feedthrough. First, as shown in Fig. 7, the variation of the switch on-resistance with the input level introduces distortion. Second, as depicted in Fig. 8, the finite transition time of the sampling clock results in an input-dependent sampling instant [1].

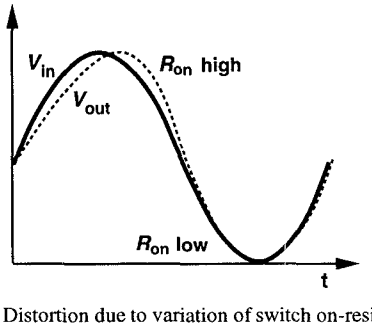


Fig. 7. Distortion due to variation of switch on-resistance.

Another issue in low-voltage applications is the high on-resistance of MOS devices, especially if the source/drain common-mode level is about mid-supply voltage. In fact, high locally-generated supplies may be required to guarantee a sufficiently low on-resistance despite threshold voltage variations [5].

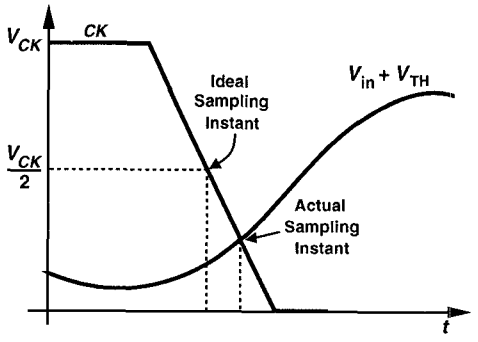


Fig. 8. Input-dependent sampling point due to finite clock transition time.

In bipolar technology, the sampling bridge of Fig. 9 is often used. Achieving a high speed, the circuit nevertheless provides little dynamic range with a 3-V supply. Alternatively, the bridge can be modified as illustrated in Fig. 10, where the upper two diodes are removed, the input diode is replaced with an emitter follower, and the bottom current source is converted to single-ended form, saving a total of approximately 1.3 V in the voltage headroom [6]. In this circuit, however, both current sources must turn off simultaneously, an issue to be discussed in Section V.E.

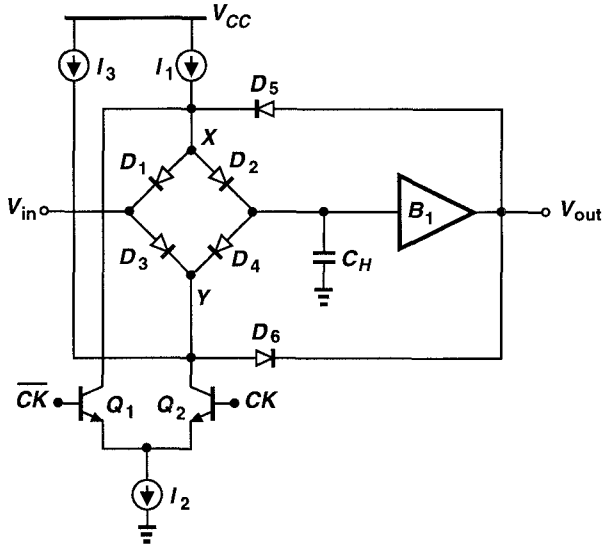
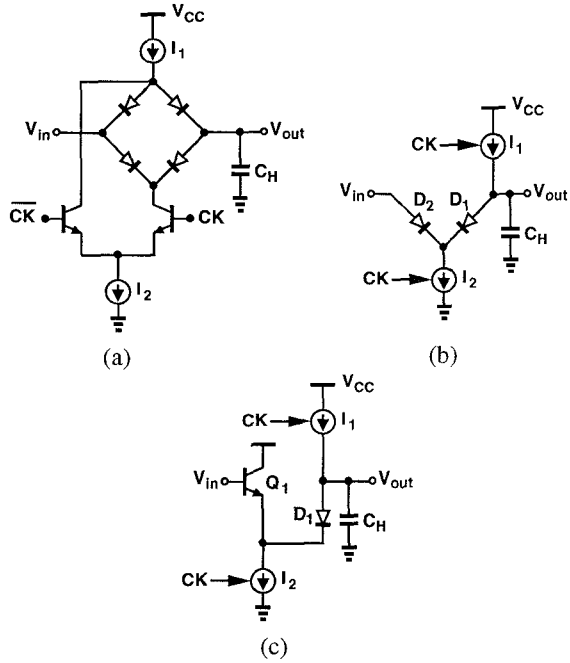


Fig. 9. Bipolar sampling bridge.

Another type of bipolar sampling switch is the emitter follower [7]. Shown in Fig. 11 in simplified form, such a circuit provides an efficient drive for the sampling capacitor, but it requires greater complexity to ensure Q_1 remains off in the hold mode (Section V.C).

IV. Conventional SHA Architectures

The trade-offs studied above can be alleviated through innovations at both architecture and circuit level. In this section,



(a) (b) (c)

Fig. 10. (a) Simplified diode bridge, (b) bridge with two top diodes removed and bottom current source converted to single-ended form, (c) bridge with input follower to lower kickback noise.

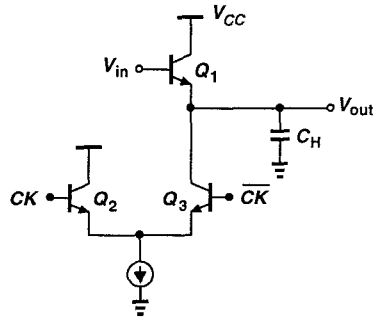


Fig. 11. Switched emitter follower.

we describe a number of conventional SHAs so as to illustrate their design challenges.

In order to suppress input-dependent pedestal errors in a SHA, the sampling switch can be embedded in a feedback loop such that it always turns off with a constant gate-source voltage. Shown in Fig. 12, the conventional closed-loop

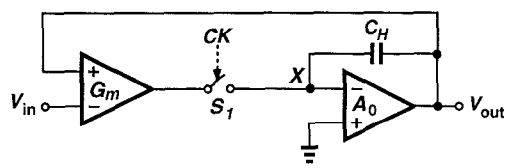
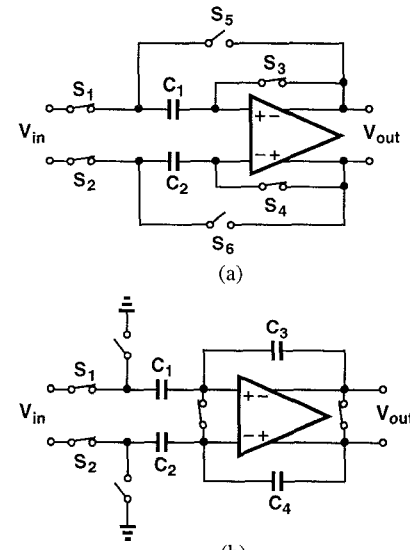


Fig. 12. Closed-loop SHA architecture.

architecture incorporates this concept in a two-stage op amp topology. Since node X is a virtual ground, the charge injected by S_1 is relatively constant. However, stability and settling considerations that plague typical two-stage op amps limit the speed of this architecture.

A SHA configuration especially popular in CMOS technology is shown in Fig. 13(a). Based on the series sampling technique of Fig. 6(b), this approach utilizes a virtual ground



(a) (b)

Fig. 13. (a) Unity-gain sampler, (b) alternative topology with independent input and output CM levels.

to perform a precise hold operation. Since at the end of the acquisition mode, S_3 and S_4 turn off before S_1 and S_2, the charge injected by the former two is constant and equal, disturbing only the output CM level. The challenge, however, lies in the design of the op amp. High-speed applications mandate the use of a telescopic cascode op amp for fast settling, but it is difficult to short the input and the output of such a topology. For this reason, the configuration in Fig. 13(b) proves useful because it allows independent choice of the input and output CM levels. Nevertheless, the trade-offs among speed, gain, and output voltage swing of op amps and the issues mentioned above in relation with MOS switches make this approach less attractive at low supply voltages.

Fig. 14 depicts a SHA architecture originally proposed by Ryan [8] and later modified by Petschacher et al. [9]. Employing transconductance stages G_{m1} and G_{m2} and transresistance

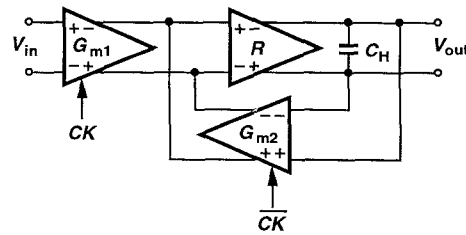


Fig. 14. SHA architecture with multiplexed input.

stage R (with $G_{m1}R = G_{m2}R = 1$), the circuit operates as follows. In the acquisition mode, G_{m1} and R function as a unity-gain amplifier, allowing V_{out} to track V_{in}. In the hold mode, G_{m1} is disabled, G_{m2} is enabled, and G_{m2} and R are configured as a unity-gain amplifier, thereby retaining the sampled value of V_{in} across C_H.

The primary drawback of this circuit is the linearity required of the open-loop amplifier $G_{m1}R$. Furthermore, the deviation of $G_{m2}R$ from unity and the drive capability of the R stage are

also problematic [1]. With ±5-V supplies, various correction techniques can be applied to a basic linearized differential pair to achieve 10-bit linearity at sampling rates as high 75 MHz [9], but with a 3-V supply the design becomes much more difficult.

Another SHA topology in which the sampling switch introduces only a constant pedestal is the recycling circuit shown in Fig. 15 [10]. In the sampling mode, S_1, S_2, and S_4 are on and

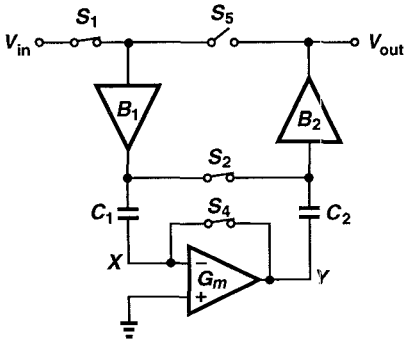


Fig. 15. Recycling SHA architecture.

the G_m stage establishes a virtual ground at X and Y. In the transition to the hold mode, first S_4 turns off, subsequently S_1 and S_2 turn off, and S_5 turns on. Thus, B_1, G_m, and B_2 constitute a unity-gain feedback loop, holding the sampled level on C_1. The settling speed of this circuit is still limited owing to the poles contributed by the three stages in the hold-mode feedback loop.

V. Design Examples

In this section, we present some of the new developments in the design of high-speed low-voltage sample-and-hold circuits.

A. Series Sampling with Source Follower

Fig. 16 shows a SHA circuit based on the series sampling technique described in Section III. The sampled voltage is buffered by a PMOS source follower, M_1, whose source-drain

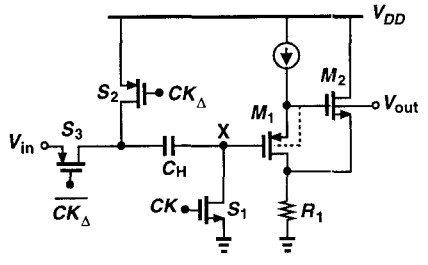


Fig. 16. Series CMOS sampler with bootstrapped buffer.

voltage is bootstrapped by M_2. The source of M_1 is connected to its n-well so as to eliminate the nonlinearity resulting from the body effect.

Bootstrapping improves several aspects of the performance. Since V_{DS1} is relatively constant, the effect of the output resistance of M_1 upon the input/output characteristic is minimal. This is especially important in submicron CMOS implementations because the output impedance of short-channel transistors *varies* with V_{DS}, causing substantial nonlinearity. Also, as the gate-drain capacitance of M_1 is bootstrapped, its loading effect at node X is reduced.

The speed of the circuit trades with the linearity through the junction capacitance of S_1 at node X. To achieve acceptable distortion, S_1 must be a narrow device or C_H a large capacitor, thus limiting the acquisition speed. Nevertheless, if the circuit is used in differential form, precisions as high as 10 bits can be attained at sampling rates exceeding 100 MHz.

B. Distributed Sampling

In flash or half-flash A/D converters, the front-end sampling can be merged with the bank of preamplifier stages to relax the trade-off between speed and precision. Illustrated in Fig. 17 [11], this technique is based on the fact that in a flash ADC,

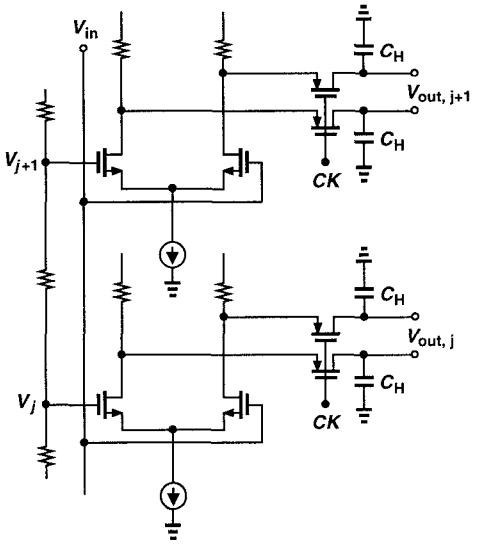


Fig. 17. Distributed sampling in flash stage.

only the input range in the vicinity of *one* ladder tap voltage is of interest at any given time. Thus, in every conversion period, the output of one of the preamplifiers accurately represents the difference between the input and the corresponding reference voltage and can therefore be sampled for further processing, e.g., folding, interpolation, or fine digitization.

The advantage of distributed sampling is that each SHA processes only a small voltage difference, alleviating issues related to input-dependent charge injection and voltage headroom. Of course, the preamplifiers must exhibit sufficient linearity for an input differential voltage approximately equal to $V_{j+1} - V_j$, but this range is typically a small fraction of the input full scale.

The distributed sampling technique has been employed in an 8-bit 80-MHz CMOS A/D converter with a power dissipation of 80 mW from a 3.3-V supply [11].

The chief drawback of distributed sampling is the reduction of the preamplifier bandwidth as a result of the output sampling circuit. Exacerbating the effect depicted in Fig. 4, this limitation leads to significant harmonic distortion at high input frequencies.

C. Switched Emitter Followers

As mentioned in Section III, emitter followers can operate as sampling switches if a means is provided to guarantee they remain off in the presence of large input swings. Shown in Fig. 18 is a differential SHA consisting of a unity-gain amplifier,

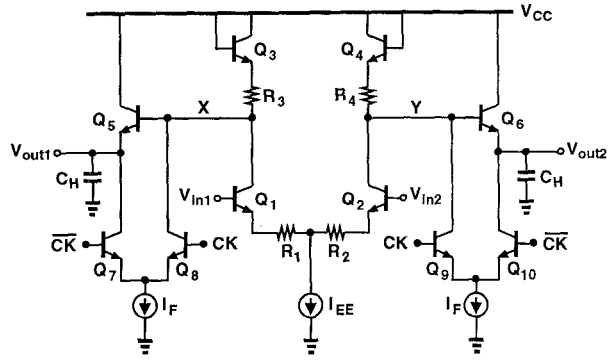


Fig. 18. SHA using switched emitter followers.

Q_1-Q_4 and R_1-R_4, and emitter followers Q_5 and Q_6 [7]. In the transition to the hold mode, the currents of Q_5 and Q_6 are switched to R_3 and R_4, respectively, so as to lower V_X and V_Y to the point where Q_5 and Q_6 are off even if Q_1 and Q_2 experience a large current swing. In practice, additional base-collector diodes are cross-connected from the input to X and Y to lower the hold-mode feedthrough [7].

While achieving a high speed and high linearity, the circuit of Fig. 18 requires a relatively large supply voltage, as seen in the path consisting of Q_3, R_3, Q_1, R_1 and I_{EE}. In fact, when designed for 10-bit linearity, the circuit accommodates only a 1-V input swing with a 5-V supply [7].

D. All-NPN Series Sampler

Since the series sampling technique of Fig. 6(b) isolates the input and output common-mode levels, it can alleviate the voltage headroom issues in an all-npn bipolar implementation. Fig. 19 shows an example [12]. The SHA employs two channels in a quasidifferential architecture to improve the overall

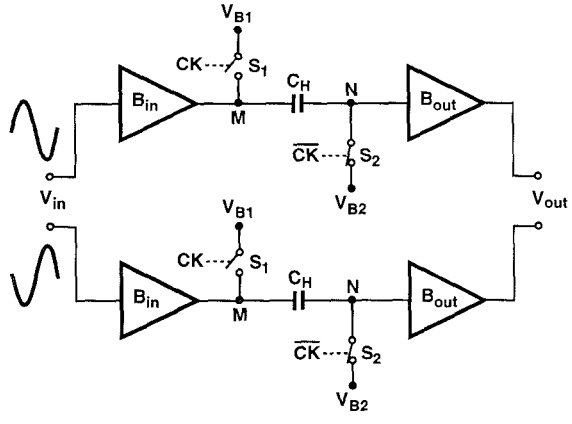


Fig. 19. Series Sampler architecture.

linearity and minimize the effect of common-mode pedestal and droop. Each channel consists of an input buffer B_{in}, a sampling capacitor C_H, and an output buffer B_{out}. In a fashion similar to that in Fig. 6(b), switches S_1 and S_2 connect nodes M and N to fixed potentials V_{B1} and V_{B2}, respectively. The input buffer is designed such that it is disabled when S_1 is on, thus operating as S_3 in Fig. 6(b).

The implementation of one channel is depicted in Fig. 20. Here Q_1 and Q_4 operate as input and output buffers, respectively, and Q_2 and Q_3 as switches. In the acquisition mode [Fig. 20(a)], Q_5 is on, drawing current from R_1 such that $V_P \approx -2$ V. Thus, Q_2 is off and Q_1 is on if V_{in} remains greater than V_P by a few hundred millivolts (condition 1). During this mode, Q_6 is also on, allowing Q_3 to clamp node N at $-2V_{BE}$. (The drop across R_2 is negligible). In the transition to the hold mode [Fig. 20(b)], Q_5 and Q_6 turn off and Q_7 turns on. Consequently, V_P rises to the ground potential, pulling node M high and turning Q_1 off if V_{in} remains less than zero by a few hundred millivolts (condition 2). Also, Q_7 draws current from R_2, turning Q_3 off rapidly.

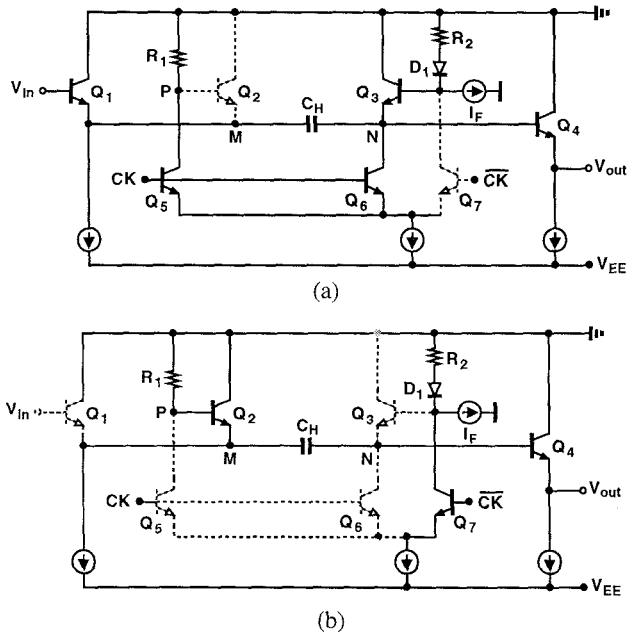


Fig. 20. Operation of one channel of series sampler, (a) acquisition mode, (b) hold mode.

From conditions 1 and 2, we note that each channel can accommodate input/output voltage swings of approximately 1.5 V, thus providing an overall differential full scale of 3 V with a 3.3-V supply.

As with the circuits of Figs. 6(b) and 16, the speed of this circuit trades with the nonlinearity of the parasitic capacitance seen at node N. This capacitance originates from the collector-base and collector-substrate junctions of Q_6, base-emitter junction of Q_3, and base-collector junction of Q_4. Thus, C_H must be large enough to achieve the required linearity.

Another issue in the circuit of Fig. 20 is the hold-mode feedthrough. Note that the base-emitter junction capacitance of Q_1, C_{je1}, conducts appreciably in the hold mode, and C_H does not attenuate the feedthrough signal. Fortunately, however, Q_2 is on in the hold mode, providing a relatively low

impedance from M to ground and forming a high-pass filter with C_{je1}. Also, the bottom-plate parasitic capacitance of C_H, placed at node M, further suppresses the feedthrough noise.

The all-npn SHA achieves a sampling rate of 100 MHz with a power dissipation of 10 mW while proving a 3-V differential swing with a 3.3-V supply voltage [12].

E. BiCMOS SHA

The low-voltage BiCMOS sampling switch of Fig. 10(c) can be used in a SHA environment to achieve a relatively high speed. We describe the actual implementation of the switch before presenting the design of the SHA.

The switched current source I_1 in Fig. 10(c) can be realized as shown in Fig. 21(a). However, the small transcoductance of M_2 and the large capaciatnce at node X yield a long time

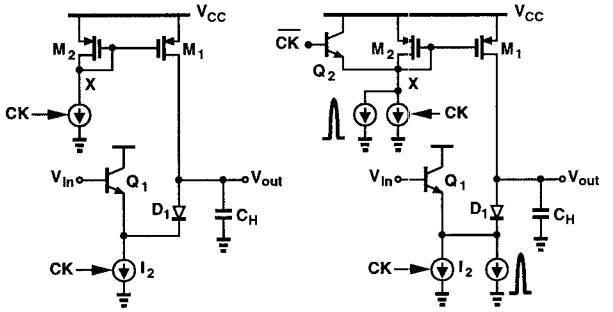


Fig. 21. (a) Implementation of low-voltage sampling switch, (b) speed-up by emitter follower and current impulse.

constant. Note that the time constant itself increases as M_2 turns off, slowing down the switching considerably. This issue is resolved as shown in Fig. 21(b) [6]. To minimize the aperture window, emitter follower Q_2 is added so that it rapidly pulls node X high when M_1 and M_2 must turn off. Also, to speed up the turn-on, an additional impulse of current is pulled from M_2 on the proper clock edge, thereby discharging X quickly.

Since M_1 and I_2 are driven by inherently different signal paths, it is difficult to guarantee that they switch simultaneously. It can be shown that if M_1 turns off before I_2, the sampled signal incurs harmonic distortion whereas if M_1 turns off after I_2, V_{out} experiences only a constant offset [6]. Thus, the timing is arranged such that I_2 always turns off a few hundred picoseconds earlier than M_1 does.

The BiCMOS SHA architecture is shown in Fig. 22. It consists of identical BiCMOS switches S_1-S_3, equal capacitors C_{H1} and C_{H2}, amplifier A_1, and a switch driver that interfaces the input clock with S_1 and S_2. Switch S_3 is always off and its role will be explained later. Outputs X and Y of the amplifier differ by one V_{BE} but are otherwise identical.

In the sampling mode, S_1 and S_2 are on, the voltage across C_{H1} tracks V_{in}, and A_1 is configured as unity-gain amplifier. In the hold mode, S_1 and S_2 are off and C_{H2} maintains a unity-gain loop around A_1. In this toplogy, both the charge injection of S_1 and S_2 and the hold-mode droop appear as a common-mode voltage at the inputs of A_1, thereby allowing the use of

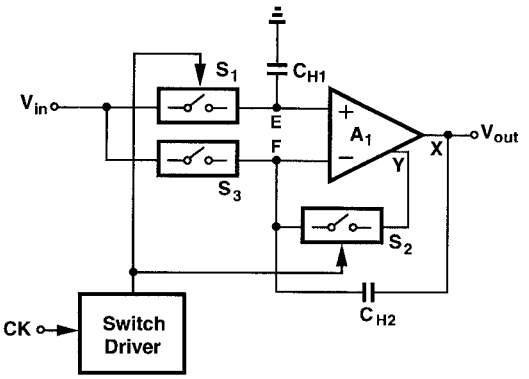


Fig. 22. BiCMOS SHA architecture.

smaller values for C_{H1} and C_{H2} than in a single-ended case.

The amplifier A_1 in Fig. 22 must efficiently drive the input capacitance of the following A/D converter while providing an output common-mode level approximately equal to mid-supply. Fig. 23 shows the evolution of the amplifier. The

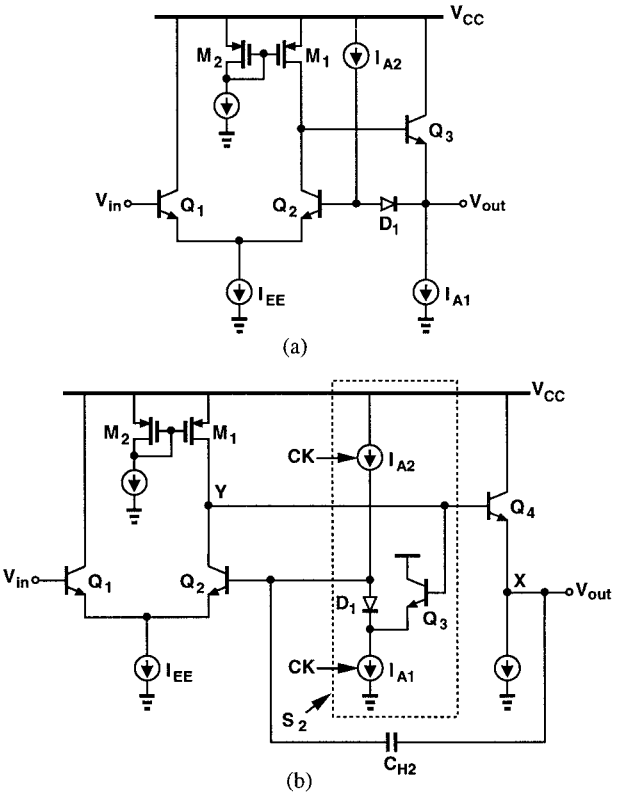


Fig. 23. (a) Unity-gain amplifier with feedback level shift, (b) conversion of feedback network to sampling switch.

circuit of Fig. 23(a) is a unity-gain buffer incorporating a level shifter (D_1 and I_{A2}) in the feedback path so as to allow operation from a 3-V supply [1]. Interestingly, the circuit comprising Q_3, D_1, I_{A1}, and I_{A2} happens to be the same as the sampling switch of Fig. 10(c) and can operate as such. As shown in Fig. 23(b), this structure performs the role of S_2 in Fig. 22. In order to maintain feedback after this switch turns off, another emitter follower, Q_4, and a capacitor, C_{H2}, are placed around the amplifier.

An important issue in the BiCMOS switch of Fig. 21 is

the hold-mode feedthrough path resulting from the junction capacitance of Q_1 and D_1. In the architecture of Fig. 22 this difficulty is overcome by allowing S_1 and S_3 conduct equal feedthrough signals to both inputs of the amplifier (Fig. 24). This technique remains effective as long as the output

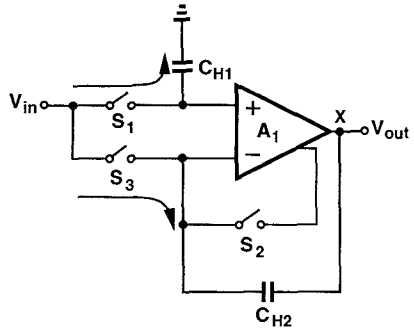


Fig. 24. Hold-mode feedthrough cancellation.

impedance seen at node X is sufficiently low.

The switch driver serves to provide proper timing for the two switches in Fig. 22. The details are described in [6]

The BiCMOS SHA operates at a sampling rate of 200 MHz while dissipating 15 mW from a 3-V supply [6]. The circuit provides 1.5-V single-ended swings, but it can easily be converted to differential form.

VI. SHA Characterization

Testing and characterization of high-speed SHAs are difficult, lengthy tasks, often requiring a different setup for measuring each parameter of interest. A dilemma in testing a stand-alone SHA that is intended for use at the front end of A/D converters is the output drive capability: if integrated along with the converter, the SHA need not drive a 50-Ω load, but in a high-speed test setup, it must.

Since direct measurement of the speed in the time domain usually demands custom-designed instrumentation circuits [1], in many cases the SHA output is characterized in the frequency domain, with the philosophy that incomplete acquisition or hold phenomena manifest themselves as distortion (or gain error) in the sampled signal.

The principal difficulty in obtaining the output spectrum of a sample-and-hold circuit is that if the entire output waveform is applied to a spectrum analyzer, the observed distortion susbtantially underestimates the performance. This is because slewing on the acquisition and hold "edges" of the signal waveform introduces distortion whereas the A/D converter digitizes only the *held* levels produced by the SHA.

In order to resolve both of the above issues, the output of the SHA under test can be resampled by means of another SHA that is integrated on the same chip and clocked properly [7, 13]. Illustrated in Fig. 25 for Nyquist-rate operation, the test setup drives SHA_1 with clock rate f_{CK} and an input sinusoid with frequency $f_{CK}/2 + \Delta f$, where Δf is a small number. The output of SHA_1 therefore contains spectral lines at $f_{CK}/2 \pm \Delta f$, both of which are translated to Δf upon resampling by SHA_2 at a rate $f_{CK}/2$. Proper phase adjustment

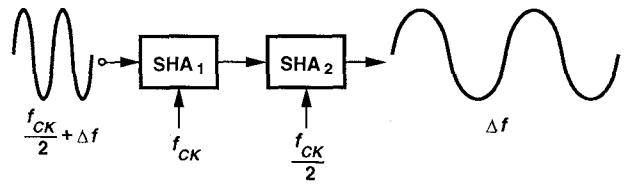


Fig. 25. Resampling test setup.

guarantees that SHA_2 samples only the held levels at the output of SHA_1, thus avoiding the distortion due to the acquisition and hold edges. Furthermore, the resampled output is at such a low frequency that 50-Ω terminations are not necessary.

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