CMOS Technology Characterization for Analog and RF Design

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Abstract

Characterization of CMOS technologies for digital applications often proves inadequate for analog and RF design. This paper describes a set of characterization vehicles and tests that quantify the analog behavior of active and passive devices in CMOS processes, in particular, properties that are not represented accurately in SPICE models. Test structures and circuits are introduced for measuring speed, noise, linearity, loss, matching, and dc characteristics.

I. Introduction

The semiconductor industry continues to challenge analog and RF IC designers with demand for higher performance and better compatibility with a digital world. Issues such as technology development costs, CAD infrastructure, and fabrication turnaround time make it desirable to use a single mainstream digital CMOS process for all IC products. "Analog processes" may be approaching extinction.

The design of analog and RF circuits in a digital CMOS technology entails many difficulties: the set of available active and passive devices is quite limited, the technology is optimized for digital design, and the devices are characterized and modeled according to simple benchmarks such as current drive and gate delay. While the first two issues can be somewhat alleviated by circuit and architecture innovations, the quandary of poor characterization leads to substantial conservatism in analog design, thus resulting in circuits that do not exploit the "raw" speed of the technology. In some cases, even conservatism does not solve the problem, mandating lengthy iterations in the design. For example, in a narrowband RF oscillator, it is difficult to guarantee a correct output frequency without accurate data on device parasitics and their variation with process and temperature.

This paper describes a set of technology characterization methods that provide the basic information required in analog and RF design. It also reviews some relevant modeling difficulties. Section II presents the motivation for and the issues related to the task. Sections III and IV deal with characterization for analog design and RF design, respectively. For the sake of brevity, we may use the term "analog" to mean "analog and RF."

II. Motivation and Issues

The principal difficulty in using a digital CMOS technology for analog design is that the process is optimized and characterized for primarily one trade-off: that between speed and power dissipation. By contrast, analog circuits entail a multidimensional design space. This is illustrated in Fig. 1, where almost every two parameters trade with each other. The true

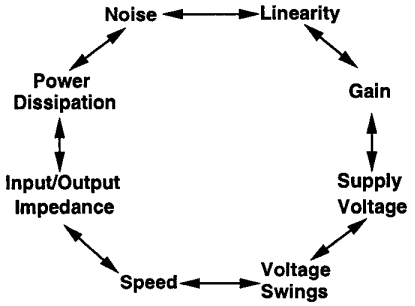

Fig. 1. Analog design octagon.

severity of these trade-offs is known only if relevant data has been obtained for the technology.

The need for specialized "analog characterization" arises from two types of shortcomings: inaccurate modeling (e.g., the output resistance of transistors or its nonlinearity), or simply lack of modeling (e.g., self-resonance frequency of inductors or matching properties of transistors). While efforts toward improving submicron device models continues vigorously, scaling appears to degrade the modeling accuracy faster. That is, it seems that for no generation of CMOS devices, models have been sufficiently accurate![1]

It is also important to note the rapid migration of digital circuits from one generation of the technology to the next. Analog circuits have historically lagged behind by more than one generation, failing to utilize the full potential of new processes or comply with their supply voltage scaling. A solid understanding of the properties and limitations of devices also minimizes the number of design iterations and hence the time to market.

The above observations indicate that analog design in a new technology can be greatly simplified if *measured* data points describing the analog behavior of devices and subcircuits are obtained. In fact, such data points do become available as analog designers begin to use a process, but in an ad hoc

[1] This is the author's opinion rather than a documented fact.

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manner and very slowly. A unified effort to collect all of the necessary data soon after the qualification of a technology is rarely seen.

Technology characterization for analog design nonetheless involves a number of difficult issues:

- Owing to the lack of universally-applicable analog benchmarks, many test structures must be built to satisfy the needs of various systems. Op amps, filters, comparators, data converters, oscillators, phase-locked loops, frequency synthesizers, and RF transceivers incorporate many different functions that heavily depend on poorly-modeled properties of devices.
- Some device characteristics, for example, capacitor mismatch and thermal and $1/f$ noise, are difficult to measure. Thus, proper circuits must be included on the die to allow reliable measurement.
- Some measured properties are difficult to incorporate in simulations. For example, the voltage-dependence of the output impedance of transistors cannot be easily included in the simulation of an op amp. Such cases may mandate designing a complete circuit to measure the overall effect.
- The large number of test structures requires substantial characterization time and effort. It is therefore desirable to automate the measurements to the extent possible.
- The test structures and circuits must be designed such that they can be ported into the next generation of the process with minimal modifications.

It is also beneficial to design two sets of structures: a comprehensive version to be used in the early phases of a new technology and a brief version to be included in product mask sets. The latter proves useful in detecting anomalies in the process.

III. Characterization for Analog Design

The device and circuit properties of interest in analog design can be grouped into six categories: (1) dc behavior, (2) ac behavior, (3) linearity, (4) matching, (5) noise, and (6) temperature dependence. We consider those aspects of each category that are not modeled accurately in SPICE simulations.

A. DC Behavior

Typical I_D-V_{DS} characterization seeks to minimize the *overall* error in the curve fitting procedure, thus incurring significant relative *local* errors. While advanced models such as BSIM level 13 and 39 incorporate many parameters to lower such errors, some submicron device properties still defy accurate representation. For this reason, it is important to have measured I-V data points in a range suitable to analog design.

Subthreshold characteristics of MOSFETs are difficult to model. (The BSIM level 39 model does represent this behavior, but it also yields a *negative* gate-source capacitance under certain conditions.) In sampled-data circuits, the subthreshold conduction of switches in the off state, especially at high temperatures, may lead to significant leakage, thereby corrupting the stored information. This effect also becomes important in determining the lower bound on the speed of dynamic latches in mixed-signal and digital circuits.

A difficulty in subthreshold modeling is dc and ac slope discontinuity in the vicinity of strong inversion as V_{GS} increases. In fact, time-domain simulation of circuits in which MOSFETS reciprocate between the two regions exhibit substantial dynamic errors. For example, in two-tone simulations of RF CMOS circuits, the output spectrum often suffers from a high noise floor that is an artifact of slope discontinuities in the device models. This issue remains unresolved.

Subthreshold operation actually proves useful in some cases. For example, as depicted in Fig. 2, a diode-connected MOSFET biased in subthreshold exhibits a large incremental resis-

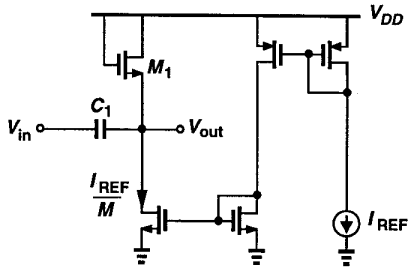

Fig. 2. AC coupling using devices biased in subthreshold region.

tance, thus creating a low cut-off frequency in the high-pass filter formed with C_1. By contrast, a resistor of comparable value would consume a large area and introduce considerable parasitic capacitance at the output node. The circuit of Fig.2 can be employed if the subthreshold properties of transistors are known at different temperatures.

Another troublesome effect is the output resistance of short-channel MOS transistors and in particular its *variation* with the drain-source voltage even in the saturation region. Shown in Fig. 3, this phenomenon causes the intrinsic gain, $g_m r_o$, to

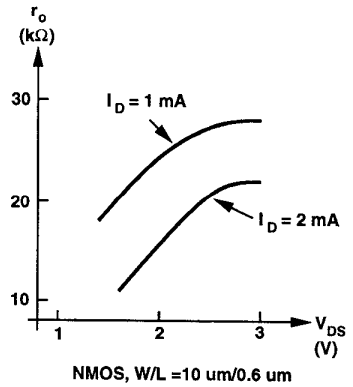

Fig. 3. Measured variation of MOS output resistance vs. V_{DS}.

depend on the output potential, thereby creating nonlinearity in amplifiers. Present models include this behavior but with more than 50% error in some cases.

For op amp design, it is useful to obtain measured plots of $g_m r_o$ as a function of the drain current for various device dimensions.

The nonlinear dependence of the threshold voltage, V_{TH}, on the source-bulk potential difference is another quantity that suf-

fers from poor modeling and impacts the performance of some circuits. In addition to nonlinearity in source followers that experience source-bulk voltage change, the variation of V_{TH} also gives rise to input-dependent charge injection in MOS switches (Fig. 4). Approximated as $Q_{ch} = WLC_{ox}(V_{GS} - V_{TH})$, the

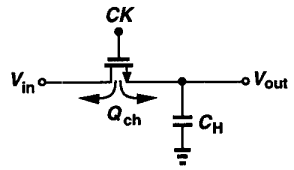

Fig. 4. Input-dependent charge injection.

channel charge exhibits a nonlinear component because V_{TH} does not vary linearly with the input signal. Measurement of V_{TH} versus the source-bulk voltage yields results that can be incorporated in hand calculations of the nonlinearity.

B. AC Behavior

The discrepancy between the simulated and measured speed of MOS devices and circuits continues to haunt designers. For example, the device models extracted from a wafer often fail to accurately predict the gate delay of ring oscillators fabricated on the same wafer.

In order to obtain a versatile set of data points, ac characterization of a technology must be performed at both device level and circuit level. For devices, f_T and f_{max} must be measured under bias conditions common in analog circuits, e.g., $V_{GS} - V_{TH} \approx 100, \cdots, 500$ mV and $I_D \approx 5, \cdots, 20\mu A/\mu m$. For a given current, $f_T \propto (V_{GS} - V_{TH})$ [1], indicating that the f_T's encountered in analog applications are much lower than those measured with $V_{GS} = V_{DD}$, the value typically reported for CMOS technologies.

Another ac device parameter of interest is the nonlinearity of MOS gate-channel capacitance in accumulation and inversion. This effect can be better seen by plotting the *derivative* of the C-V data versus the gate-channel voltage (Fig. 5). While MOS capacitors are quite nonlinear, they nonetheless prove

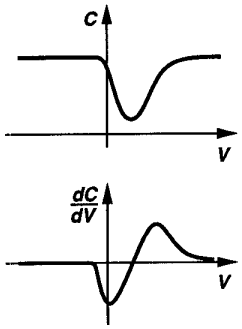

Fig. 5. Capacitance-voltage characteristic of a MOS device along with its derivative.

useful in some analog circuits [2].

MOS capacitors are also utilized as supply and bias by-pass elements (Fig. 6). In such cases the series resistance of the capacitor impacts the effectiveness of the by-passing. For

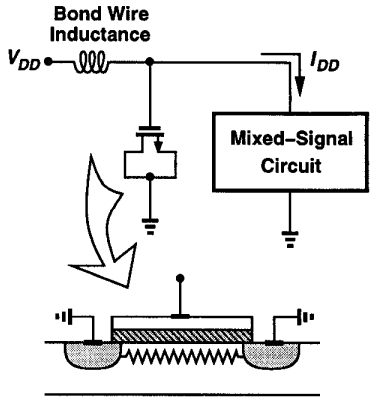

Fig. 6. MOS capacitors as by-pass elements along with illustration of channel resistance.

example, the resistance can be used to produce a critically-damped response if lead inductance or current slew rates are significant [3]. The series resistance is readily calculated in the strong inversion region [4], but its value in accumulation must be measured.

Another rarely-available process parameter is the capacitance of the n-well to the substrate. If the source and n-well of a PMOS device are connected to avoid body effect (Fig. 7), the n-well capacitance must be taken into account. The

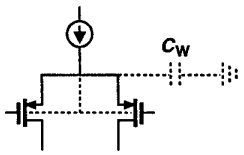

Fig. 7. N-well capacitance in a PMOS differential pair.

capacitance of resistors made of n-well may also be important. In Fig. 8, for example, resistor R_b and transistor M_b set

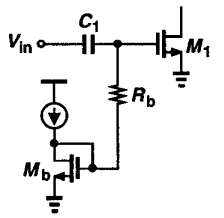

Fig. 8. Bias circuit using n-well resistor.

the bias current of M_1, thus allowing ac coupling of the input signal. In this circuit, the value of R_b is not critical so long as it remains much greater than the output impedance of the preceding stage, but the parasitic capacitance of R_b attenuates the signal if C_1 cannot be large.

For ac characterization at circuit level, frequently-used building blocks can serve as test vehicles. The choice of a circuit for this purpose is determined by three factors: (1) the complexity and design time of the circuit, (2) the useful information obtained from testing the circuit, and (3) the level of difficulty in *testing* the circuit. Differential ring oscillators (Fig. 9) with realistic device dimensions and bias currents are more widely

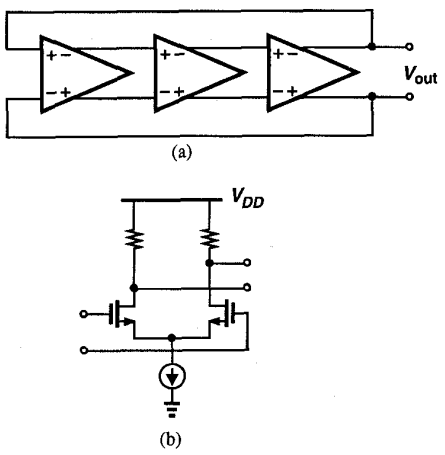

Fig. 9. (a) Differential ring oscillator, (b) implementation of one stage.

accepted than single-ended topologies. The speed of these circuits and its correlation with process corner models constitute a more reliable basis for design than those of ring oscillators using simple inverters.

Another circuit that exercises the intrinsic speed of the technology is a voltage comparator. Fig. 10 shows an example, where M_1 and M_2 amplify the input difference and M_3 and

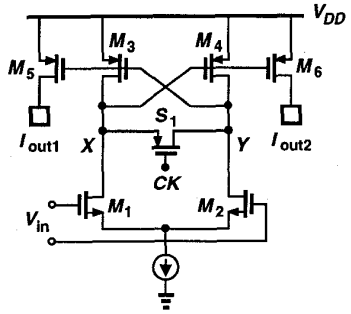

Fig. 10. Simple comparator for measuring metastability.

M_4 perform regeneration after S_1 turns off. The regeneration speed at nodes X and Y can be measured by operating the comparator near metastability [5, 6] and measuring the *change* in the response time for small increments in the input voltage. In practice, all the dimensions and bias currents may be scaled up by a factor of 100 so that the currents provided by M_5 and M_6 generate moderate voltage swings in a 50-Ω instrumentation environment. Note that such scaling does not change the regeneration time constant.

C. Linearity

The linearity of both passive and active devices plays a critical role in many analog circuits. The value of a resistor or a capacitor can be expressed in terms of the voltage across the device as $x \approx x_0(1 + \alpha_1 V + \alpha_2 V^2)$. The coefficients α_1 and α_2 must be measured for different types of resistors and capacitors available in a process. Note that the linearity of polysilicon resistors typically improves with the length [7].

The linearity of op amps is also of great interest. In a conservative design, the open-loop gain of the circuit is chosen large enough to obtain a small closed-loop *gain error*, thus guaranteeing that the nonlinearity is of the same order. However, the low $g_m r_o$ of submicron devices makes it difficult to achieve a high open-loop gain. Furthermore, gain error per se is not critical in many applications or it can be corrected by calibration techniques. Thus, aggressive designs seek to minimize the nonlinearity by *adequate* open-loop gain. This is possible only if the nonlinearity of the open-loop circuit is well understood.

In a fully differential op amp, e.g., Fig. 11, the nonlinearity arises from two principal sources: compressive voltage-

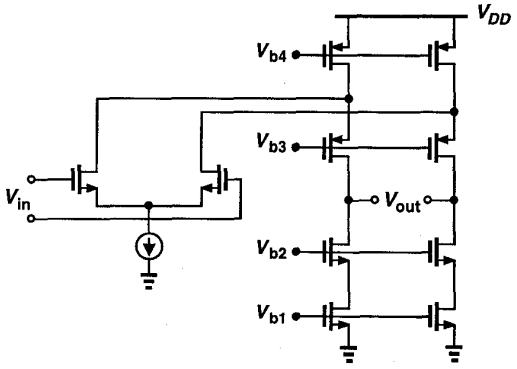

Fig. 11. Folded-cascode op amp (common-mode feedback not shown).

to-current conversion of the input differential pair and the voltage-dependence of the output impedance of the cascode devices. The nonlinearity can be measured by means of the configuration shown in Fig. 12, where all the passive devices

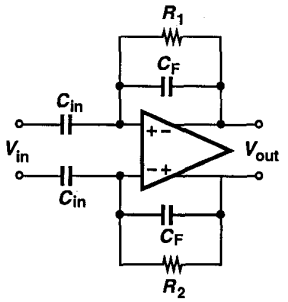

Fig. 12. Arrangement for measuring op amp distortion.

may be external for simplicity. Resistors R_1 and R_2 establish the bias but are large enough to be considered ac open. With a pure sinusoid applied to the input and different choices of C_{in}/C_F, the output harmonic contents can be measured and the "static" nonlinearity of the open-loop op amp derived.

D. Matching

While matching properties of passive and active devices have been extensively studied in terms of dimensions and process constants [8]-[11], actual measurement of mismatches is often necessary. This is because, in addition to fundamental parameters such as device area, other characteristics such as

"cleanness" of the process determine the magnitude of mismatches as well.

Measurement of resistor and transistor matching is straightforward. The test structures must employ many different dimensions so as to quantify the dependence on the area. Fig. 13(a) shows an arrangement with minimum number of pads for measuring the gate-source voltage of each transistor in every differential pair. A tail current is drawn from the common source node of the pair, node X or node Y is tied to V_{DD}, and the other is connected to ground, thus establishing the value of V_{GS}. Using this technique, the V_{GS} mismatch can be measured as a function of the drain current. The resistor-capacitor network prevents oscillations due large parasitic inductances in the setup.

It is also desirable to include nominally-identical current sources [Fig. 13(b)]. Since the mismatch between two current

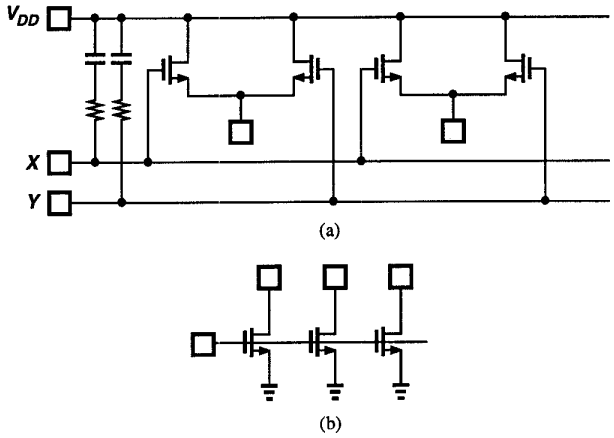

Fig. 13. Structures for measuring device mismatch.

sources depends on both the threshold voltage mismatch and $\mu C_{ox} W/L$ mismatch [11, 6], measurements on both structures in Figs. 13(a) and (b) allow cross-checking the validity of the extracted data.

Measurement of resistor mismatch usually requires a four-point ("force" and "sense") arrangement so as to avoid resistance mismatches due to external connections. The topology shown in Fig. 14 allows such a measurement with a relatively small number of pads.

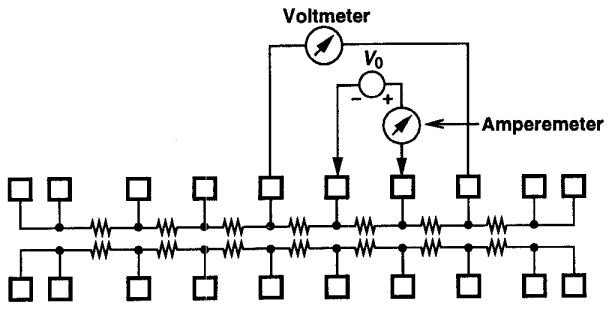

Fig. 14. Topology for measuring resistor mismatch.

Characterization of capacitor matching is quite difficult. For small capacitors used in most analog circuits, in the range of 0.1 to 1 pF, direct measurement would suffer from many uncertainties resulting from parasitics in the physical setup. Thus, the capacitors must be isolated from external connections by means of on-chip circuitry.

Fig. 15 illustrates an efficient approach to measuring capacitor mismatch [12]. The top plates of C_1 and C_2 are connected

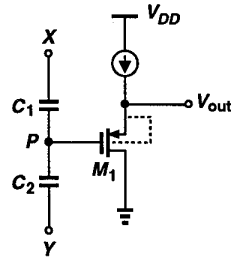

Fig. 15. Capacitor mismatch measurement.

to node P and a PMOS source follower serves as a buffer. The n-well of M_1 is tied to its source to eliminate the nonlinearity due to body effect. The test proceeds by applying a ramp to X while Y is grounded, generating a ramp at V_{out} whose slope is approximately equal to $S_1 = C_1/(C_1 + C_2)$. Next, X and Y are interchanged and the output slope, $S_2 = C_2/(C_1 + C_2)$, is obtained. The relative mismatch can then be calculated as

$$2\frac{S_1 - S_2}{S_1 + S_2} = 2\frac{C_1 - C_2}{C_1 + C_2}. \quad (1)$$

Utilizing only the *change* in V_{out}, this approach cancels the effect of three nonidealities: (1) initial charge at node P, (2) parasitic capacitance at node P, including the input capacitance of the source follower, and (3) drain-source impedance of M_1 [12]. The measurement must nonetheless be performed with relatively large voltage excursions so as to calculate the difference between S_1 and S_2 accurately.

E. Noise

The thermal noise of submicron MOS transistors does not satisfy the long-channel approximation $\overline{i_n^2} = 4kT[2/(3g_m)]$ [13]. Depending on the bias conditions, the "excess noise factor" may be quite higher than $2/3$, an issue not reflected in present SPICE models. Moreover, the $1/f$ noise calculation of MOSFETs requires the technology constant K_F in $\overline{v_n^2} = 4kTK_F/(WLC_{ox})$, which must be measured for both PMOS and NMOS devices.

Direct measurement of device noise is quite difficult simply because the values to be measured are too small to be sensed properly by typical instrumentation. Some amplification is therefore necessary, but the noise contributed by the gain stage(s) must be sufficiently lower than that of the device under test.

Fig. 16 shows an arrangement for measurement of both thermal and $1/f$ noise of MOSFETs. Biased by means of M_0 and I_{REF}, the transistor under test, M_1, forms a cascode configuration with M_2, providing an intrinsic voltage gain of approximately $g_{m1}g_{m2}r_{o1}r_{o2}$. The external resistor R_L is

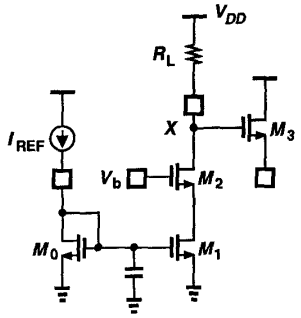

Fig. 16. Arrangement for measuring device noise.

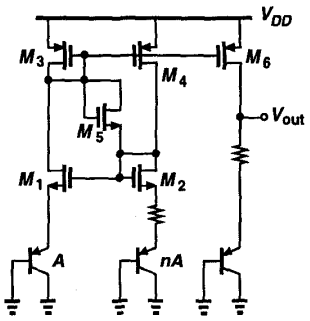

Fig. 17. Simple bandgap reference. (Transistor M_5 serves as startup.)

chosen to be higher than the output impedance of the cascode to avoid lowering the voltage gain. A high value for R_L also minimizes its noise contribution. Note that the effect of the noise generated by M_2 is negligible at low frequencies if $g_m r_o$ exceeds approximately 4.

The large value of R_L together with typical bias currents used in the test translates to a relatively high supply voltage, but V_X can be maintained below the maximum allowable value to avoid stressing the cascode device. To minimize drifts in V_X, some dc feedback may be added from X to the gate of M_1. The source follower, M_3, lowers the output impedance of the circuit, an important provision because the input noise current of the external sensing circuitry may be significant.

Since power supplies and biasing networks typically exhibit considerable noise, the circuit of Fig. 16 must be supplied from a low-noise battery. Furthermore, the supply line, the gate-source bias of M_1, and the gate bias of M_2 must be bypassed by several capacitors ranging from a few nanofarads to several hundred microfarads.

F. Temperature Dependence

The temperature variations of many device parameters are not modeled accurately in SPICE. Examples include output resistance, mobility, subthreshold conduction, and capacitances. Furthermore, the temperature coefficient of resistors and capacitors must be measured for each technology generation as it may depend on doping levels or the type of dielectrics.

In addition to basic device parameters, some other circuit-related quantities should also be characterized as a function of temperature. For example, direct measurement of the variations of the transconductance, on-resistance, and threshold voltage provides a more reliable and versatile characterization, thus simplifying the design procedure.

The ac properties of the technology also vary with temperature. The ring oscillator and comparator circuits described in Section III.B can serve as structures allowing the measurement of speed as a function of temperature.

Another useful test structure is a simple bandgap reference [14]. Depicted in Fig. 17, such a circuit finds wide use in most analog and mixed-signal systems. With a simple version of the reference available in the early phases of technology qualification, subsequent iterations in the design are minimized.

IV. Characterization for RF Design

Most of the analog characterization methods described above also prove essential to RF design. In particular, dc and ac properties, noise, and temperature dependence are critical here as well. In addition, many RF characteristics must be measured at device and circuit levels to facilitate the design of highly-integrated RF systems.

A. Device Properties

The severe trade-offs between noise, frequency of operation, gain, and power dissipation in RF circuits limit the number of active devices in the signal path of some building blocks. Examples include low-noise amplifiers (LNAs), mixers, and oscillators. Consequently, passive monolithic devices that exhibit little loss and operate as high-quality loads or interfaces can greatly simplify the design. Inductors, capacitors, varactors, and transformers appear in many RF ICs today.

While the value of spiral inductors can be calculated with reasonable accuracy [15], the Q and self-resonance frequency are much more difficult to predict. The distributed nature of the spiral and the underlying substrate usually requires the use of finite element analysis, especially for complex structures such as stacked inductors [16]. Furthermore, the dependence of inductor parameters upon line width and spacing, the number of turns, the size of the opening in the middle, and the type of the "shield" placed underneath the inductor [17] makes it difficult to choose the optimum structure for a give frequency of operation. For these reasons, it is beneficial to obtain measured data for parameters of inductors with different geometries. Shown in Fig. 18 are two structures of interest in RF design [18].

A simple method of measuring the Q and the self-resonance frequency, f_{SR}, of inductors is illustrated in Fig. 19. Identical inductors L_1 and L_2 together with the negative-G_m pair M_1 and M_2 form an oscillator. If the capacitance contributed by the transistors and the output buffer is negligible with respect to the parasitic capacitance of L_1 and L_2, the circuit oscillates at f_{SR}. Moreover, if the tail current is decreased until the oscillation is near failure, the negative transconductance provided by M_1 and M_2 is approximately equal to the equivalent parallel resistance of the inductors, i.e., $-1/g_m = R_p$. Thus, $Q = R_p/(L\omega) = (L\omega g_m)^{-1}$. The value of g_m under this

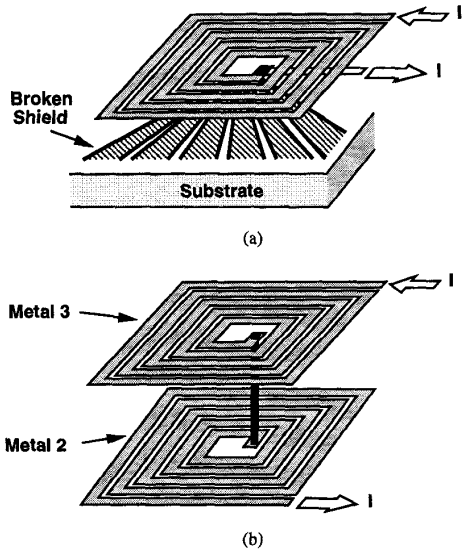

Fig. 18. (a) Inductor with broken shield, (b) stacked inductors.

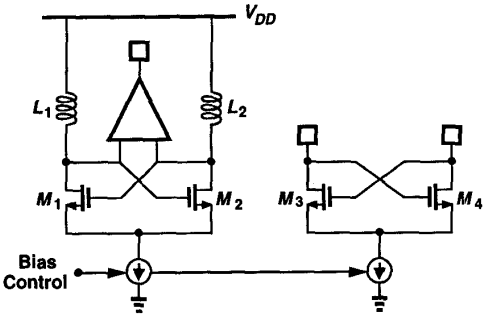

Fig. 19. Arrangement for measuring self-resonance frequency and Q of inductors.

condition can be measured for M_3 and M_4, which are identical to M_1 and M_2.

Varactors built in CMOS technology also suffer from a low quality factor. Depicted in Fig. 20, a floating varactor exhibits substantial series resistance due to the n-well material. Direct

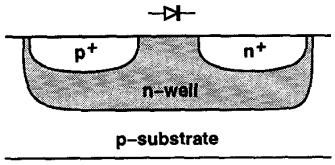

Fig. 20. Floating varactor in CMOS technology.

measurement of the varactor provides an equivalent lumped value for the two-dimensional distributed resistance of the structure.

Another useful passive component is a transformer. Monolithic transformers suffer from parasitic capacitances and frequency-dependent voltage and power loss [19, 20]. Measurement of these parameters can lead to a model suited to circuit simulations. A simple transformer-based oscillator, e.g., that in Fig. 21, can also yield the self-resonance frequency and

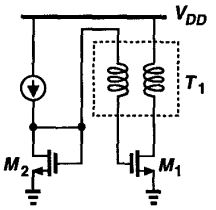

Fig. 21. Transformer-based oscillator.

loss of the structure.

B. Circuit Properties

The design of such RF building blocks as LNAs, mixers, oscillators, modulators, and power amplifiers heavily depends on the overall transceiver architecture and the intended wireless standard. For this reason, it is difficult to introduce test vehicles that provide useful data for various RF applications. For example, the design of an LNA that must drive a 50-Ω load may be significantly different from one that need not. Thus, RF characterization circuits are somewhat specialized.

A critical issue in today's RF CMOS design is the substantial variability of device and circuit parameters with process and temperature. While analog circuits have, for decades, utilized tracking and cancellation techniques to achieve well-defined, stable parameters, RF circuits still lack such precautions. For example, since the gain of LC-tuned amplifiers is a strong function of parasitic capacitances, it must be measured on various wafers from different lots so as to obtain a realistic distribution. Similarly, the center frequency of typical oscillators, e.g., that in Fig. 19, must be measured on many dice and at temperature extremes to yield the required tuning range.

Matching properties play an important role in many RF circuits. Fig. 22 illustrates an example of measuring the phase and gain mismatch between two RF mixers. The high-

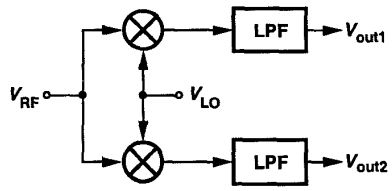

Fig. 22. Arrangement for measuring phase and gain mismatch between two RF mixers.

frequency inputs, V_{RF} and V_{LO}, directly drive the two mixers to avoid mismatches in the external connections. If the frequency difference between the two inputs is relatively small, V_{out1} and V_{out2} have a low frequency and hence their phase and amplitude mismatch can be measured with high precision.

Another useful benchmark is a frequency divider. Divide-by-two circuits [Fig. 23(a)] and dual-modulus dividers [Fig. 23(c)] find wide usage in quadrature generation and frequency synthesis, respectively. At present, the power-speed trade-off of these circuits is much more severe in CMOS technology than

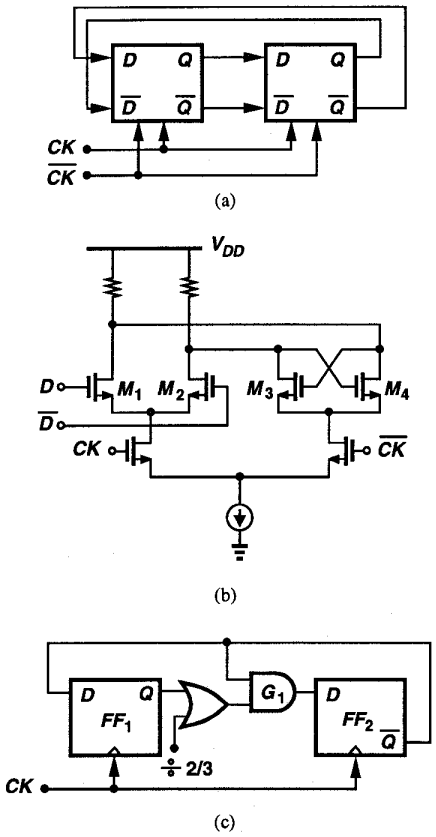

Fig. 23. (a) Divide-by-two circuit, (b) implementation of one stage in (a), (c) $\div 2/3$ circuit.

in bipolar implementations. Furthermore, significant discrepancy is often observed between the simulated and measured speed-power trade-off of the circuits. Thus, measured data corresponding to different divider topologies proves valuable.

Power amplifiers (PAs) are also critical components whose design remains a formidable task. Owing to large current and voltage changes that the output transistor in a PA experiences, accurate device modeling to predict efficiency and linearity has become a serious issue. As a result, PA design heavily relies on the data measured for single transistors. Thus, large MOSFETs with proper layout and pad configurations must be included to allow high-power high-frequency characterization.

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