11.9 A 0.13μm CMOS UWB Transceiver

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Ultra-wideband (UWB) communication in the form of direct sequence or orthogonal frequency division multiplexing (OFDM) has been proposed for high-date-rate applications. In this paper, a UWB transceiver designed for OFDM systems operating in the "Mode 1" bands (centered at 3432MHz, 3960MHz, and 4488MHz) is described. Each band occupies 528MHz and can accommodate data rates as high as 480Mb/s.

In addition to broadband gain and input matching requirements, the UWB standard also poses a tight specification on the band switching time (9ns), thus precluding the direct synthesis of frequencies by phase locking. An approach suggested for this task incorporates a single phase-locked loop (PLL) and a number of single-sideband (SSB) mixers to generate different frequencies that are present at all times and can be simply selected as the local oscillator (LO) signal [1]. Unfortunately, SSB mixing suffers from several drawbacks: (1) At least one signal applied to each "submixer" in an SSB system must contain a low harmonic distortion, a very difficult issue with respect to waveforms generated by practical gigahertz oscillators. (Reduction of harmonics by means of filtering requires a great deal of power dissipation.) (2) The port of each submixer that senses the low-distortion sinusoid must itself provide high linearity, inevitably creating a high loss and demanding a high power dissipation to amplify each final (I and Q) output and achieve levels suited to the receive and transmit mixers. (3) Even with these precautions, phase and gain mismatches at several gigahertz lead to many spurious components at the output of SSB mixers.

In this work, the three LO frequencies necessary for Mode 1 are produced by three fixed-modulus phase-locked loops, thus avoiding SSB mixers. System simulations suggest that a (wideband) phase noise of –100dBc/Hz degrades the sensitivity by 0.2dB, making ring oscillators a possible candidate. With each PLL drawing about 10mW, this approach in fact consumes less power than SSB mixers while remaining free from distortion and spur issues.

Figure 11.9.1 shows the direct-conversion transceiver architecture. In the receive path, a low-noise amplifier (LNA) with three switched resonant networks drives three sets of I and Q mixers, one of which is activated according to the band select (BS) command. The baseband signals are applied to a fourth-order Sallen and Key (SK) filter, programmable gain stages, and a first-order RC filter. In the transmit path, the baseband signals are applied to a similar SK filter and subsequently quadrature mixers that receive the proper LO frequency according to BS. To avoid an explicit transmit/receive switch, a mechanism is employed (explained below) that allows shorting the LNA input to the transmitter output.

The receiver incorporates a gain switch of 16dB in the LNA, six 6dB gain steps in the down-conversion mixers, and seven 2dB steps in the baseband. The design of the LNA is governed by several challenging requirements. Broadband input matching and frequency response can be achieved through the use of *LC* ladders at the input of cascode stages [2,3]. However, at low supply voltages, it is difficult to employ shunt peaking at the drain node. Furthermore, the input matching degrades if the gain of the LNA is to be switched by a large factor. Thus, a cascode common-gate (CG) stage with low-Q tanks is used in this design. Shown in Fig. 11.9.2, the LNA employs M_1 and M_2 as a CG stage and M_3-M_5 as switched cascode devices with tanks resonating at the center frequency of each band. The Q of the tanks is lowered to about 3 to ensure a small droop near the band edges. The source inductance, $L_1 \approx 20$nH, resonates with the total capacitance at this node at near 3.5GHz, thus presenting a relatively high impedance across all three bands.

The LNA gain reduction is accomplished by turning M_1 off ($W_1 \approx 8W_2$). The resulting increase in the input impedance is compensated by turning M_6 on. The on-resistance of M_6 varies with process and temperature but the correction still guarantees $|S_{11}| > 10$dB under all conditions. Each of the down-conversion mixers is implemented as illustrated in Fig. 11.9.3. Resistor R_H carries about half of the bias current of M_1, allowing M_2 and M_3 to switch more efficiently as well as accommodating a larger value for the mixer load resistance and hence the conversion gain. (The common-mode level of the LO is set by means of a tracking circuit to ensure a well-defined current through R_H.)

To obtain gain steps that are "linear in dB," the output currents of the mixer are switched into different taps along a binary-scaled ladder. This topology offers both a high linearity and a constant output impedance (necessary for the subsequent filter).

The SK filter following the mixer must achieve a bandwidth of greater than 300 MHz. Therefore, the core amplifier of the filter consists of a simple degenerated differential pair having an open-loop gain of 2 and buffered by source followers. Using the load resistors of the mixer as part of its input network, the filter provides a relatively low impedance at the mixer output nodes, thereby avoiding compression at these nodes.

Figure 11.9.4 depicts the transmitter along with the receiver and the antenna interface. The up-converter outputs are applied to a differential to single-ended converter consisting of M_1-M_3. Inductor L_1 resonates with a low Q, improving the bandwidth above 4 GHz. Transistor M_4 delivers an output level of –10dBm to the antenna while the LNA is disabled. As a result of the capacitance introduced by M_4 at the antenna port, the above RX/TX switching scheme entails a trade-off between the TX output power and the degradation of the RX noise figure. In the present design, this degradation is about 0.2 dB. The UWB transceiver is realized in 0.13μm CMOS technology. Depicted in Fig. 11.9.7, the die occupies an active area of 0.9mm×0.8mm^2. The circuit is tested with a 1.5V supply.

Figure 11.9.5 summarizes the measured results. The noise figure varies from 5.5dB in bands 1 and 2 to 8.4dB in band 3. Since the communication resides in each band for 1/3 of the time, the three noise figures are essentially averaged, falling close to the value recommended in [1]. In addition to in-band 1dB compression tests, the receiver is also subjected to tones in 2.4GHz and 5.2GHz bands. The gain in Band 1 degrades by 1dB as the 2.4GHz tone reaches –28.5dBm. Similarly, the gain in Band 3 falls by 1dB as the 5.2GHz tone approaches –17dBm.

Figure 11.9.6 shows the transmitter output with 4MHz tones applied to the baseband. With a cable loss of 1.1dB, the output power is –10.5dBm. Due to poor I/Q matching of the external signals, the unwanted sideband (on the left) is about 27dB below the desired sideband. The output 1dB compression of the transmitter is equal to –10dBm.

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References:
[1] A. Batra et al., Multi-Band OFDM Physical Layer Proposal, IEEE 802.15-03/267r5, July, 2003.
[2] A. Bevilacqua and A. Niknejad, "An Ultrawideband CMOS LNA for 3.1 to 10.6GHz Wireless Receivers," *ISSCC Dig. Tech. Papers*, pp. 382-383, Feb., 2004.
[3] A. Ismail and A. Abidi, "A 3 to 10GHz LNA Using a Wideband LC-Ladder Matching Network," *ISSCC Dig. Tech. Papers*, pp. 384-385, Feb., 2004.

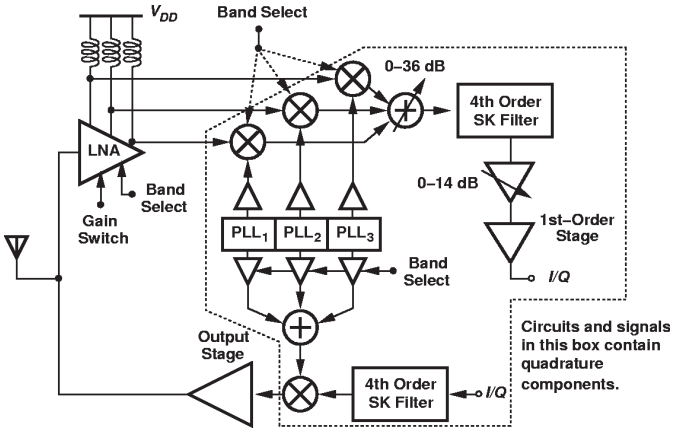

Figure 11.9.1: Transceiver architecture.

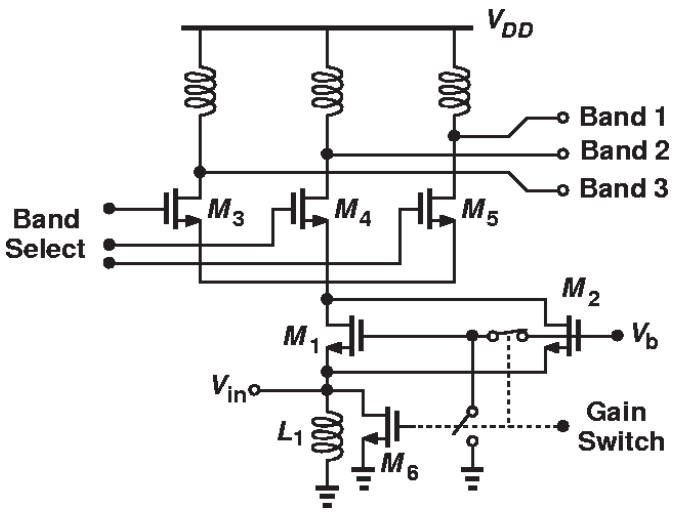

Figure 11.9.2: Low-noise amplifier.

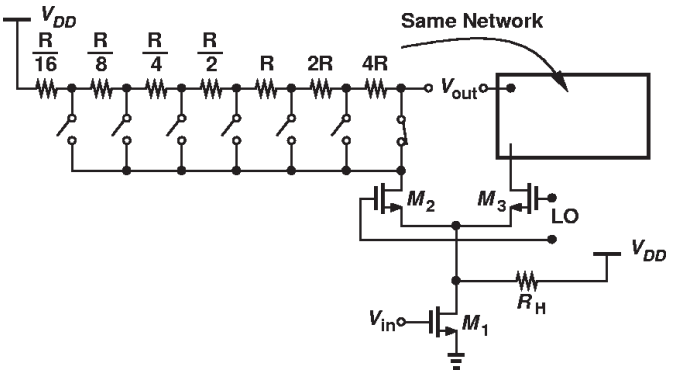

Figure 11.9.3: Mixer.

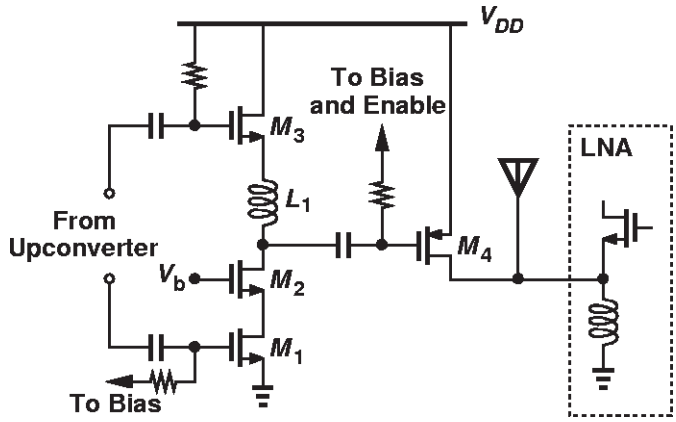

Figure 11.9.4: Transmitter and its interface with receiver.

Voltage Gain	**69–73 dB**
Noise Figure	**5.5 – 8.4 dB**
In–Band 1–dB Compression Point	
High LNA Gain	**–27.5 – –29.5 dBm**
Low LNA Gain	**–9.5 – –12.5 dBm**
S11	
High LNA Gain	**–12 dB**
Low LNA Gain	**–11 dB**
TX Output 1–dB Comp.	**–10 dBm**
Phase Noise @ 1–MHz Offset	**–104 – –108 dBc/Hz**
Power Dissipation	**105 mW**
Supply Voltage	**1.5 V**
Technology	**0.13–um CMOS**

Figure 11.9.5: Measured performance of transceiver.

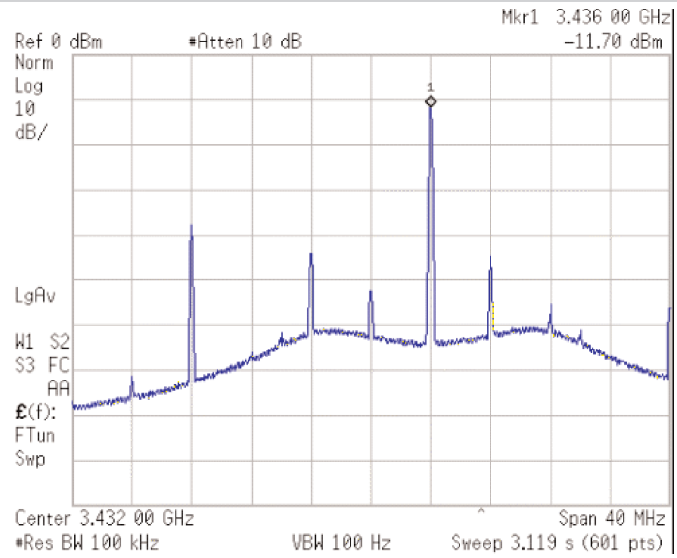

Figure 11.9.6: Transmitter output spectrum.

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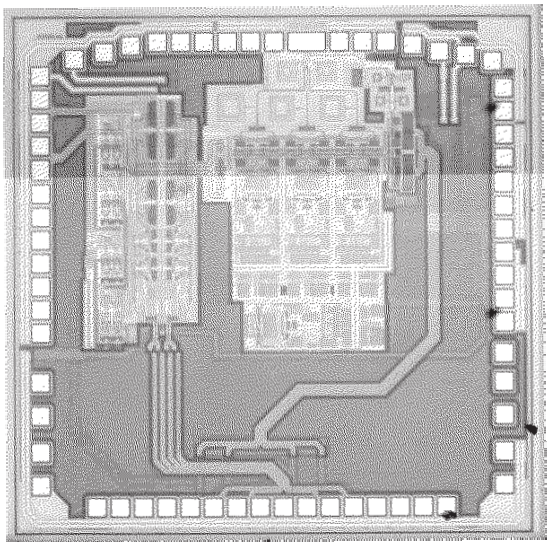

Figure 11.9.7: Transceiver die photograph.

