TP 3.1: A 1.5V 900MHz Downconversion Mixer

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The demand for fewer batteries and lighter weight in portable RF transceivers has motivated efforts to reduce the supply voltage of both analog and digital building blocks of such systems. In front-end RF circuits, however, trade-offs among six parameters have constantly challenged the designers: noise, power dissipation, linearity, voltage headroom, gain, and operating frequency. While upconversion mixers with supplies as low as 2V have been reported, noise, speed, and supply rejection issues prohibit the use of such topologies for downconversion [1].

This 900MHz downconversion mixer employs circuit techniques to relax some of the above trade-offs. The fully-differential circuit consists of a core and an output buffer/amplifier, and operates from a 1.5V supply.

A differential Gilbert cell mixer employing resistive degeneration suffers from three drawbacks: (1) the thermal noise due to the degeneration resistor imposes a trade-off among linearity, power dissipation, and noise figure; (2) the stacked differential pairs require a supply voltage greater than $2V_{BE}$; (3) as the minimum allowable voltage across the load resistors and the tail current sources is reduced, their contribution to the noise figure increases. To alleviate the first drawback, the degeneration resistor is replaced by a capacitor, C_{EE}, with impedance in a 25MHz band around 900MHz such that the conversion gain and hence the third intercept point (IP_3) remain the same (Figure 1). Two-tone simulations confirm that resistive and capacitive degeneration linearize the input differential pair by the same amount. Equivalently, for a given IP_3 and noise figure, capacitive degeneration requires less dc power than does resistive degeneration.

An important concern in using capacitive degeneration is the amplification of noise components beyond the band of interest, in particular those due to Q_1 and Q_2 in Figure 1. Illustrated in Figure 2 for a local oscillator (LO) signal with 50% duty cycle, this effect manifests itself when amplified noise in the vicinity of $3\omega_{LO}$, $5\omega_{LO}$, etc., is downconverted, thereby increasing the noise contributed by Q_1 and Q_2.

To lower the supply voltage, capacitive coupling is used between the input and the mixing stages, allowing each stage to operate from $V_{CC,min}=V_{BE}+V_{IEE}$, where V_{IEE} is the voltage headroom consumed by each current source (Figure 1). (If the voltage drop across R_1-R_4 does not exceed approximately 400 mV, the base voltage of Q_1-Q_4 can be close to V_{CC}.) The low-pass filter consisting of R_3, R_4, and C_3 suppresses high-frequency components that would otherwise create intermodulation products in the following amplifier.

Since all the current sources in the circuit of Figure 1 contribute to the overall noise figure, it is important to minimize their output current noise. Figure 3 compares the total noise current per unit bandwidth of bipolar and MOS current sources, indicating that for a 600mV headroom the MOS current source exhibits three times less noise than the bipolar counterpart.

As mentioned above, capacitive degeneration amplifies high-frequency noise components. To resolve this issue, the value of the coupling capacitors C_1 and C_2 is chosen such that their bottom-plate parasitic capacitance (placed at nodes X and Y) forms a low-pass filter having a cutoff frequency of approximately 1GHz. Consequently, as with the standard Gilbert cell, noise components in the vicinity of $3\omega_{LO}$, $5\omega_{LO}$, etc., experience no net gain and hence contribute little to the noise figure.

Due to the limited voltage drop across R_3 and R_4, the mixer core of Figure 1 suffers from a few dB of conversion loss, mandating some post-amplification so as to reduce the noise contribution of the following circuits. In the post-amplifier, both noise and linearity are critical, but capacitive degeneration cannot be used because the capacitor value required at the intermediate frequency (IF) is prohibitively large.

Shown in Figure 4, the post-amplifier includes a differential pair Q_1-Q_2, emitter followers Q_3-Q_4, and a capacitive feedback network C_{I1}-C_{I2} and C_{F1}-C_{F2}. This circuit has two advantages over a similar configuration using a resistive feedback network: it exhibits less thermal noise, and it can operate from a lower supply voltage. Note that in this circuit, no path from V_{CC} to ground includes more than one base-emitter junction, and hence the supply voltage can be as low as 1.5V.

To establish the bias current of Q_1 and Q_2, pMOS transistors M_1 and M_2 are added to the circuit. Since these devices generate the base current of the differential pair according to the common-mode level at node E, a stable operating point is reached where $|V_{GSP}|+I_{EE}R_E=V_{CC}$. As M_1 and M_2 have a small W/L and are biased at low current levels, they exhibit a small transconductance and hence low-noise current. For the values chosen in this design, the noise power due to M_1-M_2 is approximately three times less than that due to R_3-R_4. Also, since the impedance of the capacitors in Figure 4 is relatively small at intermediate frequencies greater than several tens of megahertz, the base current noise of Q_1 and Q_2 flows through a low impedance and hence has a negligible effect.

The mixer prototype in 1µm 20GHz BiCMOS has been tested in a TQFP package while operating from a 1.5V supply [2]. The circuit dissipates 8mW in the core and 7mW in the output amplifier.

The downconverted output spectrum is shown in Figure 5 when two tones at 900MHz and 901.3MHz with a power of -20dBm are mixed with an LO frequency of 892MHz. The circuit exhibits an input IP_3 of 3dBm and a noise figure of 15dB. The conversion gain is 4dB. Table 1 summarizes measured characteristics.

References:

[1] Tsukahara, T., M. Ishikawa, M. Muraguchi, "Si-Bipolar Direct-Conversion Quadrature Modulator," ISSCC Digest of Technical Papers, pp. 40-41, Feb., 1994.

[2] Sung, J., et al., "BEST2 - A high performance super self-aligned 3V/5V BiCMOS technology with extremely low parasitics for low-power mixed-signal applications," Proc. IEEE CICC, pp. 15-18, May, 1994.

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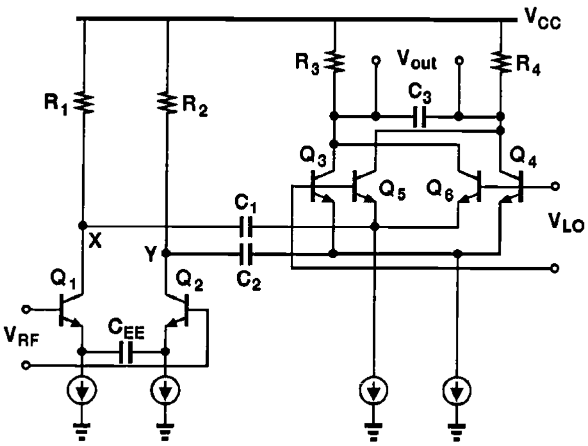


Figure 1: Mixer core.

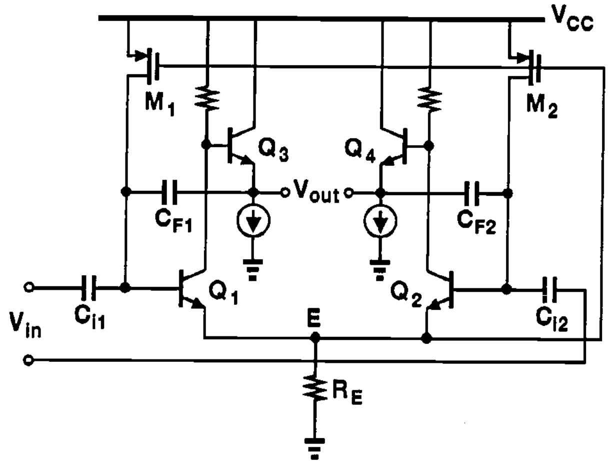


Figure 4: Post-amplifier.

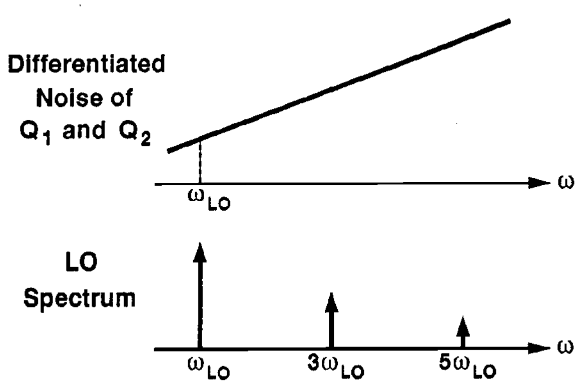


Figure 2: Effect of capacitive degeneration on noise.

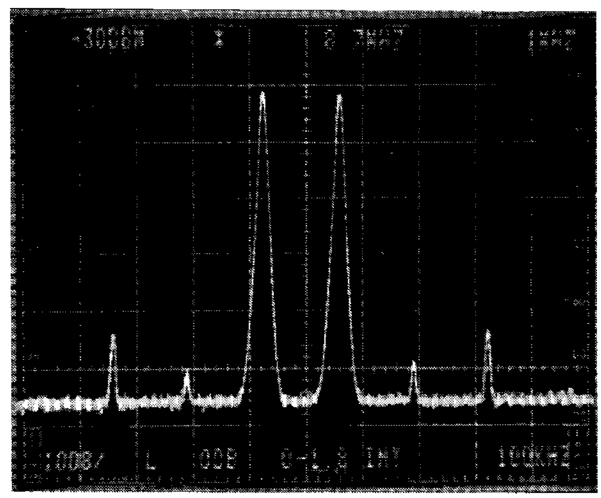
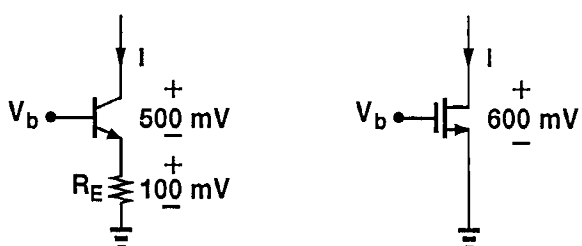


Figure 5: Output spectrum in a two-tone test (horiz. 1 MHz/div., vert. 10dB/div.).



$$\overline{I^2_{n,bi}} = 2kT\frac{1+2g_mR_E}{(1+g_mR_E)^2}g_m \approx 0.74kT\frac{I}{V_T}$$

$$\overline{I^2_{n,MOS}} = 2kT\frac{4}{3}\frac{I}{V_{GS}-V_{TH}} \approx 0.23kT\frac{I}{V_T}$$

Figure 3: Comparison of noise in bipolar and MOS current sources.

Noise figure	15dB
IIP_3	3dBm
Conversion gain	4dB
Supply voltage	1.5V
LO-RF feedthrough	-37dB
1dB compression point	-10dBm
Power dissipation	15mW
BiCMOS technology	20GHz 1.0μm

Table 1: Performance summary.