A 900-MHz CMOS Direct Conversion Receiver

Behzad Razavi
Formerly with: Hewlett-Packard Laboratories, Palo Alto, CA
Presently with: University of California, Los Angeles

This paper describes the design of a single-chip 900-MHz CMOS direct conversion receiver (DCR) fabricated in a digital 0.6-μm technology and operating from a 3-V supply.

Shown in Fig. 1 is the DCR architecture, consisting of a low-noise amplifier (LNA), quadrature mixers, simple low-pass filters (LPFs), a local oscillator (LO), a divide-by-two circuit, and baseband amplifiers, A_1. An important goal in the design has been to achieve a relatively high gain (approximately 35 dB) in the RF section so as to minimize the effect of the $1/f$ noise contributed by the baseband amplifiers. For this reason, passive mixers have been avoided even though they provide potentially higher linearity than do their active counterparts. Another goal has been to include the LO on the chip so as to obtain a realistic estimate of the leakage to the front end. The design incorporates on-chip inductors extensively to improve the performance.

Fig. 2 shows the implementation of the LNA and the quadrature mixers. The LNA is configured as a cascode stage, M_1 and M_2, with a 10-nH inductive load [1]. Providing high isolation between the output and the input, the cascode transistor not only improves the stability of the circuit but suppresses the LO leakage to the antenna as well. Utilizing large devices [$(W/L)_1 = 2000\ \mu$m$/0.6\ \mu$m)] and a relatively high bias current ($\approx$ 5 mA), the LNA achieves a noise figure of less than 2 dB and a voltage gain of approximately 20 dB. The inductive load provides a high gain while consuming negligible voltage headroom.

The use of an inductive load in the LNA prohibits the use of feedback to define the bias current and the output dc voltage of the circuit. While M_3 and I_b determine the bias current, the output voltage remains close to V_{DD}, a serious problem with respect to the bias point of the *following* stage—the mixer. This issue is resolved as explained below.

The mixer employs a single-balanced topology consisting of an input transistor M_4 and a switching pair M_5-M_6. In order to improve the linearity of the voltage-to-current conversion performed by the input stage, capacitor C_1 degenerates transistor M_4 at 900 MHz [2]. The current source defines the bias condition of M_4 with little dependence on its gate voltage. The problem of noise differentiation [2] is overcome by allowing L_2 and the bottom-plate parasitic capacitance of C_2 (C_p) to resonate in the vicinity of 900 MHz and shunt the noise current at higher harmonics of this frequency. Capacitor C_2 provides ac coupling, relaxing the limited voltage headrooom issues in the switching stage and also suppressing low-frequency beat signals that are generated if two input interferers experience *even-order* distortion in M_1, M_2, and M_4.

Even without the voltage headroom loss that would otherwise accompany M_4 in a simple mixer, the switching stage in Fig. 2 entails a number of trade-offs. To achieve a high conversion gain, M_5 and M_6 must remain in saturation and, more importantly, the voltage drop across R_1 and R_2 must be maximized. On the other hand, to minimize the noise current of M_7, the allowable drain-source voltage of this device must be as large as possible. In this design, the noise current of M_7 is suppressed in the band of interest (and higher harmonics thereof) through the use of the degenerating inductor L_3. This technique makes it possible to choose $V_{DS7} \approx 0.5$ V with negligible noise penalty, thereby allowing a large voltage drop across R_1 and R_2.

The output nodes of the mixer are loaded with on-chip capacitors to suppress high-frequency components, but channel-selection filtering is not included here.

Fig. 3 illustrates the LO and the divide-by-two circuit. Using a cross-coupled pair M_1-M_2 and 10-nH inductors L_1 and L_2, the oscillator operates at 1.8 GHz while directly driving the divider. The latter is configured as a master-slave flipflop driven differentially through M_3-M_4 and M_5-M_6. Proper sizing of the devices in each latch provides division speeds in excess of 2 GHz even with the relatively heavy capacitive loading imposed by the switching pairs in the quadrature mixers. Resistors R_5 and R_6 shift the high level of I_{LO} and Q_{LO} down to avoid driving the mixer switching pairs into the triode region.

The downconverted signal can be further processed by one of the three permutations depicted in Fig. 4 [3]. In Fig. 4(a), a low-pass filter suppresses out-of-channel interferers, allowing A_1 to be a nonlinear, high-gain amplifier and the analog-to-digital converter (ADC) to have a moderate dynamic range. (roughly 4 to 8 bits depending on the gain control in the RF domain and the type of modulation). However, the low-pass filter design entails severe noise-linearity-power tradeoffs. The second permutation, shown in Figure 4(b), relaxes the LPF noise requirements while demanding a higher performance in the amplifier. The difficulty here is that the signals are still quite small and the interferers quite large. Thus, A_1 must exhibit both low noise and high linearity. The present design is intended for permutations in Figs. 4(b) and (c).

Shown in Fig. 5 is the implementation of the baseband amplifier, consisting of a degenerated differential pair M_1-M_2 and load devices R_1-R_2 and M_3-M_4. Since high linearity requires a large $I_S R_S$, the maximum voltage gain with a 3-V supply is quite limited. To resolve this issue, the PMOS current sources have been added so as to provide about 75% of the drain current of M_1 and M_2, thereby allowing a large value for R_1 and R_2 and hence a high gain in the stage.

The linearity of the baseband amplifier is limited by both the nonlinear characteristics of M_1-M_2 and the nonlinear *output impedance* of M_3-M_4, even though all the transistors are in saturation. For this reason, the length of M_3-M_4 has been increased to 4 μm. To reduce the $1/f$ noise, wide transistors have been used: $W_{1,2} = 2000\ \mu$m, $W_{3,4} = 1600\ \mu$m.

The complete receiver has been fabricated in a 0.6-μm digital CMOS technology. The inductors are implemented as a stack of two spiral structures made of the second and third metal layers

with no additional wafer processing steps. Table 1 summarizes the preliminary measured performance of the overall receiver and Fig. 6 shows the LO divided output spectrum.

REFERENCES

[1] D. K. Shaeffer and T. H. Lee, "A 1.5 V 1.5 GHz CMOS Low Noise Amplifier," *VLSI Symp. Dig. Tech. Papers*, pp. 32-33, June 1996.

[2] B. Razavi, "A 1.5-V 900-MHz Downconversion Mixer," *ISSCC Dig. Tech. Papers*, pp. 48-49 , Feb. 1996.

[3] B. Razavi, "Design Considerations for Direct-Conversion Receivers," to be published in *IEEE Trans. Circuits and Systems II*, May 1997.

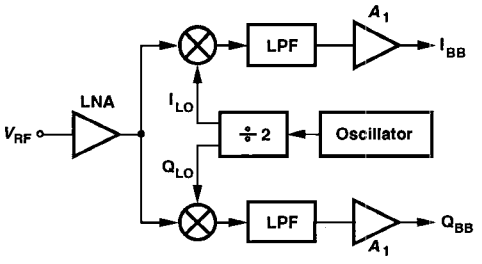

Fig. 1. Receiver architecture.

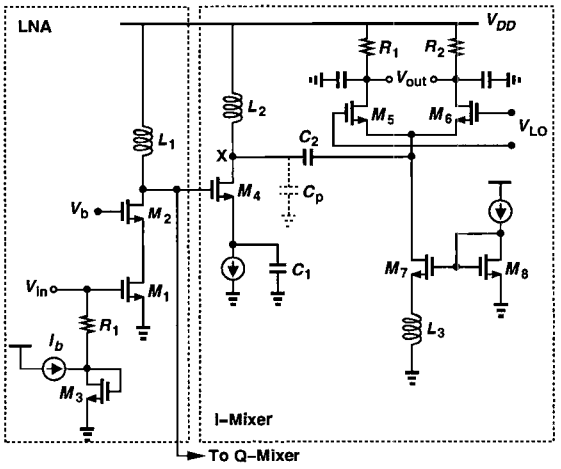

Fig. 2. LNA/mixer implementation.

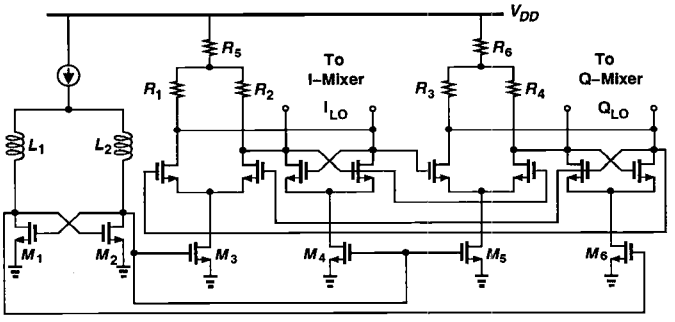

Fig. 3. LO/divider circuit.

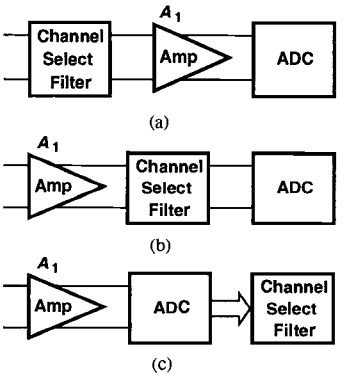

Fig. 4. Baseband processing.

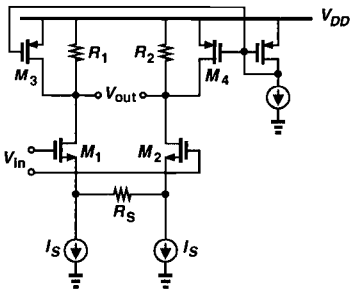

Fig. 5. Baseband amplifier.

Noise Figure	**4 dB**
IIP_3	**–20 dBm**
IIP_2	**+10 dBm**
LO Leakage	**–65 dBm**
LO Phase Noise	**–90 dBc/Hz @100 kHz offset**
Voltage Gain	**55 dB**
Power Dissipation	**90 mW**
Supply Voltage	**3 V**
Technology	**0.6–μm CMOS**

Table 1. Measured performance.

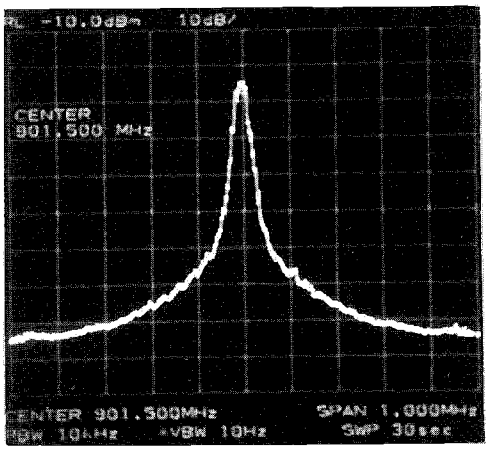

Fig. 6. LO divided output spectrum. (Horiz., 100 kHz/div.;Vert. 10 dB/div.; Resolution bandwidth, 10 kHz.)