A 19-GHz PLL with 20.3-fs Jitter

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Abstract

A PLL samples both the rising and falling edges of the reference clock and employs a new retiming method in the feedback divider. Fabricated in 28-nm CMOS technology, the prototype achieves an rms jitter of 20.3 fs from 10 kHz to 100 MHz with a spur of -66 dBc while consuming 12 mW. **Keywords: phase-locked loop (PLL), double-sampling phase detector, voltage-controlled oscillator (VCO)**.

The problem of clock generation with low jitter assumes new dimensions as communication systems seek higher performance. A number of PLLs achieving sub-60-fs jitter values have been reported [1-4]. This paper presents a 12-mW PLL realized in 28-nm CMOS technology that incorporates a number of new techniques to reduce the jitter to 20.3 fs_{rms}.

For a jitter approaching 20 fs, the contribution of every component becomes critical. Thus, we (1) abandon circuits such as PFDs and charge pumps for their excessive noise, and (2) identify the functions that are fundamentally necessary and whose phase noise is inevitably significant. As shown in Fig. 1, the reference oscillator, the reference buffer (RBUF), and the VCO fall under this category. The jitter contributed by RBUF enters the picture because the reference oscillator's output suffers from slow transitions. Denoting the total phase noise at the output of RBUF by S_{REF}, we recognize from the spectra shown in Fig. 1 that the PLL bandwidth, f_1, must be chosen so as to minimize the total integrated jitter.

If the free-running VCO phase noise is modeled as α/f^2, it can be shown that the optimum bandwidth, $f_{1,opt}$, and the minimum output jitter, $\sigma^2_{j,min}$, are approximately given by the expressions shown in Fig. 1. These equations assume negligible flicker noise in the three critical blocks.

Based on the foregoing observations, we propose the PLL architecture shown in Fig. 2. The circuit consists of RBUF, a phase detector (PD), a loop filter, a VCO, and a feedback divider. We wish to make negligible the jitter contributed by the PD, the Gm stage and the divider chain.

The PD plays a central role in our architecture. Driven by nonoverlapping phases ϕ_1 and ϕ_2, it is a differential, double-sampling version of that in [5] and provides crucial benefits. First, the relatively fast transitions in V_X confer a high gain to the PD, suppressing the Gm and kT/C noise. Second, the master-slave sampling action created by ϕ_1 and ϕ_2 leads to a wide capture range [5], obviating the need for a PFD/CP circuit or a frequency-locked loop. Third, differential operation doubles the PD gain. As a result, the kT/C noise components arising from the four switches are divided by a factor of 4 when referred to the PD input, offering a 3-dB reduction in the PD's phase noise.

The most remarkable advantage of the double-sampling PD, however, derives from its ability to reduce the jitter contributed by the (external) crystal oscillator and RBUF. This point is illustrated in Fig. 3. We note that if the rising edge of V_X is displaced by a random amount, Δt_1, then V_3 changes by $\Delta V_3 = (2\pi\Delta t_1/T_{REF}) \cdot K_{PD}$, where T_{REF} is the reference period and K_{PD} is the PD gain. Similarly, a displacement of Δt_2 in the falling edge of V_X translates to a change of $\Delta V_4 = (2\pi\Delta t_2/T_{REF}) \cdot K_{PD}$ in V_4. These random changes are combined by the Gm stage in Fig. 1. Thus, if V_X carries white phase noise and hence Δt_1 and Δt_2 are uncorrelated, the combining action in essence averages the jitter of the rising and falling edges, offering a 3-dB reduction. In view of the PLL bandwidth of about 10 MHz, we observe that the proposed PD lowers the in-band noise by nearly 3 dB.

The double-sampling function of the PD demands that the duty cycle of V_X remain around 50%. According to simulations, a range of 49.5% to 50.5% is acceptable. The duty cycle correction circuit in Fig. 2 serves this purpose.

The feedback path in Fig. 2 can potentially raise the jitter as well. Employing a C^2MOS topology and drawing 1.4 mW, the $\div 2$ stage contributes negligibly, but the remaining chain does not. Two options emerge here. If the divider is omitted through the use of subsampling, a narrow-pulse generator is typically inserted in the reference path [1,2], which, according to our simulation, adds 5 to 10 fs of jitter. Alternatively, a retiming flipflop can be interposed between the divider and the PD to remove the former's jitter, but it may experience metastability. We propose a programmable divider that successively removes the excess delay and phase noise as the signal propagates through the chain, ensuring that excess delay is maintained below 30 ps and hence metastability is avoided. Fig. 4 depicts the $\div N$ circuit implementation. In a manner similar to [6], we employ a cascade of $\div 2/\div 3$ stages, but we also insert flipflops FF_0 - FF_2. We observe that FF_2 retimes CK_5 under the command of CK_2. Thus, the excess delays of Div_a, Div_b and Div_c are removed. Similarly, FF_1 eliminates those of Div_d and FF_2, and finally, FF_0 removes those of Div_e and FF_1. It follows that ϕ_1 carries only the phase noise of CK_{in} and FF_0. This circuit provides a divide ratio from 32 to 62.

The nonoverlap time between ϕ_1 and ϕ_2 in Fig. 2 is necessary to avoid transparency in the master-slave sampling stages; otherwise, V_{cont} experiences substantial ripple. However, the nonoverlap generator also contributes jitter, a critical issue with respect to ϕ_1 and $\overline{\phi_1}$, as they are responsible for phase comparison with V_X. We must therefore avoid passing ϕ_1 and $\overline{\phi_1}$ through additional stages and yet generate ϕ_2 and $\overline{\phi_2}$. This is accomplished by the lower section in Fig. 4, where three latches, L_1 – L_3, and a delay stage, ΔT, produce a signal ϕ_0, which is then inverted and ANDed with ϕ_1 and $\overline{\phi_1}$ to provide ϕ_2 and $\overline{\phi_2}$, respectively. The nonoverlap time is given by $\Delta T \approx 50$ ps. Since ϕ_2 and $\overline{\phi_2}$ only transfer charge from C_1 and C_2 to C_3 and C_4, respectively, their phase noise is not critical.

The VCO in Fig. 2 is based on a complementary cross-coupled LC topology with inductive tail resonance. It consumes 7.2 mW.

The PLL die photograph in 28-nm technology is shown in Fig. 5(b) and has an active area of 315 µm x 350 µm, including decoupling capacitors. For ease of measurement, the output of the $\div 2$ circuit in Fig. 2 is used for the characterization. The

VCO frequency is slightly short of the target value of 20 GHz; hence the PLL is locked with a divide ratio of 76. The external 250-MHz reference is provided by Crystek's CRBSCS-01-250 crystal oscillator, which has a phase noise of -171.5dBc/Hz at 1-MHz offset. Fig. 5(a) shows the measured output spectrum, revealing a reference spur level of -72 dBc, which translates to -66 dBc at the VCO output.

Fig. 6 plots the measured phase noise at the output of the ÷2 circuit. The phase noise exhibits a plateau of about -133.3 dBc/Hz up to 10-MHz and falls to -155.9 dBc/Hz at 100-MHz offset; the phase noise at the VCO output is 6 dB higher. The jitter integrated from 10 kHz to 100 MHz is equal to 20.3 fs_{rms}. It is worth noting that the crystal oscillator and the on-chip buffer, RBUF, contribute about 40% of this jitter. RBUF is a thick-oxide inverter running from 1.2 V and consuming 1.3 mW.

Table I summarizes the performance of our prototype along with that of other sub-60fs PLLs. We note more than twofold reduction in the jitter and an improvement of 4.1 dB in FoM1.

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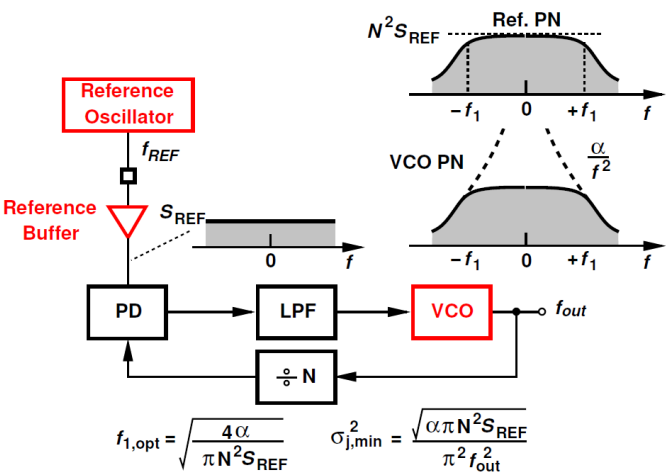


Fig. 1 Optimum PLL bandwidth and minimum integrated jitter.

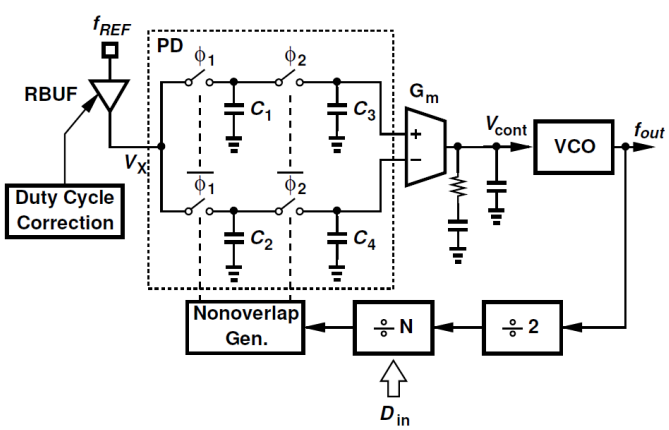


Fig. 2 Proposed PLL architecture.

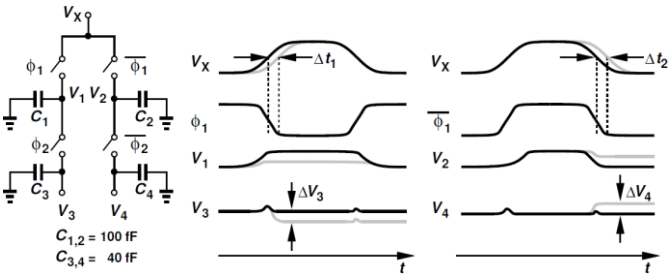


Fig. 3 Uncorrelated noise averaging by double-sampling PD.

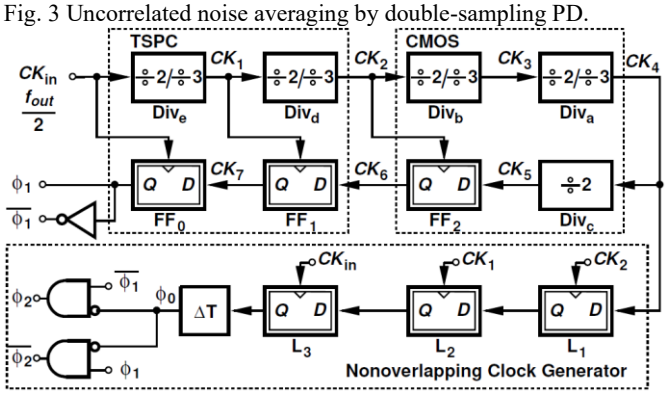
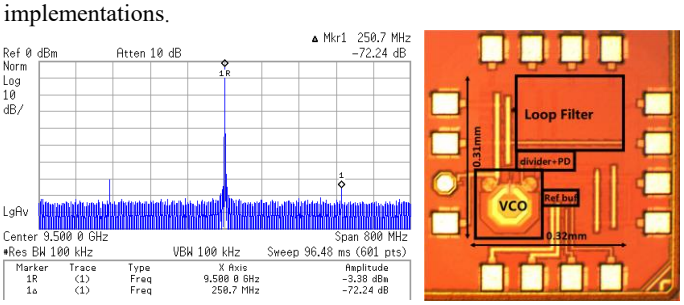


Fig. 4 Divider, retimer and nonoverlapping generator implementations.



(a) (b)

Fig. 5 (a) Measured spectrum and (b) die photo graph.

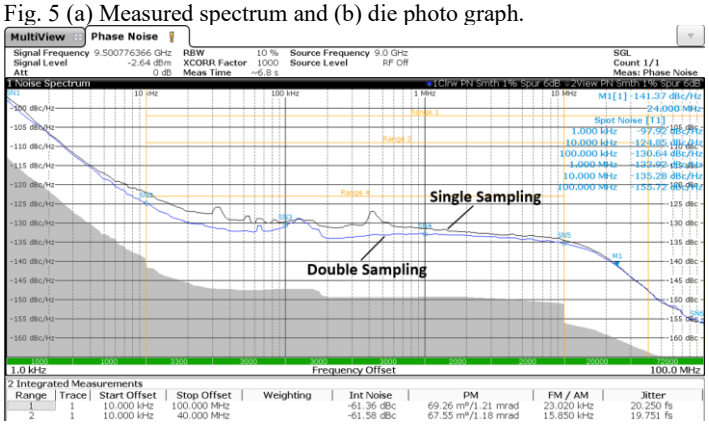


Fig. 6 Measured phase noise.

TABLE I Performance summary.

	[1]	[2]	[3]	[4]	This Work
Architecture	Sub-sampling PLL	Charge Sampling PLL	Single-Sampling PLL	Charge-pump based PLL	Double Sampling PLL
Ref. Freq.(MHz)	200	100	500	500	250
Freq. Range (GHz)	12 ~ 16	9.8 ~ 12.2	11.9 ~ 14.1	7.4 ~ 14	19
RMS Jitter (fs) Integ. range (MHz)	56.4 (0.001~100)	50.5 (0.001~100)	51.7 (0.001~100)	53.6 (0.01~10)	20.3 (0.01~100)
Ref. Spur (dBc)	-64.6	-65.7	-73.5	-75.5	-66
Power (mW)	7.2	5	18	45	12
Area (mm^2)	0.234	0.13	0.16	0.45	0.06
Tech. (nm)	40	40	28	16	28
FoM_1^* (dB)	-256.4	-258.9	-253.2	-248.9	-263
FoM_2^* (dB)	-247.9	-279.5	-267.2	-262.9	-281.9

$^*FoM_1 = 10\log_{10}[(\frac{Jitter}{1\ s})^2(\frac{Power}{1\ mW})]$ $^*FoM_2 = 10\log_{10}[(\frac{Jitter}{1\ s})^2(\frac{Power}{1\ mW})(\frac{f_{ref}}{f_{PLL}})]$