## 26.6 A 2.4GHz 34mW CMOS Transceiver for Frequency-Hopping and Direct-Sequence Applications

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The proliferation of 2.4GHz wireless standards such as Bluetooth and IEEE802.11b makes it desirable to realize low-power, compact transceivers capable of interoperability between frequency-hopping and direct-sequence systems. While Bluetooth requirements for receiver sensitivity and phase noise and transmitter linearity are relatively relaxed, those of IEEE802.11b are much more stringent. This paper describes a transceiver targeting both standards. The frequency planning and the design of all of the building blocks achieve low power dissipation for the overall system (while accommodating a GPS input in future implementations).

Figure 26.6.1 shows the transceiver architecture. The receiver employs two downconversion stages using a first local oscillator (LO) frequency of 1.6GHz and a second LO frequency of 800MHz, translating the input spectrum from 2.4GHz to an intermediate frequency (IF) of 800MHz and subsequently to zero. Similarly, the transmitter upconverts baseband quadrature waveforms to an 800MHz IF, and subsequently to 2.4GHz.

This architecture has several advantages over typical homodyne or heterodyne counterparts. First, the LO emission produced by the receiver is well out of the band. Second, the pulling of the LO by the power amplifier (PA) is negligible. Third, the system requires a single frequency synthesizer (but with a channel spacing of 2/3 MHz rather than 1MHz). Fourth, since the image and signal frequencies differ by 1.6GHz, on-chip partial image rejection becomes feasible. Fifth, since the downconversion to zero occurs with an LO frequency of 800MHz, the flicker noise of the mixers corrupts the signal to a lesser extent [1] and matching between the quadrature phases is more accurate. Finally, an LO frequency of 1.6GHz allows addition of a low-IF GPS path to the receiver.

The minimum supply voltage of the system is dictated by linearity and headroom issues in the downconversion mixers, the baseband section, and the prescaler (in the synthesizer) as well as the tuning range required of the VCO. For this reason, the supply is set at 2.5V and stacking techniques are employed to save power.

Figure 26.6.2a shows the LNA and the first downconversion mixer. This circuit has three advantages over conventional implementations. First, to reduce power consumption, the mixer is stacked on top of the LNA. Stacking is possible here because the IF is high and hence inductive (rather than resistive) loads can be used. Second, a double balanced topology is used to reduce the LO feedthrough. Third, to increase the image rejection of the circuit, the tanks consisting of $L_1$ and $C_1$ resonating at 800MHz are added. This tank degenerates $M_3$ at the image frequency and increases the image rejection of the circuit from 20dB to 40dB. This tank also attenuates the image noise of the LNA and mixer, thereby improving the noise figure of the mixer by roughly 3dB. Measurements on monopole antennas show that they provide another 25dB of rejection at 800MHz.

The choice of IF mixers is determined primarily by their linearity and power dissipation. As shown in Figure 26.6.2b, each mixer incorporates a double-balanced passive topology with two measures taken to improve the linearity. The transistors are degenerated by $C_1$ and $C_2$ and the divide-by-two circuit provides rail-to-rail LO swings to rapidly switch the devices. Since passive mixers cannot drive low-impedance resistive loads, they are followed by common-source pMOS stages. Despite their high power consumption (a total of 7.5mW), these amplifiers still limit receiver linearity.

Shown in Figure 26.6.3, the transmitter utilizes passive mixers in the first upconversion to achieve low power dissipation and higher linearity. The upconverted voltages are then converted to current (by $M_1$-$M_2$ and $M_3$-$M_4$) and multiplied by the 1.6GHz LO. The 2.4GHz signal is subsequently applied to the PA. The PA consists of a driver and an output stage, tapered in device size to deliver 0dBm to a 50Ω load. The driver is stacked on top of the output stage to reduce the power dissipation. Stacking also limits the maximum drain-source voltage of $M_1$ and $M_2$ to <2.5V.

To deliver 0dBm, the peak-to-peak output current must exceed 12.5mA even if linearity is not important. Since the voltage swing at node X can be larger than the required swing at the load, an on-chip matching network consisting of $C_1$ and $C_2$ along with the bond wire inductance $L_b$ boosts the output current. As a result, the PA delivers 0dBm with 3mA supply current while providing reasonable linearity.

This work introduces a phase-locked loop (PLL) synthesizer architecture that potentially achieves low output spurs. As shown in Figure 26.6.4a, if the divider in a type II PLL is followed by a voltage-controlled delay line (VCDL) with a sensitivity $K_D$, then the open-loop transfer function is given by $I_{CP}/(2\pi)\,[1/(sC_1)]\,(K_{vco}/(Ns)+K_D)$, where $I_{CP}$ denotes the charge pump current. Thus, a stabilizing zero is obtained without adding a resistor in series with $C_1$, allowing a small ripple on the oscillator control voltage. This is in contrast to the design in Reference 2, where the delay line is placed at the input. In the actual synthesizer, the controls of the VCO and the VCDL are separated. This isolates the oscillator control line from the kickback noise produced by the VCDL as the divided signal propagates through it. The phase noise of VCDL is removed by a retiming flipflop clocked by the VCO. The prescaler shown in Figure 26.6.4b uses only NOR flipflops to avoid level shifts and consumes only 1.25mW.

The transceiver is fabricated in a 0.25μm CMOS technology. Figure 26.6.5 shows die micrographs. Figure 26.6.6 summarizes measured system performance. The receiver achieves 3.9dB measured noise figure with 41dB image rejection. Receiver $IIP_3$ (limited by the baseband amplifiers) is -17.5dBm. However, since the noise figure of the receiver is lower than the values required by Bluetooth and IEEE802.11b, it can be traded for linearity. In fact, measurements indicate that if the gate voltage of $M_2$ in the LNA is lowered, the $IIP_3$ and noise figure rise at roughly the same rate. The overall receiver consumes 18mW, which along with 13mW dissipated in the synthesizer, amounts to a total of 34mW (including low-pass filters) from a 2.5V supply.

The transmitter delivers 0dBm with all unwanted components 30dB below the desired signal and a power consumption of 16mW. Figure 26.6.7 shows the output spectrum of the synthesizer at 1.66GHz. The spurs at 666.7kHz offset are 63dB below the carrier and the phase noise at 1MHz offset is approximately -110dBc/Hz. The low spur levels suggest that the synthesizer architecture is well suited to RF applications.

*Acknowledgment:*
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*References:*

[1] H. Darabi and A. Abidi, "Noise in RF CMOS Mixers: A Simple Physical Model," IEEE JSSC, vol. 35, pp. 15-25, Jan. 2000.
[2] T. H. Lee and J. F. Bulzacchelli, "A 155MHz Clock Recovery Delay- and Phase-Locked Loop," IEEE JSSC, pp. 1736-1746, Dec. 1992.


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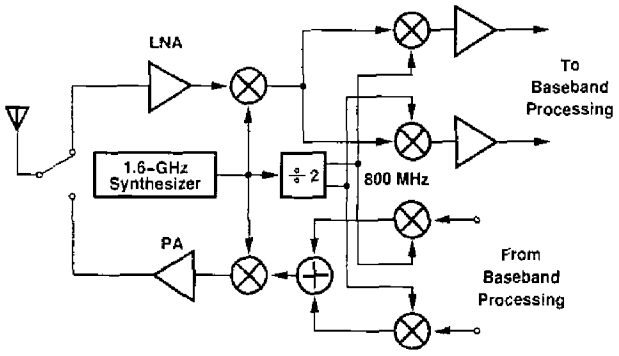


Figure 26.6.1: Transceiver architecture.

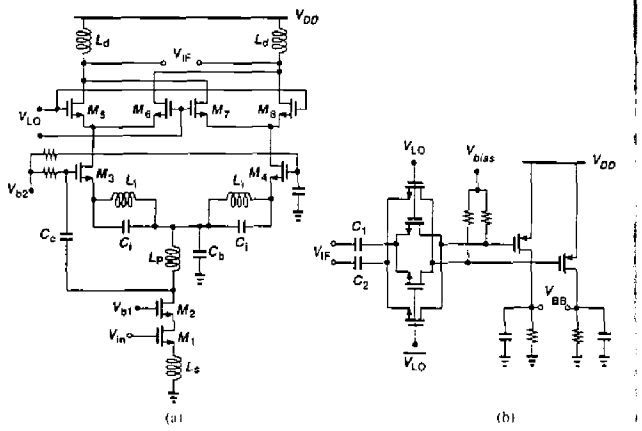


Figure 26.6.2: Receiver circuit (a) RF front-end, (b) IF mixer and amplifiers.

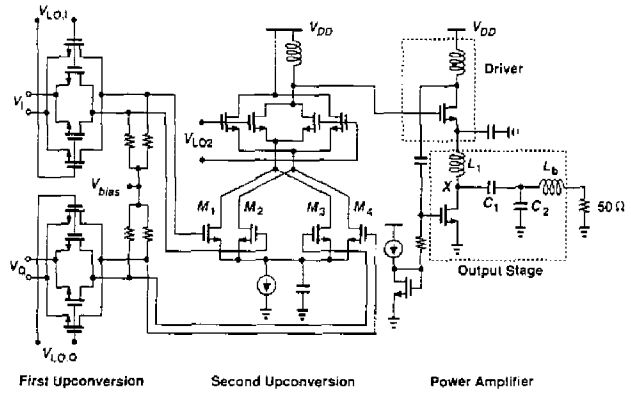


Figure 26.6.3: Transmitter circuit.

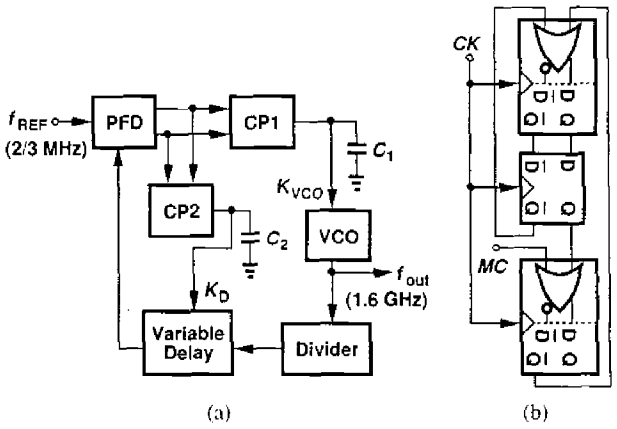


Figure 26.6.4: (a) Synthesizer architecture, (b) divider prescaler.

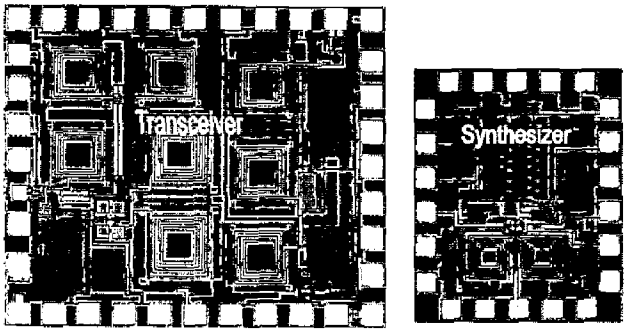


Figure 26.6.5: Die micrographs.

| | | | |
|---|---|---|---|
| Receiver | | Transmitter | |
| Noise Figure | 3.9 dB | Output Power | 0 dBm |
| \|S11\| | −12 dB | Sidebands | −30 dBc |
| IIP3 | −17.6 dBm | Power Dissipation | |
| Image Rejection | 41 dB | LNA & Mixers | 6.25 mW |
| Voltage Gain | 40 dB | Divider | 4.25 mW |
| Blocking | −28 dBm | Baseband Amps | 7.5 mW |
| Synthesizer | | Synthesizer | 13 mW |
| Frequency | 1.6 GHz | Total Receiver | 34 mW |
| Channel Spacing | 666.7 kHz | Upconverters & PA | 12 mW |
| Sidebands | −63 dBc | Supply Voltage | 2.5 V |
| Phase Noise @ 1 MHz Offset | −110 dBc/Hz | Technology | 0.25-μm CMOS |

Figure 26.6.6: Measured system performance.

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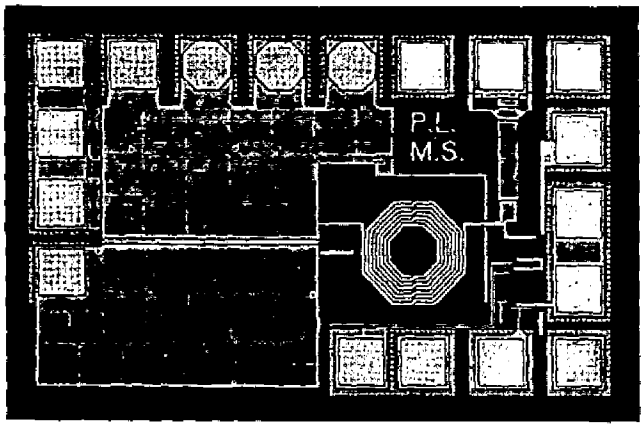


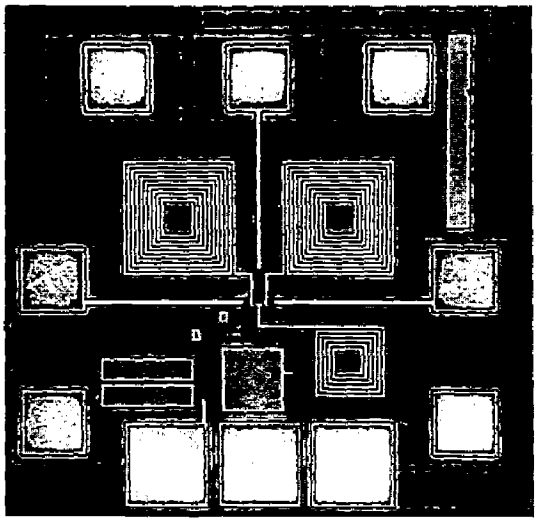

Figure 26.2.7.: LNA micrograph.

| | | | |
|---|---|---|---|
| Temperature | -34°C | 27°C | 85°C |
| Conversion Gain | 14.7dB | 15.0dB | 15.4dB |
| Noise Figure (SSB) | 8.6dB | 9.5dB | 9.6dB |
| IIP3 | -6.3dBm | -5.0dBm | -4.9dBm |
| Current Consumption | 13mA | 15mA | 17mA |
| 3-dB Bandwidth | | 600MHz | |
| Supply Voltage | 2.7V | 2.7V | 2.7V |

Figure 26.4.7: Summary of measured results.

9GHz ILFD.

19GHz ILFD.



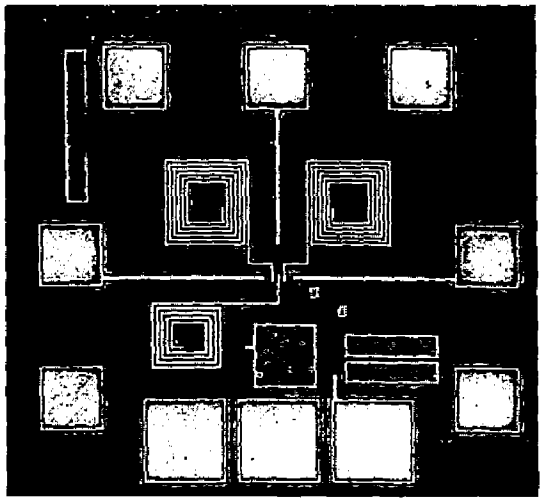


Figure 26.3.7: Chip micrographs.

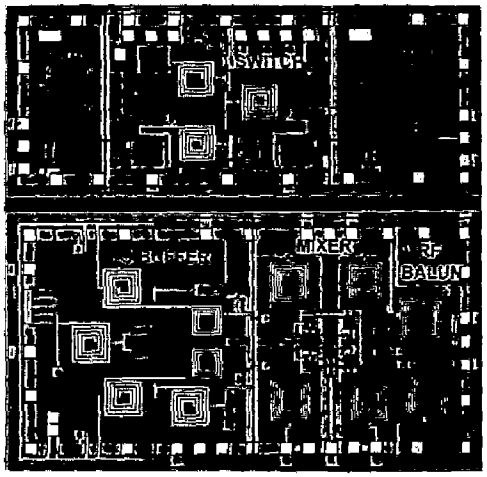



Figure 26.5.6: Micrograph of the integrated base station RF receiver.

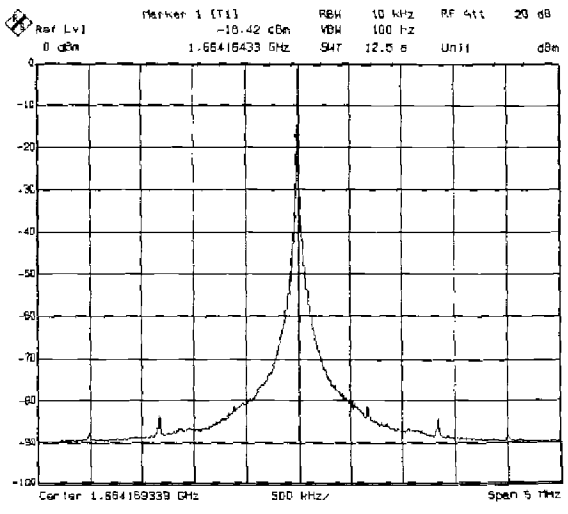



Figure 26.6.7: Synthesizer output spectrum.