Stacked Inductors and 1-to-2 Transformers in CMOS Technology[1]

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Abstract

A modification of stacked spiral inductors increases the self-resonance frequency by 100% with no additional processing steps, yielding values of 5 nH to 266 nH and self-resonance frequencies of 11.2 GHz to 0.5 GHz. Closed-form expressions predicting the self-resonance frequency with less than 5% error have also been developed. A 1-to-2 transformer consisting of 3 stacked spirals achieves a voltage gain of 1.8 at 2.5 GHz. The structures have been fabricated in standard CMOS technologies with four and five metal layers.

I. Introduction

Monolithic inductors have found extensive usage in RF CMOS circuits. Despite their relatively low quality factor, Q, such inductors still prove useful in providing gain with minimal voltage headroom and operating as resonators in oscillators. Monolithic transformers have also appeared in CMOS technology [1], allowing new circuit configurations. This paper presents a modification of stacked inductors that increases the self-resonance frequency, f_{SR}, by as much as 100%, a result predicted by a closed-form expression that has been developed for f_{SR}. A transformer structure is also introduced that achieves a nominal voltage or current gain of 2.

II. Stacked Inductors

In addition to the Q, the maximum value of inductance that can be utilized in a circuit is also important. As a tuned load, an inductor with a value L and a quality factor Q exhibits an equivalent parallel resistance of $R_P = Q.L\omega$ at resonance. Thus, to maximize R_P, the product of Q and L must be maximized. Similarly, to increase the tuning range of an oscillator, the f_{SR} of the inductor must be maximized. Simulations indicate that the inductor modification introduced in this paper increases the tuning range of a 900-MHz CMOS voltage-controlled from 4.2% to 23% for a 2x varactor capacitance range.

Since the Q of spiral inductors in CMOS technology is quite limited, it is reasonable to seek methods of achieving high inductance values with high self-resonance frequencies and a moderate silicon area. A candidate is the stacked structure of Fig. 1(a) [2], where the top and bottom layers are made of metal 5 (M_5) and metal 4 (M_4), respectively. In such a structure, owing to the strong mutual coupling between the layers, the total inductance is increased by a nominal factor of n^2, where n is the number of the layers.

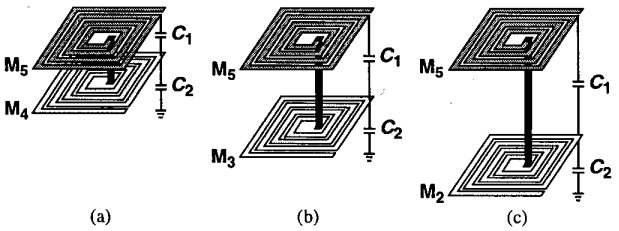

Fig. 1. Two-layer stacked inductor modification.

The f_{SR} of the stacked inductor of Fig. 1(a) is limited by the interlayer capacitance, C_1, and bottom-layer capacitance, C_2. Note that $f_{SR} = (2\pi\sqrt{L_{tot}C_{eq}})^{-1}$, where L_{tot} and C_{eq} are the total inductance and the equivalent capacitance of the structure, respectively. As proved in the Appendix,

$$C_{eq} = \frac{1}{12}(4C_1 + C_2) \qquad (1)$$

for a two-layer inductor. This expression reveals that the interlayer capacitance impacts the resonance frequency four times as much as the bottom-layer capacitance. Thus, if C_1 is reduced, C_{eq} may decrease substantially even if C_2 increases slightly.

The above observation suggests that C_{eq} can be reduced by moving the bottom spiral farther down, i.e., using metal 3 rather than metal 4 [Fig. 1(b)]. In a typical CMOS technology with five metal layers, $C_{M_5-M_4} \cong 40$ aF/μm^2 and $C_{M_4-sub} \cong 6$ aF/μm^2, whereas $C_{M_5-M_3} \cong 14$ aF/μm^2 and $C_{M_3-sub} \cong 9$ aF/μm^2. It follows that for the structure of Fig. 1(a), $C_{eq,a} \approx 14$ aF/μm^2, whereas for Fig. 1(b), $C_{eq,b} \approx 5.4$ aF/μm^2, an almost three-fold reduction.

Equation (1) proves very useful in estimating the performance of various stack combinations. For example, it predicts that the structure of Fig. 1(c) has an equivalent capacitance $C_{eq,c} \approx 4$ aF/μm^2 because $C_{M_5-M_2} \cong 9$ aF/μm^2 and $C_{M_2-sub} \cong 12$ aF/μm^2. In other words, the self-resonance frequency of the inductor in Fig. 1(c) is almost twice that of the inductor in Fig. 1(a).

Note that the value of the inductance remains relatively constant because the lateral dimensions are nearly two orders of magnitude greater than the vertical dimensions. This is verified by measurements as well.

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The idea of moving stacked spirals away from each other so as to increase f_{SR} can be applied to multiple layers as well. For n stacked layers, it is shown in the Appendix that

$$C_{eq} = \frac{1}{3n^2}(4\sum_{i=1}^{n-1} C_i + C_n), \qquad (2)$$

where $C_1, \cdots, C_{n-1}$ are the interlayer capacitances and C_n is the bottom-layer capacitance. Consequently, the structure of Fig. 2(a) can be modified as depicted in Fig. 2(b), thereby raising f_{SR} by 50%.

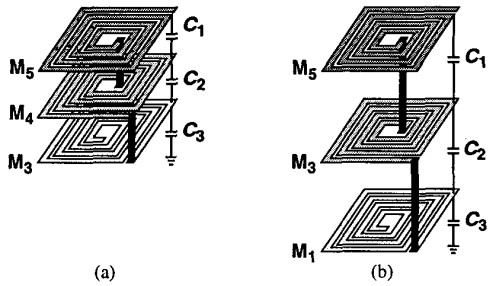


Fig. 2. Three-layer stacked inductor modification.

We should note that measurements indicate that Eq. (2) provides a reasonable approximation for f_{SR} of a single spiral as well, though the focus of the paper is on stacked spirals.

III. Transformers

Monolithic transformers producing voltage or current gain can serve as interstage elements if the signals do not travel off chip, i.e., if power gain is not important. Such transformers can also perform single-ended to differential and differential to single-ended conversion.

Figure 3(a) shows the 1-to-2 transformer structure. The primary is formed as a single spiral in metal 4 and the secondary as two series spirals in metal 3 and metal 5.

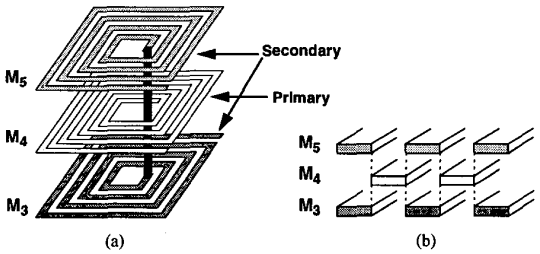


Fig. 3. Transformer Structure.

The performance of the transformer is determined by the inductance and series resistance of each spiral and the magnetic and capacitive coupling between the primary and the secondary. To minimize the capacitive coupling, the primary turns are offset with respect to the secondary turns as illustrated in Fig. 3(b). Thus, the capacitance arises only from the fringe electric field lines. The number of turns in each spiral also impacts the voltage (or current) gain at a desired frequency because it entails a trade-off between the series resistance and the amount of magnetic flux enclosed by the primary and the secondary. For single-ended to differential conversion, two of the structures in Fig. 3(a) can be cross-coupled so as to achieve the symmetry.

To design the transformer for specific requirements, a circuit model is necessary. Figure 4 illustrates one section of the distributed model developed for the 1-to-2 transformer. The

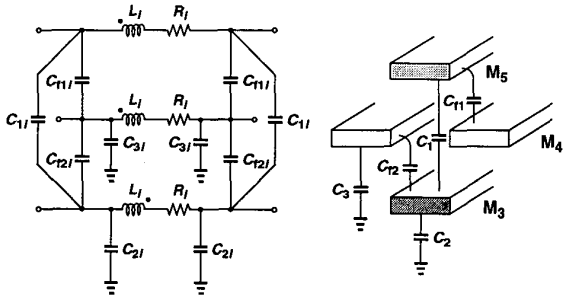


Fig. 4. Transformer model.

segments L_i and R_i represent a finite element of each spiral, C_f's denote the fringe capacitances, C_1 models the capacitance between M_5 and M_3, and C_2 and C_3 are the capacitances between the substrate and M_3 and M_4, respectively. Figure 5 depicts the simulated voltage gain of two transformers. The first transformer consists of eight-turn spirals with 7-μm wide metal lines while the second one is made of four-turn spirals with 9-μm wide metal lines.

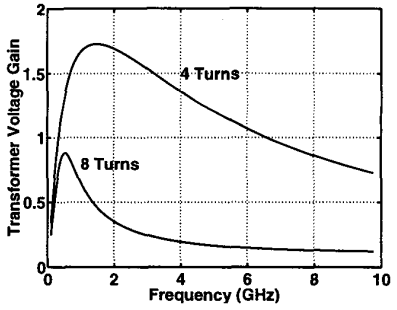


Fig. 5. Simulated voltage gain of the transformers.

Unlike stacked inductors, where the resonance frequency is not affected by the inductor loss, the voltage gain of the transformer depends on the quality factor of the spirals. In this simulation, a Q of three has been used for each winding. As Fig. 5 shows, for the eight-turn transformer, capacitive coupling between the spirals is so large that it does not allow the voltage gain to exceed one, while for the four-turn transformer we expect a gain of about 1.8 at about 2 GHz.

IV. Experimental Results

A large number of structures have been fabricated in a 0.4-μm four-metal-layer and a 0.25-μm five-metal-layer CMOS technology with no additional processing steps. A photograph of the 0.25-μm die is shown in Fig. 6. Calibration structures are also included to de-embed pad parasitics.

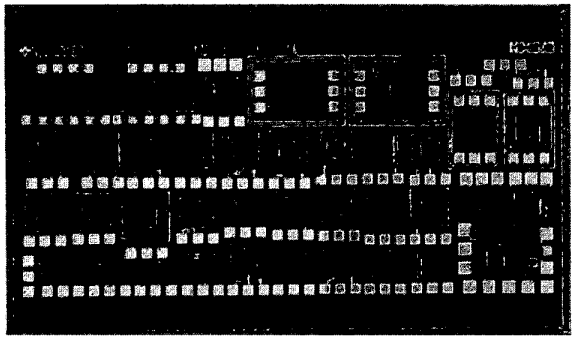


Fig. 6. Die photo.

Table 1 shows the measured characteristics of some inductors fabricated in the 0.25-μm process. The Q at self-resonance is approximately equal to 3. As expected from Fig. 1, inductors L_1, L_2, and L_3, with two layers of metal, demonstrate a steady increase in f_{SR} as the bottom spiral is moved away from the top one. Figure 7 shows the measured impedance of these inductors as a function of frequency, revealing a two fold increase in f_{SR}. For the three-layer inductors, L_4 and L_5 in Table 1, proper choice of metal layers can considerably increase the f_{SR}. To show how accuratly Eq. (2) predicts the f_{SR}, calculated values are included as well. The error is less than 5%.

Inductor	Metal Layers	L (nH)	Measured f_{SR} (GHz)	Calculated f_{SR} (GHz)
$L_1(240\mu m)^2$	5,4	45	0.92	0.96
$L_2(240\mu m)^2$	5,3	45	1.5	1.53
$L_3(240\mu m)^2$	5,2	45	1.8	1.79
$L_4(240\mu m)^2$	5,4,3	100	0.7	0.7
$L_5(240\mu m)^2$	5,3,1	100	1.0	1.0
$L_6(200\mu m)^2$	5,3,2	50	1.5	1.46
$L_7(200\mu m)^2$	5,2,1	48	1.5	1.54

Table 1. Measured inductors in 0.25-μm technology.

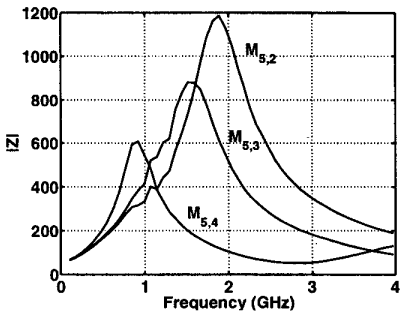


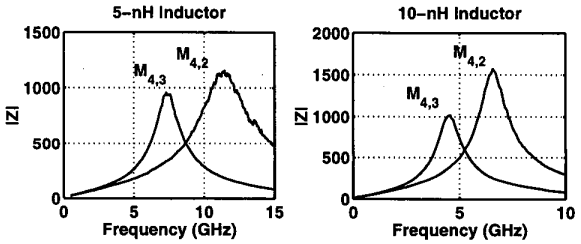
Fig. 7. Measured inductor characteristics.

Table 2 shows how adding the number of metal layers can increase the inductance value. In this table, all inductors have the same dimensions but incorporate different number of layers. Using five layers of metal yields an inductance value of 266 nH in an area of $(240\mu m)^2$. Such high values even raise the possibilty of integrating voltage regulators and dc-dc converters monolithically.

Inductor Size	Metal Layers	L (nH)	Measured f_{SR}(GHz)	Calculated f_{SR}(GHz)
$(240\mu m)^2$	5,4	45	0.92	0.96
$(240\mu m)^2$	5,4,3	100	0.7	0.7
$(240\mu m)^2$	5,4,3,2	180	0.55	0.58
$(240\mu m)^2$	5,4,3,2,1	266	0.47	0.49

Table 2. High-value inductors in 0.25-μm technology.

In Fig. 8, some other measured results for two pairs of 5-nH and 10-nH inductors in 0.4-μm technology (with four layers of metal) are shown. In this case, the self-resonance frequency increases by 50% with the proposed modification. The Q at self-resonance is between 3 and 5 for the four cases. Note that for the 5-nH inductor resonating at 11.2 GHz, the skin effect is quite significant. The data points also confirm the accuracy of the calculated f_{SR} from (2).



f_{SR} (GHz)	$M_{4,3}$ 5 nH	$M_{4,2}$ 5 nH	$M_{4,3}$ 10 nH	$M_{4,2}$ 10 nH
Measured	7.5	11.2	4.5	6.8
Calculated	7.8	11.7	4.6	6.8

Fig. 8. Measured inductors in 0.4-μm technology.

The 1-to-2 transformers of Section III have been fabricated in a 0.25-μm technology. Figure 9 plots the measured voltage gain as a function of frequency. The measured behavior is reasonably close to the simulation results using the disctributed model. The four-turn transformer achieves a voltage gain of 1.8 at 2.4 GHz. The plot also illustrates the effect of capacitive loading on the secondary (calculated using the measured S-parameters), suggesting that capacitances as high as 100 fF have negligible impact on the gain.

V. Appendix

To derive an expression for the equivalent capacitance, C_{eq}, of stacked inductors, a circuit model is necessary. Since the inductor loss does not affect the f_{SR}, the lossless distributed model shown in Fig. 10 can be used.

Finding the equivalent impedance of the simplified circuit of Fig. 10 still seems difficult. However, we can use the

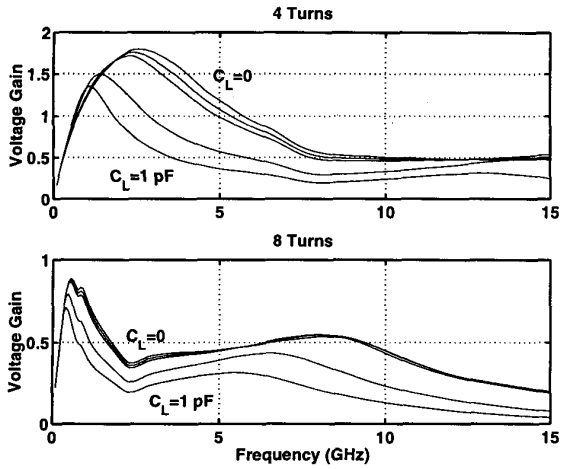


Fig. 9. Measured transformer voltage gain for C_L =0, 50 fF, 100 fF, 500 fF, 1 pF.

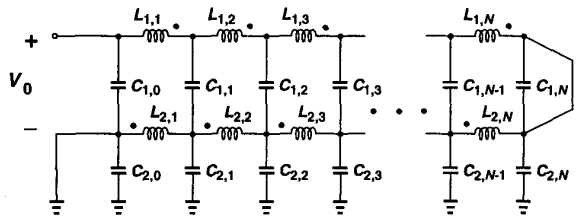


Fig. 10. Distributed model of two-layer inductor.

physical definition of resonance. The resonance frequency can be defined as the frequency at which the peak magnetic and electric energies are equal. To derive the electric energy stored in the capacitors, we first find the voltage profile across the distributed capacitance of the structure.

Assuming perfect coupling between every two inductors in Fig. 10, we express the voltage across each as:

$$V_{L,l,m} = \sum_{l=1}^{2} \sum_{m=1}^{N} j\omega I_{l,m} L_{l,m}, \tag{3}$$

where $I_{l,m}$ is the current through $L_{l,m}$ and N is the number of the sections in the distributed model. Equation (3) reveals that all inductors sustain equal voltages. Therefore, for a given applied voltage, V_0, we have

$$V_{L,l,m} = \frac{V_0}{2N}. \tag{4}$$

From (3) and (4), it follows that the voltage across the distributed capacitance C_1 varies with a constant slope from V_0 to 0 while for C_2, the voltage changes from 0 to $V_0/2$ (left to right).

Having determined the voltage variation, we write the electric energy stored in the mth element, $C_{1,m}$, as

$$E_{e,C_{1,m}} = \frac{1}{2} C_{1,m}[(V_0 - mV_{L,l,m}) - mV_{L,l,m}]^2. \tag{5}$$

The total electric energy in C_1 is therefore equal to

$$E_{e,C_1} = \frac{1}{2} \sum_{m=0}^{N} C_{1,m}(V_0 - 2mV_{L,l,m})^2. \tag{6}$$

Since $C_{1,m} = C_1/(N+1)$, if we substitute (4) in (6), define a new variable $x = m/N$, and let N go to infinity, (6) reduces to

$$E_{e,C_1} = \frac{1}{2} C_1 V_0^2 \int_0^1 (1-x)^2 dx = \frac{1}{2} \cdot \frac{C_1}{3} V_0^2. \tag{7}$$

The above equation states that if the voltage across a distributed capacitor changes linearly from zero to a maximum value V_0, then the equivalent capacitance is 1/3 of the total capacitance. Since C_2 sustains a maximum voltage of $V_0/2$, its electric energy is

$$E_{e,C_2} = \frac{1}{2} \cdot \frac{C_2}{3} \cdot (\frac{V_0}{2})^2 = \frac{1}{2} \cdot \frac{C_2}{12} V_0^2. \tag{8}$$

From (7) and (8), the total electric energy is

$$E_e = E_{e,C_1} + E_{e,C_2} = \frac{1}{2} \cdot \frac{4C_1 + C_2}{12} V_0^2, \tag{9}$$

yielding the expression in (1) for the equivalent capacitance.

The foregoing method can be applied to stacks of multiple spirals as well. For an inductor with n stacked spirals, (3) suggests that the voltage is equally divided between the spirals. Therefore, the maximum voltage for interlayer capacitances is $2V_0/n$ while for the bottom-layer capacitance it is V_0/n. Now, using the result of (7) and adding the electric energy of all layers, we have

$$E_e = \frac{1}{2} \sum_{i=1}^{n-1} \frac{C_i}{3} (\frac{2V_0}{n})^2 + \frac{1}{2} \cdot \frac{C_n}{3} (\frac{V_0}{n})^2 \tag{10}$$

$$= \frac{1}{2} \cdot \frac{4\sum_{i=1}^{n-1} C_i + C_n}{3n^2} V_0^2, \tag{11}$$

thus obtaining (2).

To derive the equivalent capacitance, we assumed that all inductors are perfectly coupled. However, the coupling between orthogonal segments of a spiral or different spirals is very small. Nonetheless, if we assume that the inductor elements that are on top of each other are strongly coupled, then they sustain equal voltages. Therefore, the total voltage is equally divided between the spirals and since each spiral is composed of a few groups of coupled inductors, the linear voltage profile is a good approximation.

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