Relation Between Delay Line Phase Noise and Ring Oscillator Phase Noise

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***Abstract*—The phase noise of a ring oscillator can be obtained by multiplying its open-loop phase noise by a simple shaping function. The shaping function is computed using first principles and is applicable to both flicker-noise-induced and white-noise-induced phase noise, leading to compact equations for ring oscillators. It is also shown that flicker noise upconversion in ring oscillators is primarily a function of the total gate capacitance and inevitable regardless of the risetime and falltime symmetry. Two oscillator prototypes fabricated in 65-nm CMOS technology verify the validity of the results.**

***Index Terms*—Flicker noise, inverter phase noise, jitter, oscillator phase noise, phase noise, white noise.**

I. Introduction

It has been recognized for more than two decades that delay lines exhibit less phase noise than ring oscillators do [1]. This advantage is intuitively explained by the lack of jitter accumulation in the former but has not been quantified analytically.

The phase noise in ring oscillators has been studied extensively [2]–[10]. In this paper, we offer an analysis that leads to a direct relation between the phase noise of delay lines and that of ring oscillators, allowing comparison of their performance for a given power dissipation and operation frequency. We begin with first principles and establish a unified relation for both white and $1/f$ noise sources. As a byproduct, our analysis also shows that the flicker-noise-induced phase noise is inversely proportional to the total gate capacitance present in a ring oscillator and relatively independent of the symmetry between rise and fall transitions. The proposed relation is experimentally verified on 9-stage and 19-stage prototypes fabricated in 65-nm CMOS technology.

Section II deals with the phase noise of delay lines, expressing their jitter as two impulse trains. Section III analyzes jitter accumulation in a ring oscillator and utilizes the results from Section II to arrive at the the proposed relation. Section IV derives some useful results, including compact phase noise equations, and Section V and VI, respectively, present simulation and experimental confirmations of the equations.

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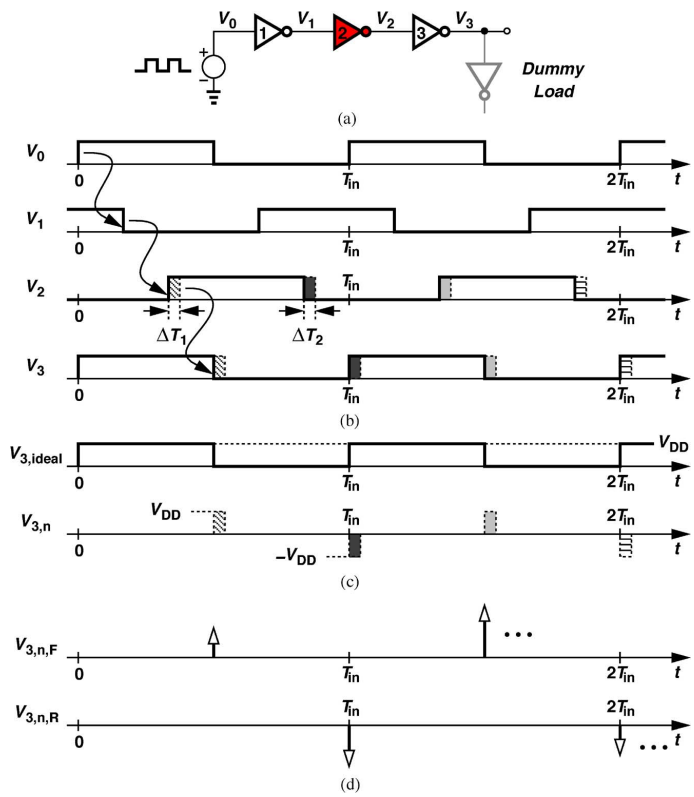


Fig. 1. (a) Three-stage delay line with only one noisy inverter, (b) node voltages in response to a frequency equal to the oscillation frequency of a three-stage ring oscillator, (c) decomposition of the output voltage to an ideal noiseless square wave and a noise waveform, and (d) approximation of the noise waveform in (c) to two uncorrelated weighted impulse trains.

II. Phase Noise of Delay Lines

Let us consider the chain of inverters shown in Fig. 1(a) as a representative delay line, with the dummy load added to ensure uniform delays. Since the inverters exhibit uncorrelated noise, the overall phase noise (as a power quantity) is equal to that of one multiplied by the number of stages (if they are identical). For our purposes, we tentatively assume that only the second inverter in Fig. 1(a) has noise. We also select the input frequency equal to the oscillation frequency of this chain as if it were reconfigured to become a ring oscillator, i.e., $f_{in} = 1/(6T_d)$, where T_d denotes the average gate delay. Thus, as V_0 propagates to V_3, it experiences three gate delays and the jitter of one inverter [Fig. 1(b)]. In other words, the falling edges of V_3 are aligned with the falling edges of V_0 but modulated by the second inverter's jitter.

The output of the third inverter in Fig. 1(a) can be decomposed into an ideal square wave and a train of narrow pulses

[11], [12] that occur every $3T_d = T_{in}/2$ seconds [Fig. 1(c)]. Since the jitters on the rising and falling edges arise from different noise sources and are uncorrelated [13], we denote them by $\sigma_R(t)$ and $\sigma_F(t)$, respectively. Now, $V_{3,n}$ in Fig. 1(c) itself can be approximated as the sum of a positive impulse train weighted by $\sigma_F(t)$ and a negative impulse train weighted by $\sigma_R(t)$ [Fig. 1(d)]:

$$\begin{aligned} V_{3,n}(t) &= V_{3,n,F}(t) + V_{3,n,R}(t) \\ &= \sum_{n=-\infty}^{\infty} \sigma_F \left[(2n+1)\frac{T_{in}}{2}\right] \delta \left[t-(2n+1)\frac{T_{in}}{2}\right] \\ &\quad - \sum_{n=-\infty}^{\infty} \sigma_R \left(2n\frac{T_{in}}{2}\right) \delta \left(t-2n\frac{T_{in}}{2}\right) \end{aligned} \quad (1)$$

With the aid of Fig. 1(d), we recognize that the phase noise of the chain is equal to the sum of the power spectral densities of $V_{3,n,F}$ and $V_{3,n,R}$ normalized to the power of the first harmonic of $V_{3,ideal}$ [13]. We derive the phase noise expression in Section IV.

III. Phase Noise of Ring Oscillators

The perspective described above for the phase noise of delay lines proves useful in the phase noise analysis of ring oscillators as well. Suppose the delay line of Fig. 1(a) is reconfigured to form a ring oscillator as shown in Fig. 2(a) (without the dummy load).

We perform a "gedankenexperiment" in which (1) the voltage source V_{in} applies a noiseless rising edge to the input of the first inverter at $t = 0^-$ and is disconnected from the circuit at $t = 0$, and (2) the second inverter produces jitter only once (i.e., a single time displacement) as this edge propagates through the chain and remains noiseless thereafter. Thus, the input rising edge arrives at V_3 with a delay equal to $3T_d$ plus the jitter of the second inverter, ΔT_1. As this edge circulates around the ring, it experiences no more jitter; i.e., all of the subsequent edges are simply displaced by a constant equal to ΔT_1. Fig. 2(b) illustrates this effect.

The output waveform obtained in the above experiment can be decomposed as shown in Fig. 2(c) and expressed as a single pulse of width ΔT_1, convolved with an alternating train of impulses, $g(t)$. Note that $g(t) = 0$ for $t < 0$. We can consider $g(t)$ as "carrier" for the time displacements.

We now repeat the above experiment while assuming that the second inverter is noisy at all times. The second time the oscillation edge passes through this inverter, the jitter causes one additional displacement, ΔT_2, as depicted by the dark shading in Fig. 2(d). The effect of this shift can be obtained by convolving a pulse of width ΔT_2 with $g(t)$ and adding the result to an ideal, noiseless waveform. Note that this calculation holds valid whether or not ΔT_1 and ΔT_2 are correlated.

The foregoing observations suggest that the ring oscillator output can be decomposed into an ideal square waveform and a noise component [Fig. 2(e)] given by

$$\begin{aligned} &V_{n,ring}(t) \\ &= \left\{ \sum_{n=-\infty}^{\infty} \sigma_R \left[(2n+1)\frac{T_{in}}{2}\right] \delta \left[t-(2n+1)\frac{T_{in}}{2}\right] \right\} * g(t) \\ &\quad - \left\{ \sum_{n=-\infty}^{\infty} \sigma_F \left(2n\frac{T_{in}}{2}\right) \delta \left(t-2n\frac{T_{in}}{2}\right) \right\} * g(t). \end{aligned} \quad (2)$$

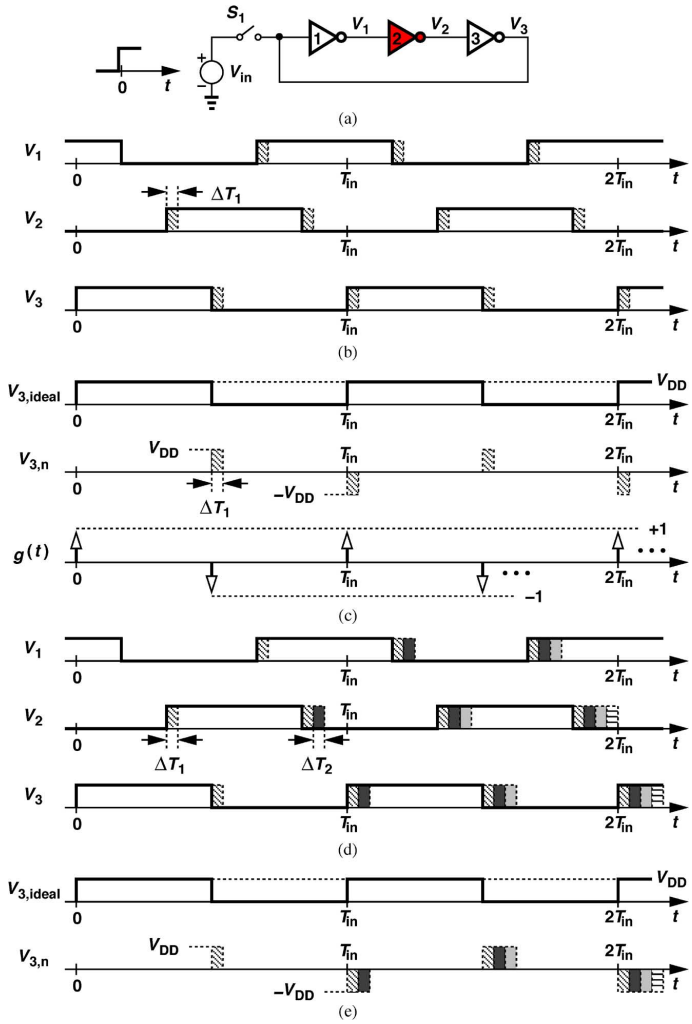


Fig. 2. (a) Three-stage ring oscillator retimed at $t = 0$ with only one noisy inverter, (b) jitter on all edges due to a single jitter event on V_2, (c) decomposition of V_3 in (b) to an ideal noiseless square wave and a noise waveform, with $g(t)$ serving as a "carrier," (d) jitter on edges when inverter #2 adds jitter on every transition, (e) decomposition of V_3 in (d) to an ideal noiseless square wave and a noise waveform.

From (1) and (2), it follows that the delay line phase noise, $S_{\Phi,DL}(f)$, and the ring oscillator phase noise, $S_{\Phi,ring}(f)$, are related as[1]

$$S_{\Phi,ring}(f) = S_{\Phi,DL}(f)\,|G(f)|^2 \quad (3)$$

where $|G(f)|^2$ denotes the spectrum of $g(t)$.

Equation (3) is a general result and merits a few remarks. First, (3) applies to the phase noise due to both white noise and flicker noise. Second, (3) holds for the phase noise arising from *all* of the devices in the delay line and the ring. Third, (3) is not limited to CMOS inverters and can be used for differential delay stages and rings as well.

To determine $|G(f)|^2$, we first write

$$g(t) = \left[\sum_{n=-\infty}^{\infty} \delta(t-nT_{in}) - \sum_{n=-\infty}^{\infty} \delta\left(t-nT_{in}-\frac{T_{in}}{2}\right) \right] u(t) \quad (4)$$

[1]Throughout this paper, all the spectra are two-sided, and the phase noise is denoted by S_Φ.

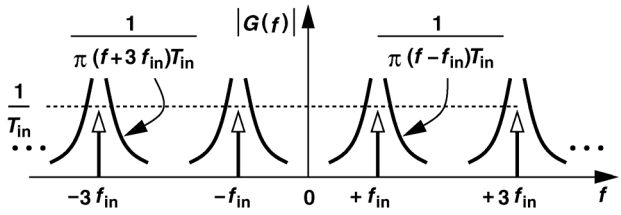


Fig. 3. Fourier transform of $g(t)$.

and hence

$$G(f) = \left[\frac{1}{T_{in}}(1 - e^{-j\pi f T_{in}}) \sum_{n=-\infty}^{\infty} \delta(f - nf_{in})\right] * \left[\frac{1}{j2\pi f} + \frac{1}{2}\delta(f)\right] \quad (5)$$

which simplifies to

$$G(f) = \left\{\frac{2}{T_{in}} \sum_{n=-\infty}^{\infty} \delta\left[f - (2n+1)f_{in}\right]\right\} * \left[\frac{1}{j2\pi f} + \frac{1}{2}\delta(f)\right]. \quad (6)$$

The unit step in (4) ensures the causality of jitter accumulation, i.e., the jitter generated at any edge is present for only subsequent edges. Fig. 3 plots the magnitude of $G(f)$, revealing how the delay line phase noise is shaped to produce the ring oscillator phase noise.

At an offset frequency of Δf with respect to the fundamental frequency, $f_{in} = 1/T_{in}$, we have

$$\begin{aligned} G(f_{in} + \Delta f) &= \frac{2}{T_{in}} \sum_{n=-\infty}^{\infty} \frac{1}{j2\pi(\Delta f + 2nf_{in})} \\ &= \frac{1}{j2\pi}\left\{\frac{2f_{in}}{\Delta f} + \sum_{n=1}^{\infty} \frac{\frac{\Delta f}{f_{in}}}{\left[\frac{\Delta f}{(2f_{in})}\right]^2 - n^2}\right\} \\ &= \frac{1}{j2\pi}\left[\pi \cot\left(\frac{\pi \Delta f}{2f_{in}}\right)\right]. \end{aligned} \quad (7)$$

Thus, (3) can be rewritten as

$$S_{\Phi,ring}(\Delta f) = S_{\Phi,DL}(\Delta f)\frac{1}{4}\cot^2\left(\frac{\pi \Delta f}{2f_{in}}\right). \quad (8)$$

For offset frequencies much less than f_{in}, we have $\cot^2[\pi\Delta f/(2f_{in})] \approx [2f_{in}/(\pi\Delta f)]^2$. Changing our notation from f_{in} to f_{osc}, we write

$$S_{\Phi,ring}(\Delta f) = S_{\Phi,DL}(\Delta f)\left(\frac{f_{osc}}{\pi \Delta f}\right)^2. \quad (9)$$

This simple, fundamental relation holds for phase noise due to both $1/f$ and white noise.

IV. Useful Insights

Equation (9) provides a multitude of interesting and useful insights into the phase noise behavior of ring oscillators. Of course, it confirms that white noise and flicker noise lead to $1/\Delta f^2$ and $1/\Delta f^3$ phase noise profiles because the corresponding delay line phase noise profiles are respectively flat and proportional to $1/\Delta f$ [13]. This section presents some other insights that may benefit the circuit designer.

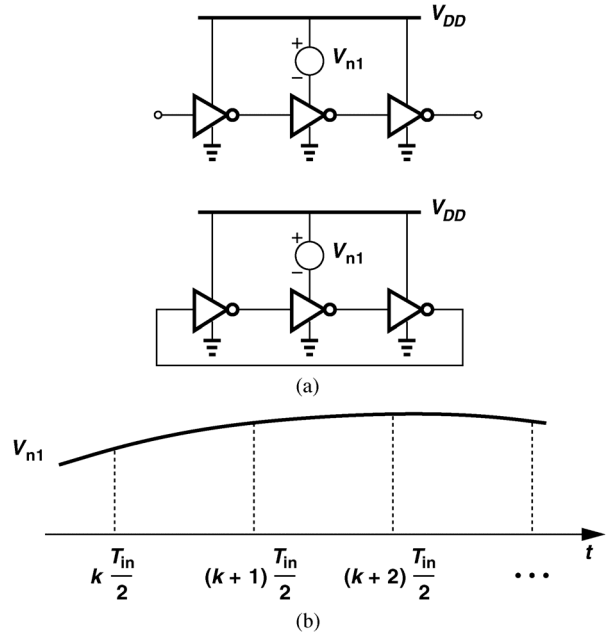


Fig. 4. (a) Delay line and ring oscillator with one equivalent noise source, V_{n1}, and (b) V_{n1} shown as a low-frequency component.

A. Comparison of Delay Lines and Ring Oscillators

Equation (9) indicates that conversion of a delay line to a ring oscillator shapes the phase noise by an $f_{osc}^2/(\pi\Delta f)^2$ function. Since Δf is usually much less than f_{osc}/π, we observe that $S_{\Phi,ring}(\Delta f) \gg S_{\Phi,DL}(\Delta f)$ for a given power dissipation and fundamental frequency. Why are low noise frequencies scaled by a greater factor? Consider the scenario depicted in Fig. 4(a), where one of the noise sources of the second inverter, V_{n1}, is explicitly shown and placed in series with V_{DD}; for example, V_{n1} represents the noise of the PMOS transistor in the inverter. Suppose V_{n1} varies at a rate much lower than the operation frequency, f_{in} [Fig. 4(b)]. We observe that the delay line simply experiences a relatively constant phase shift at $t = kT_{in}/2$, $t = (k+1)T_{in}/2$, etc., so long as V_{n1} changes negligibly. In the ring oscillator, on the other hand, the time displacements caused by V_{n1} at $t = kT_{in}/2$, $t = (k+1)T_{in}/2$, etc., continue to accumulate until V_{n1} changes polarity. The lower the frequency of V_{n1}, the longer and larger this accumulation is, producing the $1/\Delta f^2$ shaping function.

B. Compact Phase Noise Equations

The phase noise of an inverter is derived in [13] as

$$S_{\Phi,white} = \left\{\frac{\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f)\right\}_{NMOS} + \left\{\frac{\pi^2 \Delta T}{r_{edge}^2 C_L^2 T_{in}} S_I(f)\right\}_{PMOS} + \frac{2\pi^2}{r_{edge}^2 T_{in}}\frac{kT}{C_L}. \quad (10)$$

for white noise sources and as

$$S_{\Phi,1/f} = \left\{ \frac{\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{\frac{1}{f}}(f) \right\}_{NMOS} + \left\{ \frac{\pi^2 \Delta T^2}{r_{edge}^2 C_L^2 T_{in}^2} S_{\frac{1}{f}}(f) \right\}_{PMOS} \quad (11)$$

for flicker noise sources, where r_{edge} is the slew rate, C_L the load capacitance, T_{in} the input period, $S_I(f)$ the thermal noise current, $S_{1/f}(f)$ the flicker noise current, k the Boltzmann constant, T the absolute temperature, and ΔT the equivalent "on" time for each transistor [13].

In order to derive a compact expression for the delay line, we make three simplifying assumptions. (1) The equivalent on time, ΔT, is approximately equal to the gate delay, T_d. (2) The slew rate, r_{edge}, can be approximated as I_D/C_L, where I_D denotes the drain current of the on transistor when its gate voltage is near the rail and its drain voltage around $V_{DD}/2$ [13]. (3) The slew rate can also be approximated as $V_{DD}/(2T_d)$ [14].

It follows from (10) and (11) that for M noisy inverters in a delay line,

$$S_{\Phi,white,DL} = M \frac{\pi^2 T_d}{I_D^2 T_{in}} [S_I(f)|_{NMOS} + S_I(f)|_{PMOS}] + M \frac{4kT\pi^2 T_d}{I_D V_{DD} T_{in}}, \quad (12)$$

$$S_{\Phi,1/f,DL} = M \frac{\pi^2 T_d^2}{I_D^2 T_{in}^2} \left[S_{\frac{1}{f}}(f)|_{NMOS} + S_{\frac{1}{f}}(f)|_{PMOS} \right], \quad (13)$$

where it is assumed I_D is the same for NMOS and PMOS devices. In the special case where the input period is equal to the period of the corresponding ring oscillator, we have $1/f_{osc} = T_{in} = 2MT_d$, and (12) and (13) reduce to

$$S_{\Phi,white,DL} = \frac{\pi^2}{2I_D^2} [S_I(f)|_{NMOS} + S_I(f)|_{PMOS}] + \frac{2kT\pi^2}{I_D V_{DD}}, \quad (14)$$

$$S_{\Phi,1/f,DL} = \frac{\pi^2}{4MI_D^2} \left[S_{\frac{1}{f}}(f)|_{NMOS} + S_{\frac{1}{f}}(f)|_{PMOS} \right]. \quad (15)$$

With the aid of (9), we can now express the phase noise of an M-stage ring oscillator as:

$$S_{\Phi,white,ring}(\Delta f) = \frac{f_{osc}^2}{\Delta f^2} \left\{ \frac{1}{2I_D^2} [S_I(\Delta f)|_{NMOS} + S_I(\Delta f)|_{PMOS}] + \frac{2kT}{I_D V_{DD}} \right\}, \quad (16)$$

$$S_{\Phi,1/f,ring}(\Delta f) = \frac{f_{osc}^2}{4MI_D^2 \Delta f^2} \left[S_{\frac{1}{f}}(\Delta f)|_{NMOS} + S_{\frac{1}{f}}(\Delta f)|_{PMOS} \right]. \quad (17)$$

Note that these spectra are two-sided (i.e., $-\infty < f < +\infty$). Accounting for the factor of 2 difference between one-sided and two-sided spectra, we observe that the phase noise given by (17) is still twice that reported in [4]. As verified by the simulations in Section V, our result is correct. The factor of 2 error in [4] can be explained as follows. For a voltage-controlled oscillator (VCO) sensing a small sinusoidal voltage of peak V_m and frequency f_m, the relative magnitude of the sideband at the output is given by $K_{VCO}V_m/(2f_m)$, where K_{VCO} is the gain in Hz/V. It is tempting, but incorrect, to use this result directly for random noise, i.e., to write $K_{VCO}^2 S_n/(4f_m^2)$ for the phase noise resulting from noise with spectral density S_n [4]. Since phase noise is in fact the spectrum of Φ_n in $\cos(\omega_c t + \Phi_n)$, we integrate noise with respect to time and multiply the result by K_{VCO}, obtaining $S_{\Phi_n}(f_m) = K_{VCO}^2 S_n/f_m^2$. If S_n denotes a one-sided spectrum, then this result must be divided by a factor of 2 so as to represent a two-sided $S_{\Phi_n}(f_m)$, producing $S_{\Phi_n}(f_m) = K_{VCO}^2 S_n/(2f_m^2)$.

Equation (16) reveals that $S_{\Phi,white,ring}$ is independent of the number of stages, as recognized in prior work [4], [5]. To confirm that $S_{\Phi,white,ring}$ is fundamentally related to the power consumption (also recognized in [4], [5]), suppose two rings incorporate identical inverters, but one contains M_1 stages and the other M_2, where $M_1 > M_2$. We add enough capacitance to each node in the second ring so that the gate delays of the two rings, T_{d1} and T_{d2}, respectively, satisfy the relation $M_1 T_{d1} = M_2 T_{d2}$ and thus yield the same oscillation frequency. Since the gate delays are proportional to the load capacitances, it follows that $M_1 C_{L1} = M_2 C_{L2}$ and hence $f_{osc}(M_1 C_{L1}) V_{DD}^2 = f_{osc}(M_2 C_{L2}) V_{DD}^2$. That is, equal oscillation frequencies guarantee equal power consumptions in this case. Since the inverters are identical in the two designs, I_D and $S_I(\Delta f)$ in (16) are the same for the two oscillators, yielding the same $S_{\Phi,white,ring}(\Delta f)$.

Equation (17) shows that the phase noise due to flicker noise *falls* as the number of stages increases [4]. This is also observed in the simulation results of Section V.

C. Effect of Transition Symmetry on Flicker Noise Upconversion

The fundamental relation expressed by (9) implies that if flicker noise is upconverted in a delay line, so is it in a ring oscillator utilizing that delay line. Thus, the upconversion phenomenon can be studied in a simpler delay line environment.

The flicker-noise-induced phase noise of delay lines is formulated by (11), with ΔT representing a quantity roughly equal to half of the transition time caused by the NMOS or PMOS transistor in each stage. Interestingly, this equation suggests that the flicker noise is upconverted regardless of the relationship between ΔT_{NMOS} and ΔT_{PMOS}, a point in contradiction to the analysis in [5], which predicts zero upconversion if the rise and fall transitions are symmetric. In fact, as shown in Fig. 5(a), phase noise simulations of a 9-stage 2.4-GHz ring oscillator reveal that the phase noise changes by only a few decibels as the PMOS-to-NMOS width ratio varies from 1/4 to 4/1 and the rise-time-to-falltime ratio from 3 to 0.76. This weak dependence is also verified by examining the upconversion of a 1-MHz tone

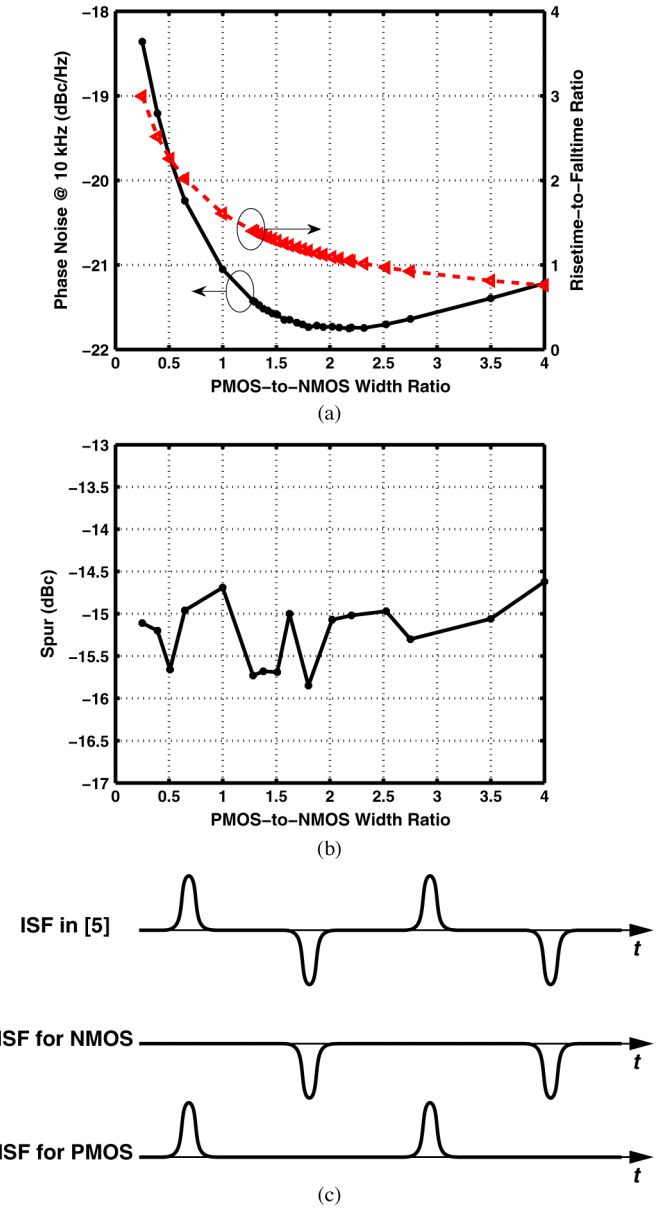


Fig. 5. (a) Phase noise and risetime-to-falltime ratio versus the PMOS-to-NMOS width ratio of a 9-stage 2.4-GHz ring oscillator, (b) spur power when a small sinusoidal voltage source is put in series with the gate of one NMOS transistor in the ring, and (c) ISF reported in [5] and uncorrelated ISF's for NMOS and PMOS devices.

placed in series with the gate of one NMOS transistor in the ring. Fig. 5(b) reveals that the FM sideband magnitude varies little.

The flaw in [5] can be explained as follows. Since the flicker noise currents injected by the NMOS and PMOS devices in a ring are uncorrelated, each must be characterized by its own impulse sensitivity function (ISF). Depicted in Fig. 5(c), the NMOS and PMOS ISFs cannot have zero time average with any choice of rise and fall transitions, thereby upconverting flicker noise unconditionally.

D. Effect of Scaling on Phase Noise

The white-noise-induced phase noise appears to be fundamentally related to the power dissipation and not much to the other factors. The effect of flicker noise, on the other hand, can be articulated by rewriting (17) as

$$S_{\Phi,1/f,ring}(\Delta f) = \frac{f_{osc}^2}{8\Delta f^3}\left[\left\{\frac{K}{MWLC_{ox}(V_{DD}-V_{TH})^2}\right\}_{NMOS} + \left\{\frac{K}{MWLC_{ox}(V_{DD}-V_{TH})^2}\right\}_{PMOS}\right], \tag{18}$$

where it is assumed $g_m = I_D/(V_{GS}-V_{TH})$ for velocity-saturated devices and $K/(WLC_{ox}\Delta f)$ is assumed to be one-sided and is therefore divided by 2. It follows that the principal parameter under the designer's control for reducing the phase noise is the total gate capacitance, $MWLC_{ox}$, of the ring oscillator. For example, as simulations confirm, $S_{\Phi,1/f,ring}$ varies by less than 1 dB as M goes from 3 to 16 while MWL and f_{osc} are constant. Notwithstanding changes in K with technology scaling, $S_{\Phi,1/f,ring}$ rises with a lower $V_{DD}-V_{TH}$ if the total gate capacitance is kept constant.

V. Simulation Results

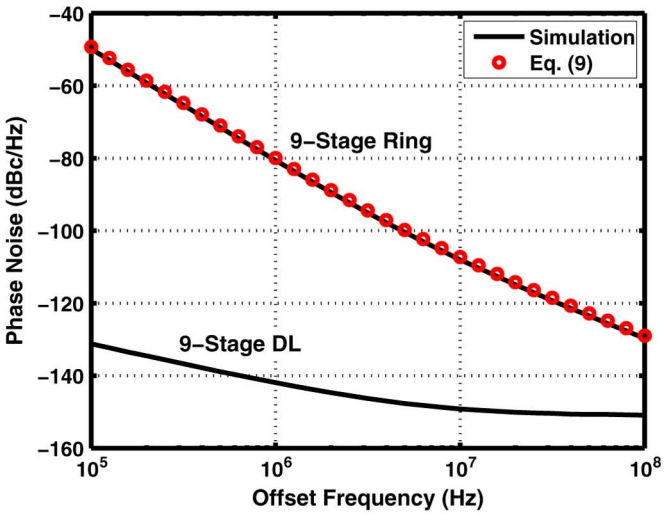
In this section, three sets of simulation results are presented: one to verify the fundamental shaping function, $f_{osc}^2/(\pi\Delta f)^2$, another to show the dependence of the phase noise on the number of delay stages, and the third to check the validity of our compact phase noise equations, (16) and (17).

In order to verify the relation expressed by (8), we have simulated 9-stage and 19-stage delay lines and ring oscillators in 65-nm CMOS technology. Each inverter incorporates a channel width of 0.6 μm and 1.2 μm for the NMOS and PMOS devices, respectively, and a channel length of 60 nm. The circuits operate with a 1-V supply. In each case, the frequency of the input applied to the delay line is chosen equal to the corresponding ring oscillator frequency.

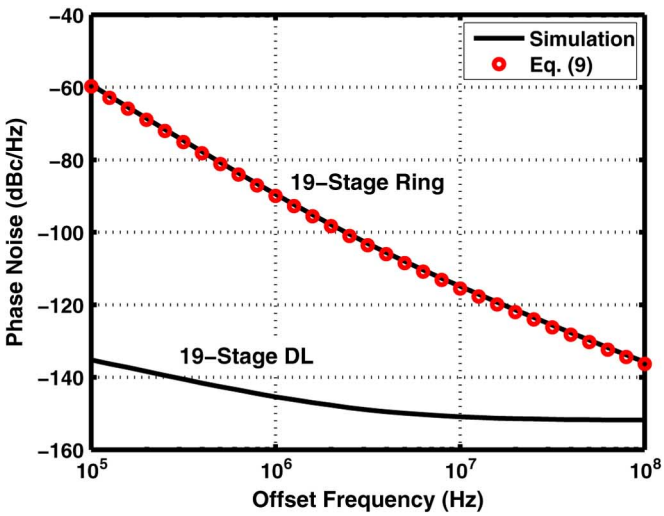
Fig. 6(a) plots the simulated phase noise for the 9-stage delay line and the corresponding ring oscillator. The latter's phase noise is obtained using (8) as well as direct simulations. We note good agreement in both flicker noise and white noise regimes. The oscillation frequency is 3.8 GHz and the power consumption 0.34 mW. Fig. 6(b) repeats the results for a 19-stage arrangement operating at a frequency of 1.7 GHz and drawing 0.32 mW. The results agree well in this case, too.

Fig. 7 plots the simulated phase noise of three ring oscillators operating at 9.54 GHz. Explicit capacitors are added to all nodes of 3-stage and 5-stage rings. Since the power consumption varies slightly, from 1.39 mW to 1.47 mW, as the rings become longer, the phase noise plots are normalized to the corresponding values. We observe that the white-noise-induced phase noise remains unchanged as the number of stages increases, but, as predicted by (17), the flicker-noise-induced component decreases in proportion to M.

Fig. 8 plots the simulated phase noise of the 9-stage ring oscillator as well as the calculated phase noise using (16) and (17).



(a)



(b)

Fig. 6. Simulated phase noise of delay lines and ring oscillators as well as calculated phase noise of the ring oscillator using the phase noise of the delay line for (a) 9-stage, and (b) 19-stage configurations.

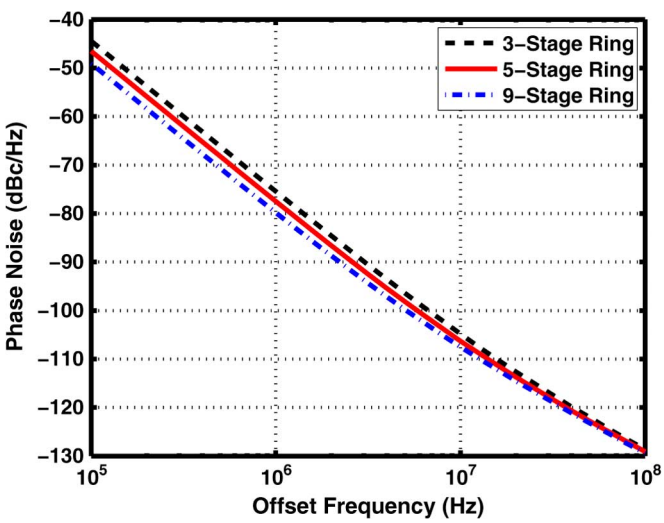


Fig. 7. Simulated effect of number of delay cells on the phase noise of ring oscillators.

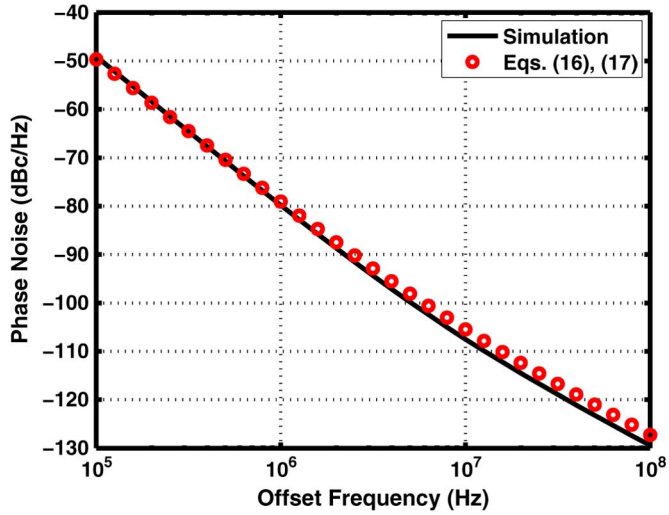


Fig. 8. Simulated phase noise of a 9-stage ring oscillator and calculated phase noise using compact equations (16) and (17).

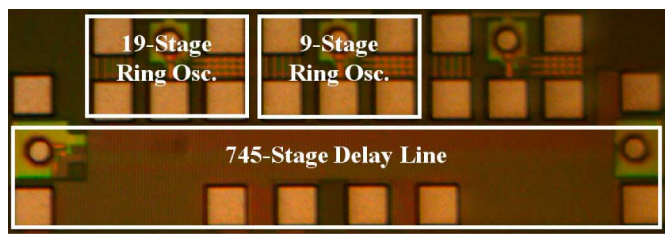


Fig. 9. Die photograph.

(The flicker and white current noise spectra, $S_{1/f}$ and S_I, respectively, are obtained from simulations in Cadence).[2]

VI. Experimental Results

The delay lines and ring oscillators described in Section V have been fabricated in 65-nm CMOS technology and characterized. Fig. 9 shows a die photograph of the prototypes. Each circuit is followed by an on-chip open-drain buffer for driving 50-Ω instrumentation.

The low phase noise of delay lines poses difficulties in measurement. For this reason, the delay line prototype in fact incorporates 745 stages rather than 9 or 19, producing a readily measurable phase noise (Fig. 10). This value is then scaled down by a factor equal to 745/9 or 745/19 to obtain the phase noise of the respective delay lines.

The phase noise of ring oscillators also proves difficult to measure if low offset frequencies are of interest. The random fluctuations of the free-running center frequency tend to smear the phase noise profile. It is therefore beneficial to phase-lock the oscillator to a low-noise input with a sufficiently small loop bandwidth so as to negligibly affect the phase noise in the offset frequency range of interest. Fig. 11 shows the test setup constructed around each ring oscillator to create a type-I phase-locked loop (PLL). Here, an off-the-shelf mixer serves as a phase detector, comparing the phases of an external RF signal

[2]The value of I_D is obtained from transient simulations at the point when $V_{DS} \approx V_{DD}/2$. The V_{GS} and V_{DS} values corresponding to this case are then used in a simple noise simulation of a single transistor.

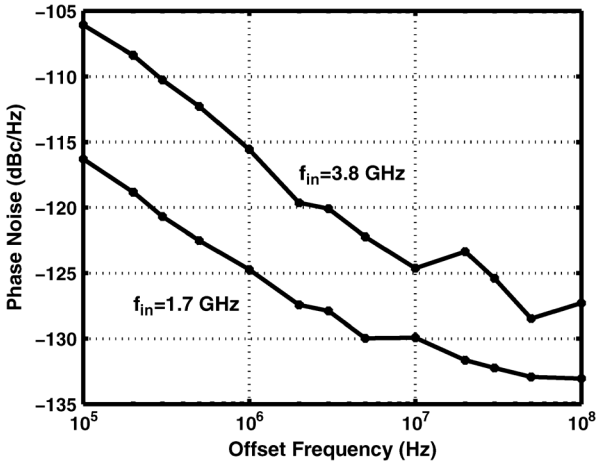


Fig. 10. Measured phase noise of 745-stage delay line at two different input frequencies.

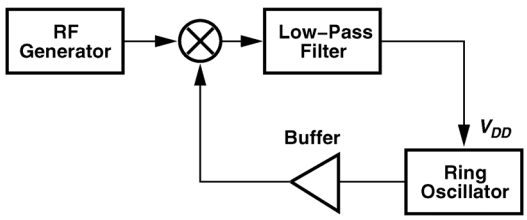


Fig. 11. Phase-locking of the ring oscillators for phase noise measurements.

and the ring oscillator output. The latter's supply line acts as the control voltage. The loop bandwidth is set by the choice of the components in the low-pass filter.

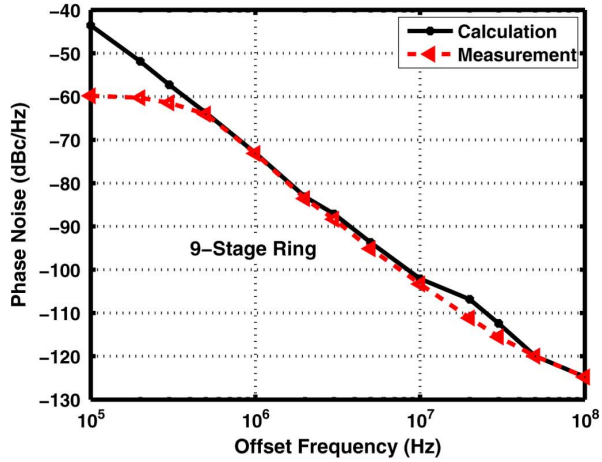
Fig. 12(a) plots the phase noise of the 9-stage ring oscillator obtained by (a) direct measurement, and (b) by multiplying the measured delay line phase noise by $f_{osc}^2/(\pi\Delta f)^2$. We observe a reasonable agreement. Fig. 12(b) repeats the results for the 19-stage configuration. In both cases, the effect of the PLL manifests itself at low offset frequencies.

VII. Conclusion

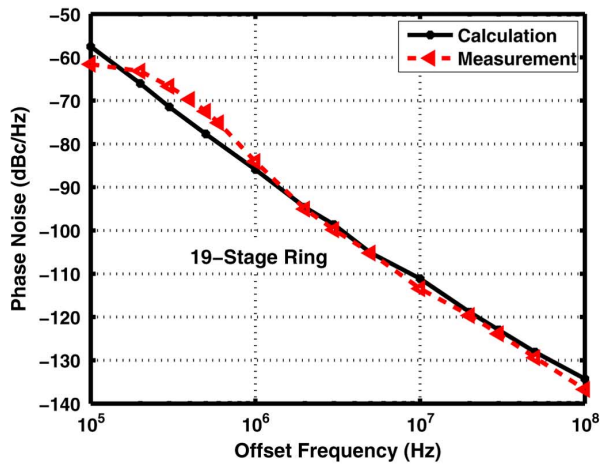
It is shown that the closed-loop phase noise of a ring oscillator is equal to its open-loop phase noise multiplied by a simple shaping function, $f_{osc}^2/(\pi\Delta f)^2$. This relation reveals why delay lines exhibit much less noise than do ring oscillators. It also leads to compact phase noise equations and shows why flicker noise is upconverted even with symmetric rise and fall times. The flicker-noise-induced phase noise is not a strong function of the PMOS-to-NMOS ratio and the minimum phase noise does not necessarily happen when the rise and fall times are symmetric. The validity of the shaping function has been verified on two ring oscillators designed in 65-nm CMOS technology.

Acknowledgment

The authors wish to thank Realtek Semiconductor for supporting this research and the TSMC University Shuttle Program for chip fabrication.



(a)



(b)

Fig. 12. Measured phase noise of ring oscillators and the calculated phase noise using the measured phase noise of delay line for (a) 9-stage, and (b) 19-stage rings.

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