A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology

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***Abstract*—Fundamental oscillators prove the existence of gain at high frequencies, revealing the speed limitations of other circuits in a given technology. This paper presents an oscillator topology that employs feedback from an output stage to the core, thus achieving a high speed. The behavior of the proposed oscillator is formulated and simulations are used to compare it with the conventional cross-coupled pair circuit. Three prototypes realized in 65-nm CMOS technology operate at 205 GHz, 240 GHz, and 300 GHz, each drawing 3.7 mW from a 0.8-V supply.**

***Index Terms*—Carrier generation, frequency generation, frequency synthesis, microwave oscillators, millimeter-wave oscillators, spiral inductors, transmission lines, VCOs.**

I. Introduction

FUNDAMENTAL oscillators serve as a benchmark of the technology, providing a more realistic measure of the attainable speeds than do f_T and $f_{\max}$ of single transistors. For example, such oscillators demonstrate the existence of *gain* at high frequencies, paving the way for the design of other building blocks, e.g., amplifiers and frequency dividers. They also reveal accuracy limitations of passive and active device models.

The speed of fundamental CMOS oscillators has grown by roughly a factor of 14 every ten years. As shown in Fig. 1 [1]–[8], the oscillation frequency reached 1.4 GHz in 1988 [1] and has steadily climbed since. Also plotted are the f_T's of the CMOS technologies around the time they have entered production. The f_T's are obtained by simulations based on transistor models available for each generation.[1]

This paper describes an oscillator topology that achieves frequencies as high as 300 GHz in 65-nm CMOS technology, the fastest reported in any silicon process. Originally conceived for bimodal operation [10], [11] in the gigahertz range, the circuit also proves superior to the conventional cross-coupled oscillator (XCO) in terms of the maximum oscillation frequency. Specifically, it is shown that the proposed topology reduces the effect of the inductor capacitance by a factor of 2 and the load capacitance by a factor of 4.

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[1]The measured f_T's reported in [9] for 90-nm and 65-nm devices are approximately equal to 140 GHz and 180 GHz, respectively, suggesting that the simulation overestimates the latter.

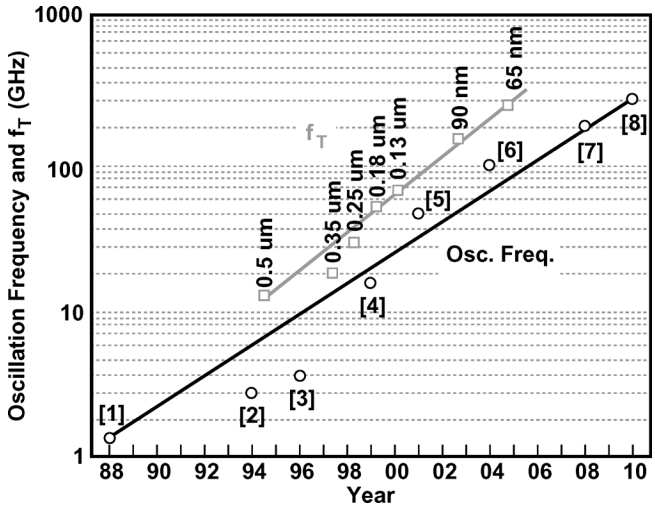

Fig. 1. Historical growth of fundamental oscillation frequency in CMOS technology.

Section II provides a brief overview of oscillation frequency limitations. Section III presents the proposed oscillator, formulates its behavior, and compares its maximum speed with that of the XCO. Section IV describes the prototype design and Section V summarizes the experimental results.

II. Background

A. Fundamental and Superharmonic Oscillators

High-frequency periodic waveforms can be derived directly from a fundamental oscillator or, through nonlinear operation, from a "superharmonic" oscillator. Examples of the latter include "push-push" topologies (where the second harmonic is sensed) or "edge-combining" arrangements [12], also known as "linear superposition" [13] or "N-push" oscillators [14]. Of course, given a fundamental oscillator, one can always extract a higher harmonic using one of these techniques to obtain a proportionally higher frequency. However, the two oscillator categories entail different system design implications. Fundamental topologies readily provide differential and even quadrature outputs with relatively large voltage swings, simplifying the design of mixers and frequency dividers. Superharmonic oscillators, on the other hand, typically provide only a single-ended output [13], [15] (except for that in [12]), requiring bulky baluns, 90° couplers, and buffers. In addition, the finite lower harmonics that leak to the output of a superharmonic topology may downconvert unwanted signals in a receiver.

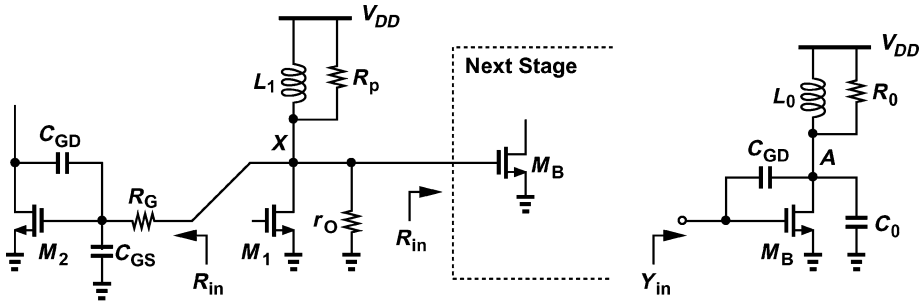

Fig. 2. (a) Loss mechanisms in an oscillator, (b) simplified circuit of stage following the oscillator.

B. Oscillation at $f_{\max}$

Defined as the frequency at which the unilateral power gain of an active device falls to unity, $f_{\max}$ is believed to set the upper bound on the oscillation frequency. It can be shown that for a MOSFET

$$\omega_{\max}^2 = \frac{g_m^2 r_O}{4R_G(C_{GS}+C_{GD})\left[C_{GS}+(1+g_m r_O)C_{GD}\right]} \quad (1)$$

where $\omega_{\max} = 2\pi f_{\max}$ and R_G denotes the lumped equivalent value of the gate resistance [16]. We note that $\omega_{\max}$ is, to the first order, independent of the drain-bulk junction capacitance, C_{DB}. In fact, operation at $\omega_{\max}$ assumes that the transistor is embedded within a *lossless* network that unilateralizes the device, nulls the effect of C_{DB}, and matches the input and output ports of the device for maximum power transfer. Unfortunately, the loss of on-chip passive networks prohibits a realistic oscillator to achieve $\omega_{\max}$. Simulations indicate an $f_{\max}$ of roughly 380 GHz for 65-nm nMOS devices with a drain current density of 0.8 mA/μm (a V_{GS} of about 0.45 V). Found to be an optimum value for the oscillator designs described in Sections III and IV, this current density differs from the value of 0.3–0.4 mA/μm recommended in [9] for maximum f_T. This disparity can be attributed to the gate resistance, which directly impacts the maximum oscillation frequency but not the f_T [16]. The accuracy of these simulations is limited by the quasi-static nature of the lumped BSIM4 model.

C. Loss Mechanisms in Oscillators

At frequencies of hundreds of gigahertz, the design of oscillators must deal with several loss mechanisms. As conceptually illustrated in Fig. 2(a), the signal circulating within the oscillator experiences (1) the loss of the resonating device, L_1; for a narrow frequency range, the loss is modeled by $R_p = QL_1\omega$; (2) the output resistance of the oscillating transistor(s), r_O; (3) the gate resistance of the oscillating transistor(s), R_G; and (4) the input resistance of the following stage, R_{in} (typically, a buffer, a mixer, or a divider). The last mechanism can be formulated from the simplified diagram in Fig. 2(b), where R_0 encompasses all of the losses at node A. At resonance

$$Re\{Y_{\text{in}}\} = \frac{(1+g_m R_0)R_0 C_{GD}^2\omega^2}{1+R_0^2 C_{GD}^2\omega^2} \quad (2)$$

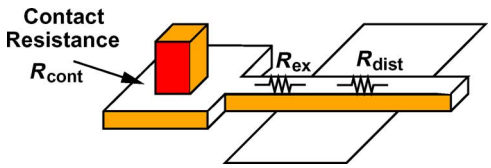

Fig. 3. Gate resistance components.

which reduces to $[(1/g_m)||R_0]^{-1}$ if $R_0^2 C_{GD}^2\omega^2 \ll 1$. We must add R_G to $(Re\{Y_{\text{in}}\})^{-1}$ to account for the gate resistance of M_B.

The key point here is that all of the mechanisms identified above produce comparable losses at several hundred gigahertz, forcing operation well below $f_{\max}$. By contrast, oscillator design at tens of gigahertz must deal with primarily the loss of the inductor.

D. Effect of Gate Resistance

As suggested by (1), the gate resistance proves a limiting factor in high-frequency oscillator design. In deep-submicron technologies, R_G arises from three components (Fig. 3): (1) the poly-metal contact resistance, R_{cont} (about 15 Ω per contact), (2) the extrinsic resistance, R_{ex}, and (3) the distributed resistance, R_{dist}. With a sheet resistance of about 10 Ω/square and the required spacing between the contact and the channel, $R_{ex} = 35\,\Omega$ (for $L = 60$ nm), and hence $R_{cont} + R_{ex} = 50\,\Omega$.

The lumped equivalent value of R_{dist} is given by $R_{dist}/3$ [16]. It is desirable to contact the gate on both ends to reduce R_{dist} by a factor of 4, and minimize the width so that $R_{dist}/3$ is well below the unscalable component, $R_{cont}+R_{ex}$. However, very narrow gates exhibit a longer equivalent channel length due to the distribution of dopants toward the shallow trench surrounding the transistor. As a compromise, in this work each gate finger has a W/L of 0.4 μm/60 nm and contacts on both ends, yielding an equivalent lumped resistance of 30 Ω.

III. Proposed Oscillator

A. Evolution of Proposed Oscillator

Shown in Fig. 4(a), the proposed topology can be viewed as an oscillating core and a buffer, with some of the output energy of the latter coupled back to the former. We call this arrangement the "buffer-feedback oscillator" (BFO) and describe

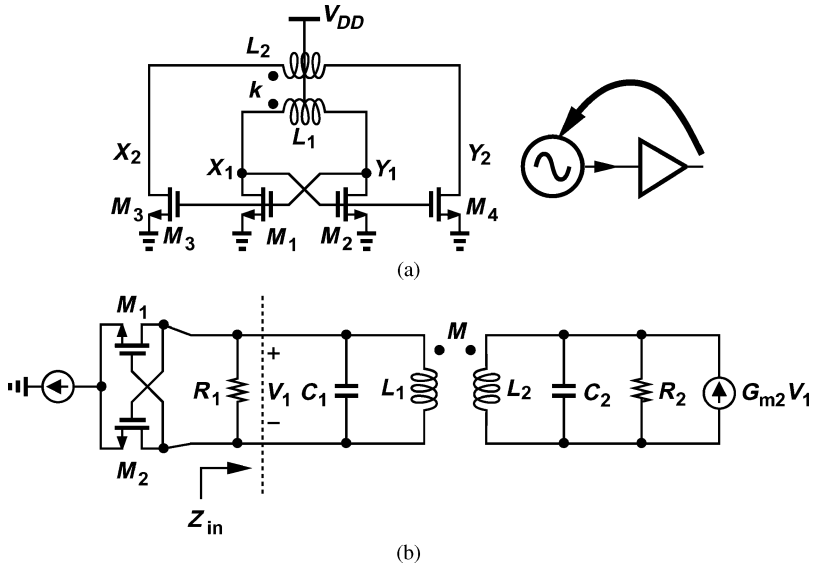

Fig. 4. (a) Buffer-feedback oscillator. (b) Simplified model.

a transformation that converts an XCO to the BFO. This evolutionary perspective ultimately allows a fair comparison of the two oscillators.

As explained in [17], the circuit of Fig. 4(a) can be decomposed as shown in Fig. 4(b), where G_{m2} represents the buffer transconductance, L_2 and C_2 its load tank, and R_2 the loss of the tank. If $Z_{\rm in}$ goes to infinity at an imaginary frequency, then the circuit to the right of the dashed line can oscillate. Setting the denominator of $Z_{\rm in}$ to zero yields the oscillation frequencies as [17]

$$\omega_{1,2}^2 = \frac{L_1C_1 + L_2C_2 \pm \sqrt{(L_1C_1 + L_2C_2)^2 - 4(L_1L_2 - M^2)C_1C_2}}{2(L_1L_2 - M^2)C_1C_2} \tag{3}$$

and the startup condition as

$$G_{m2} = \frac{L_1L_2 - M^2}{R_2M}\omega_{1,2}^2 - \frac{L^2}{R_2M}. \tag{4}$$

If $L_1 = L_2 = L$ and $C_1 = C_2 = C$, then

$$\omega_1^2 = \frac{1}{(L+M)C}, \quad G_{m2,1} = +\frac{1}{R_2}, \tag{5}$$

$$\omega_2^2 = \frac{1}{(L-M)C}, \quad G_{m2,2} = -\frac{1}{R_2}. \tag{6}$$

In this work, we consider only the lower mode, ω_1, at which the inductor currents are in phase. The higher mode, ω_2, may entail greater inductor losses due to the out-of-phase currents flowing through the two inductors. This mode can be present if the coupling polarity is inverted and has not been observed in the prototypes described in Section IV.

We can conceptually assume that G_{m2} in Fig. 4(b) cancels the loss of the second tank and the cross-coupled pair the loss of the first tank (modeled by R_1). In reality, this partitioning may not hold. Moreover, the tanks may not be identical. We return to these points in the next section.

We seek a transformation from the XCO to the BFO that reveals the speed advantage of the latter. The XCO/BFO transformation proceeds as follows. We begin with the XCO and, as shown in Fig. 5(a), view its symmetric load inductor as two equal mutually-coupled inductors, L_1 and L_2. Our goal is to derive the BFO without significantly altering the inductor and its parasitics. Depicted in Fig. 5(b), the complete XCO models the inductor's parasitic capacitance by four components and its loss by R_p. The capacitors C_L denote the input capacitance of the following stage.

We now decompose the load inductor into L_1 and L_2, with their mutual coupling intact [Fig. 5(c)]. Shown in Fig. 5(d), the circuit representation includes a resistance of $R_p/2$ in parallel with each inductor. In the last step, we turn the two-inductor (transformer) structure by 90° and tie its terminals to the cross-coupled pair and the output transistors [Fig. 5(e)]. Note that the overall inductor has remained substantially unchanged. Fig. 5(f) shows the actual implementation using octagonal inductors. The XCO and its descendent BFO are analyzed in the following section to quantify their maximum oscillation frequencies.

A by-product of the foregoing transformation is the *reduction* of the effect of the inductor's interwinding capacitance. This capacitance sustains a large voltage difference in Fig. 5(a)—due to differential excitation—but a small voltage difference in Fig. 5(f) because the voltages at X_1 and X_2 and hence other adjacent points along L_1 and L_2 are approximately equal.

B. Analysis

The objective of our analysis is to derive the oscillation startup conditions and frequencies of the XCO and the BFO, aiming to prove that the latter can achieve a higher speed. In order to arrive at an intuitively-appealing mathematically-tractable result, we make a number of simplifying assumptions here.

Our assumptions are as follows. 1) The gate-drain overlap capacitance, C_{GD}, is neglected. 2) The transistor can be modeled

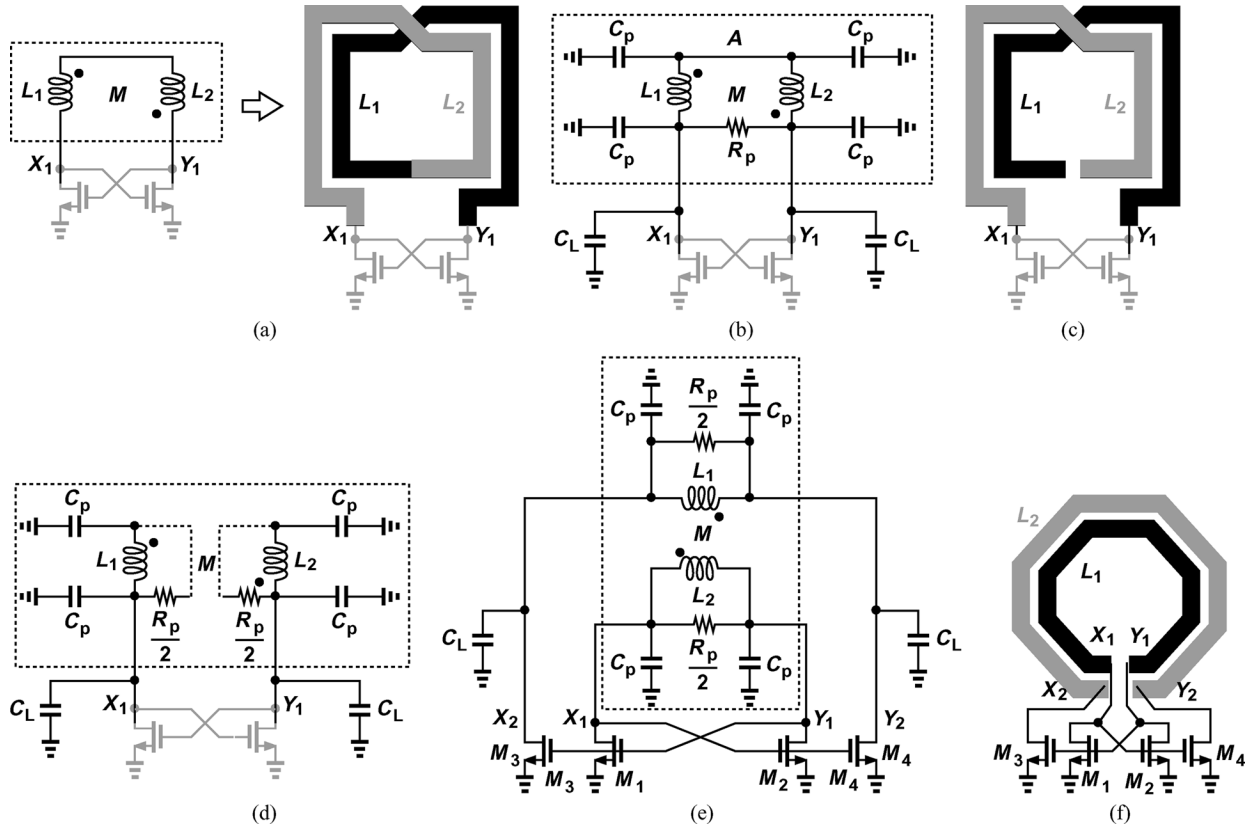

Fig. 5. (a) Cross-coupled oscillator with load inductor viewed as two mutually-coupled inductors, (b) XCO with inductor parasitics, (c) decomposition of inductors, (d) circuit model of (d), (e) reconfiguration to obtain the BFO, (f) actual implementation of BFO.

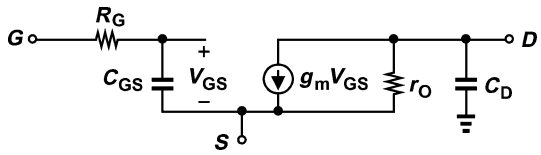

Fig. 6. Simplified transistor model for hand calculations.

by the lumped circuit shown in Fig. 6, where C_{GD} is absent but loss mechanisms are included; (3) The inductor(s) can be modeled by a lumped *RLC* circuit; (4) The interconnects are short and hence their parasitics negligible; (5) If the two tanks in Fig. 4(b) are not identical but somewhat similar, then $\omega_1^2 = [(L+M)C]^{-1}$, where $L = (L_1+L_2)/2$, $C = (C_1+C_2)/2$. In addition, if $G_{m1} = G_{m2}$, then we can assume the loss of each tank is modeled by an "average" resistance given by $2(R_1 \| R_2)$; (6) To scale the transconductance of a transistor by a factor of K, both the width (i.e., the number of gate fingers) and the drain current are scaled by a factor of K. The transistor-level simulations presented in the next section lift the first, second, and fifth assumptions and employ a BSIM4 model for the transistor.

Our derivations will draw upon the two arrangements shown in Fig. 7. In Fig. 7(a)

$$Re\{Y_{\text{in}}\} \approx \frac{1}{R_G C_{GS}^2 \omega^2}. \tag{7}$$

In the simplified cross-coupled pair of Fig. 7(b)

$$Y_X(s) = \frac{C_{GS}s - g_m}{2(R_G C_{GS}s + 1)} \tag{8}$$

and hence

$$Re\{Y_X\} = \frac{-g_m + R_G C_{GS}^2 \omega^2}{2\,(1 + R_G^2 C_{GS}^2 \omega^2)} \tag{9}$$

$$Im\{Y_X\} = \frac{(1 + g_m R_G) C_{GS} \omega}{2\,(1 + R_G^2 C_{GS}^2 \omega^2)}. \tag{10}$$

If $R_G^2 C_{GS}^2 \omega^2 \ll 1$, then

$$Re\{Y_X\} \approx -\frac{g_m}{2} + \frac{R_G C_{GS}^2 \omega^2}{2} \tag{11}$$

i.e., $Re\{Y_X\}$ consists of a negative resistance of $-2/g_m$ in parallel with a positive resistance of $2/(R_G C_{GS}^2 \omega^2)$. Moreover,

$$Im\{Y_X\} \approx (1 + g_m R_G) C_{GS} \omega \tag{12}$$

as if C_{GS} were enlarged by a factor of $1 + g_m R_G$. (The effect of r_O and C_D is taken int account below.) Appendix I presents a more detailed analysis including the gate-drain capacitance.

Based on the above observations, we can reduce the XCO of Fig. 5(b) to the arrangement shown in Fig. 8(a), where g_m denotes the small-signal transconductance of each transistor. Note that grounded (single-ended) capacitances and resistances are

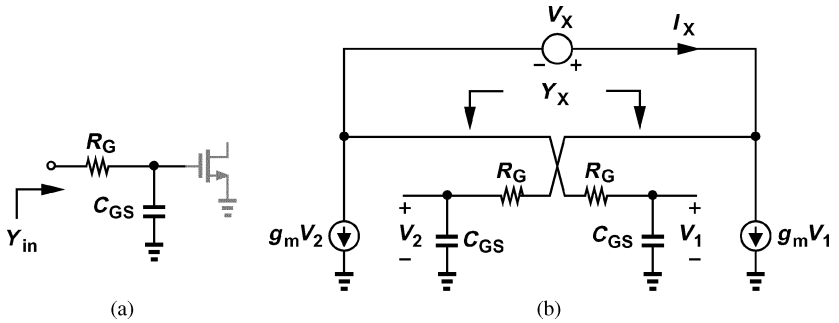

Fig. 7. Input admittance of (a) a simple CS stage, and (b) a cross-coupled pair.

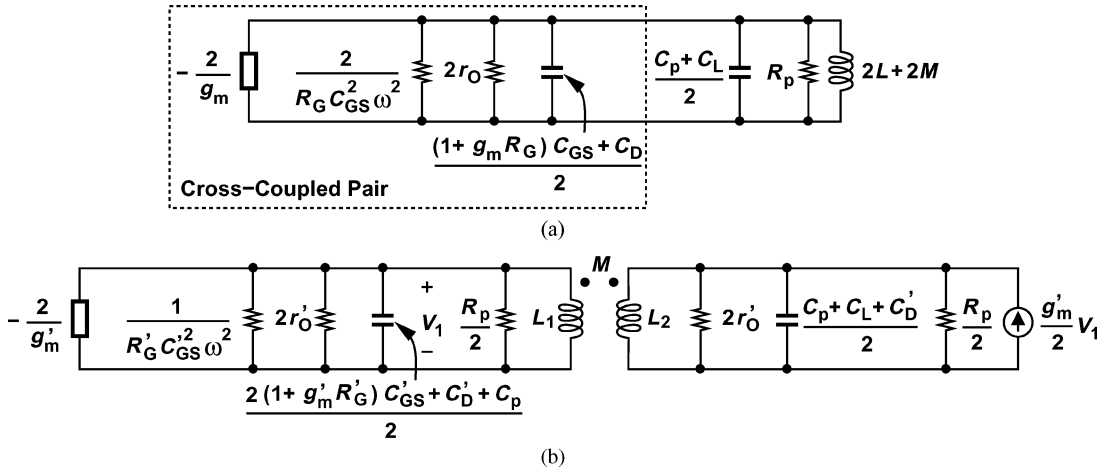

Fig. 8. Equivalent circuits of (a) XCO, and (b) BFO.

halved and doubled, respectively, to convert them to floating (differential) components. Also, the input resistance of the following stage is neglected. The oscillation startup condition is given by

$$\frac{2}{g_m} = R_p \,||(2r_O)|| \frac{2}{R_G C_{GS}^2 \omega^2} \tag{13}$$

and the oscillation frequency by

$$\omega_{XCO}^2 = \frac{1}{(L+M)\left[(1+g_mR_G)C_{GS} + C_D + C_p + C_L\right]}. \tag{14}$$

Similarly, the BFO of Fig. 5(e) can be simplified to the topology shown in Fig. 8(b), where the primes distinguish the component values from those in Fig. 8(a). Note that C'_{GS} is multiplied by 2 and the resistance due to R'_G divided by 2 so as to account for the output transistors. Assuming $G_{m1} = G_{m2}$ and $L_1 = L_2$, and using the "averaging" approximations mentioned above, we cancel the loss on the L_1 side by the negative resistive, $-2/g'_m$, and that on the L_2 side by the voltage-dependent current source, $(g'_m/2)V_1$. Since the parallel resistances on the two sides differ by one component, $1/(R'_G C'^2_{GS}\omega^2)$, we obtain the average resistance as $(R_p/2)||(2r'_O)||[2/(R'_G C'^2_{GS}\omega^2)]$. Thus, the oscillation startup condition emerges as

$$\frac{2}{g'_m} = \frac{R_p}{2} \,||(2r'_O)|| \frac{2}{R'_G C'^2_{GS}\omega^2}. \tag{15}$$

In other words, if (13) holds for the XCO, then (15) must hold for the BFO that is derived from the XFO. Equation (15) suggests that g'_m must be approximately twice g_m. If both the width (i.e., the number of gate fingers) and the bias current of the transistors are doubled, then $g'_m = 2g_m$, $r'_O = r_O/2$, $R'_G = R_G/2$, $C'_{GS} = 2C_{GS}$, and $C'_D = 2C_D$.

We now obtain the oscillation frequency of the BFO using the "average" capacitances:

$$\omega_{\rm BFO}^2 = \frac{1}{(L+M)\left[\frac{(1+g'_mR'_G)C'_{GS}}{2} + \frac{C'_D+C_p}{2} + \frac{C_L}{4}\right]}. \tag{16}$$

With the $2\times$ transistor scaling mentioned above, this expression reduces to

$$\omega_{\rm BFO}^2 = \frac{1}{(L+M)\left[(1+g_mR_G)C_{GS} + C_D + \frac{C_p}{2} + \frac{C_L}{4}\right]}. \tag{17}$$

We observe from (14) and (17) that the BFO lowers the effect of inductor parasitics by a factor of 2 and the next stage input capacitance by a factor of 4. That is, the BFO speed advantage is more pronounced as the "fanout" seen by each oscillator increases.[2] However, as shown in the next section, circuit simulations using more realistic models and avoiding the "averaging"

[2]Intuitively, we can attribute the twofold reduction of C_p to the distribution of the inductor parasitics over the two stages, and the fourfold reduction of C_L to the lower fanout (because all transistors in the BFO are doubled in width and bias current) and the "averaging" effect within the BFO.

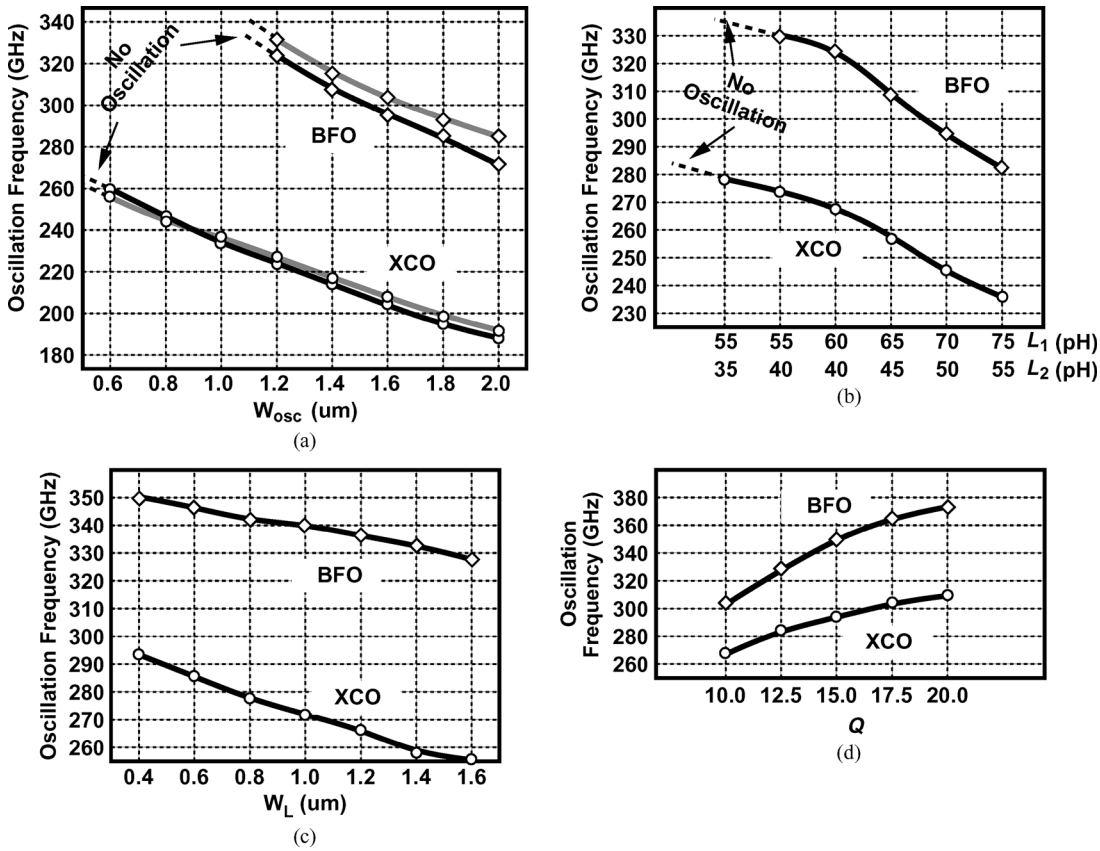

Fig. 9. Simulated behavior of XCO and BFO as a function of (a) width of transistors in each oscillator (black line: $W_L = 0.4\,\mu$m, $L_1 = 50$ pH, $L_2 = 70$ pH; gray line: $W_L = 1\,\mu$m, $L_1 = 45$ pH, $L_2 = 65$ pH), (b) inductance values, (c) input transistor width of following stage, (d) Q of inductors.

concept reveal that the BFO has about 18% speed advantage even with a small fanout. Also, as mentioned in Section III-A, the BFO reduces the effect of the interwinding capacitance.

The foregoing derivations have tacitly assumed that R_p and $1/\omega^2$ are the same in (13) and (15). Since $\omega_{\rm BFO} > \omega_{XCO}$, the value of $R_p/2$ in (15) is in fact greater than half of R_p in (13) [for a constant $Q\ (= L\omega/R_p)$]. This relaxes the required value of g'_m. On the other hand, the component $2/(R'_G C'^2_{GS}\omega^2)$ in (15) is *lower* than $2/(R_G C^2_{GS}\omega^2)$ in (13) (for a $2\times$ transistor scaling scenario), demanding a higher g'_m. It is difficult to incorporate these dependencies in the above comparisons, but the two effects partially cancel.

The BFO provides an even greater speed advantage if the input resistance, $R_{\rm in}$, of the stage following the oscillators is taken into account. To this end, a component equal to $2R_{\rm in}$ is placed in parallel with the terms on the right-hand side of (13) and (15), dropping the former by a larger percentage than the latter. The simulation results in the next section embody these effects.

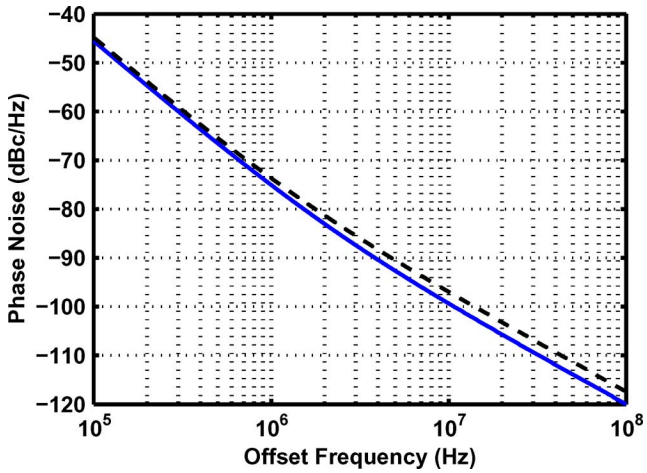

Fig. 10. Simulated phase noise of XCO at 265 GHz (dashed line) and BFO at 310 GHz (solid line).

C. Simulation Results

Transistor-level simulations are carried out to compare the XCO and BFO oscillation frequencies as a function of four parameters: 1) the width of the oscillator transistors, W_{osc} (the four transistors in the BFO are identical); 2) the load inductance; 3) the input transistor width of the subsequent stage, W_L; and 4) the Q of the load inductors. The simulations include a gate resistance of 30 Ω for each 0.4-μm-wide gate finger, a coupling factor of 0.4 between L_1 and L_2 in Figs. 5(a) and 5(e), and an inductor Q of 20 (except for the fourth case). The two inductor segments, L_1 and L_2, are unequal to reflect the choices in the prototypes.

Fig. 9(a) plots the oscillation frequencies obtained from the first simulation as W_{osc} and the corresponding drain currents are reduced from 2 μm so as to reach the maximum speed of each topology. Two cases have been considered to study the effect of the subsequent stage: (a) $W_L = 0.4\,\mu$m, $L_1 = 50$ pH, $L_2 = 70$ pH; (b) $W_L = 1\,\mu$m, $L_1 = 45$ pH, $L_2 = 65$ pH. In both cases, the BFO exhibits a speed advantage of about 23%.

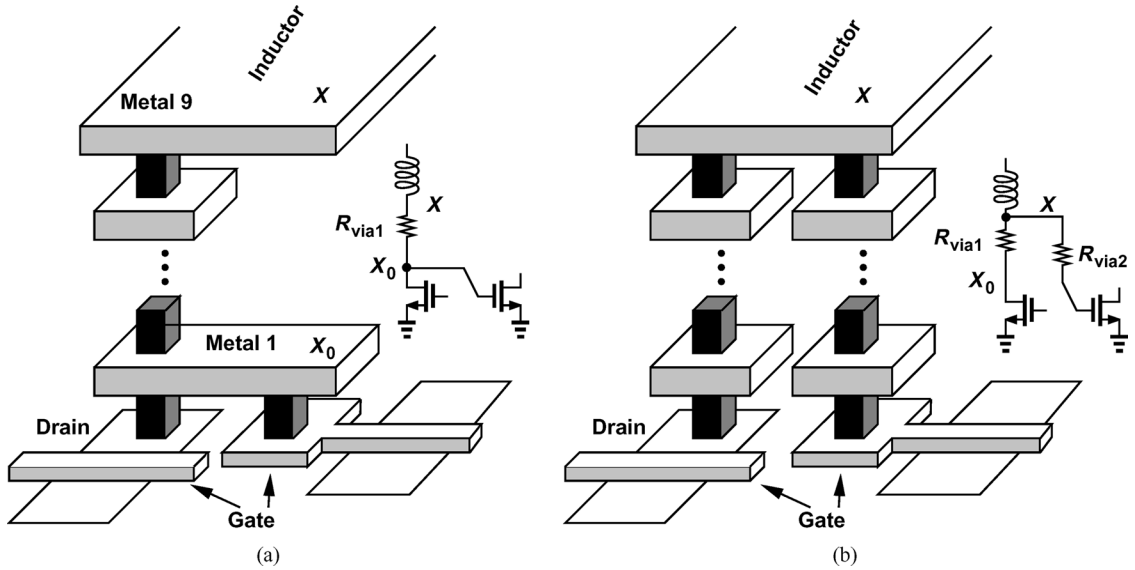

Fig. 11. Effect of contact and vias resistance in series with (a) load inductor, or (b) drain of transistor.

Note that, as predicted in the previous section, the minimum W_{osc} for the BFO (1.2 μm) is twice that for the XCO. The higher speed accrues at a cost of fourfold increase in power dissipation, an expected result because for frequencies approaching $f_{\max}$ the speed-power trade-off becomes heavily sublinear.

Depicted in Fig. 9(b) are the results as L_1 and L_2 vary. For each choice of the inductors, the transistor widths in the oscillators are reduced to place the circuits at the edge of oscillation.

Figure Fig. 9(c) plots the oscillation frequencies as the input transistor width of the following stage varies. As with the second simulation, for each choice of W_L, the oscillators' transistor widths are reduced to reach the edge of oscillation. We observe that the BFO speed advantage begins at about 18% for $W_L = 0.4$ μm and rises as W_L increases.

Shown in Fig. 9(d) is the oscillators' behavior as a function of the inductor Q, with W_{osc} reduced for each value of Q to operate at the edge of oscillation. These results suggest that the BFO speed advantage begins at about 14% for $Q = 10$ and reaches about 20% for $Q = 20$.

Fig. 10 plots the simulated phase noise of the XCO at 265 GHz and the BFO at 310 GHz. With the transformation described above, the former consumes one-fourth the power of the latter. An inductor Q of 20 is assumed. We observe that the push towards the highest oscillation frequency does degrade the trade-off between phase noise and power dissipation.

IV. Prototype Design

A. Realization and Modeling

Three prototypes of the BFO have been realized with different inductor designs. Implemented as single-turn symmetric octagonal metal-9 structures, L_1 and L_2 are "nested" so as to sustain a coupling factor of 0.4. The diameter of L_1 varies from 24 μm to 40 μm and that of L_2 from 32 μm to 48 μm, providing nominal values of $L_1 = 45$, 65, 85 pH and $L_2 = 65$, 85, 105 pH. Each of the four transistors has a W/L of 1.6 μm/60 nm with a gate finger width of 0.4 μm and a bias current of 1 mA.

Since the transistors incorporate a gate finger width of 0.4 μm, the source/drain areas accommodate only two contacts. As a result, the S/D series resistance due to only the contacts and vias becomes comparable with that of small inductors. Fig. 11(a) illustrates a case where the current flowing through a metal-9 spiral must descend through eight vias and one contact to reach the drain of a transistor. If the gate of the next stage's input device senses the voltage at node X_0, then R_{via1} (the sum of all via resistances) appears in series with the inductor. On the other hand, as shown in Fig. 11(b), if the gate senses the voltage at node X, albeit through another resistance, R_{via2}, we expect the effect of R_{via1} to vanish. Simulations suggest that the "*force and sense*" (Kelvin) arrangement in Fig. 11(b) achieves 3% higher speed than the topology in Fig. 11(a) even though R_{via2} introduces its own loss.

The oscillation frequencies of the prototypes are predicted using the modeling methodology described in [18]. The entire layout, including the gate polysilicon fingers (but excluding the source/drain pn junctions), is imported into HFSS and simulated as a multi-port network. The S-parameters thus obtained are then returned to Cadence and simulated with the BSIM4 (logic) model of the transistors.[3]

B. Design for Testability

Direct measurement of oscillators at these frequencies is difficult for two reasons: (a) the small output transistors driving 50-ohm instrumentation deliver very little power, and (b) the harmonic mixers available for these bands suffer from a high loss (50 to 60 dB). In this work, a harmonic mixer is placed on-chip to avoid driving 50 Ω at hundreds of gigahertz. Shown in Fig. 12, the mixer multiplies a harmonic of an external input by the oscillator output, generating an intermediate frequency (IF) in the range of 30 to 50 GHz. The IF output can thus be monitored directly on a spectrum analyzer with no need for external harmonic mixers. Of course, the on-chip mixer still suffers from tens of decibels of loss, but it only moderately loads

[3]The gate fingers are modeled as metal lines in HFSS and their resistance is included in circuit simulations.

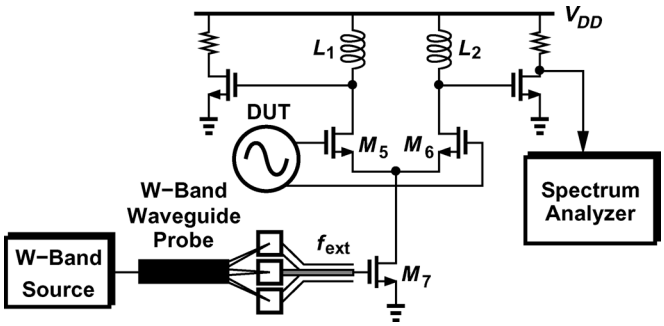

Fig. 12. On-chip harmonic mixer.

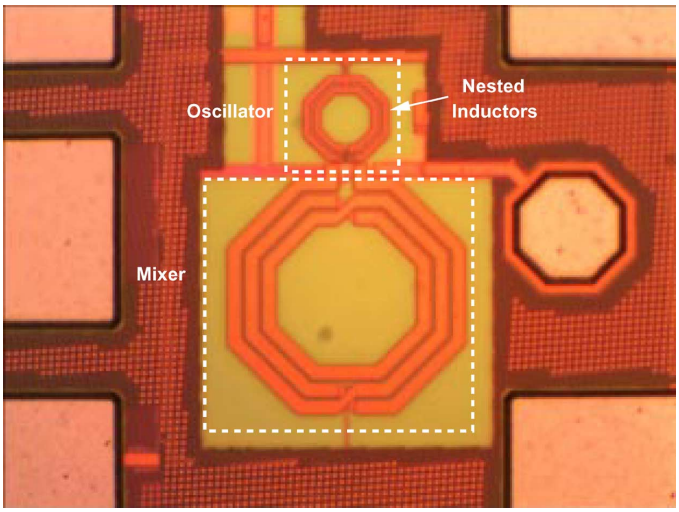

Fig. 13. Oscillator die photo.

the oscillator. In the mixer, $W_{5,6} = 0.4\ \mu$m, $W_7 = 5\ \mu$m, and $L_1 = L_2 = 500$ pH.

To determine which harmonic of f_{ext} produces the observed IF, f_{ext} is varied by Δf and the change in IF, ΔIF, is measured. The ratio $\Delta\text{IF}/\Delta f$ gives the harmonic order.

V. Experimental Results

The oscillator prototypes have been fabricated in TSMC's 65-nm CMOS technology. Fig. 13 shows the active oscillator die area, which measures approximately 100 μm $\times$ 200 μm. The nested inductors are shown on top and the mixer load on the bottom.

Two sets of measurements have been carried out. In the first set, the prototypes are mounted on a probe station, an external W-band input is applied to the mixer, and the IF output is displayed on a spectrum analyzer. Fig. 14 shows an example with $f_{ext} = 88.7$ GHz and $n = 3$, revealing oscillation at 300.5 GHz. (The sign of Δf determines whether f_{osc} is equal to $f_{ext}+nf_{IF}$ or $f_{ext}-nf_{IF}$.) The slight supply dependence of f_{osc} helps distinguish the desired output from other mixing components and also proves that the oscillator is not injection-locked to the external input. Inspection of other parts of the IF spectrum shows that the measured IF components indeed correspond to the *first* harmonic.

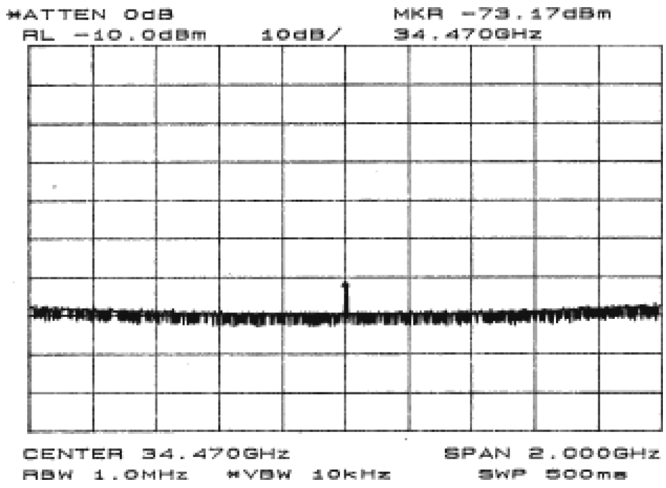

Fig. 14. IF spectrum measured with $f_{ext} = 88.7$ GHz.

In the second set, the output radiated by the prototypes is sensed by an FFT spectrometer [15] and the spectrum is constructed. Depicted in Fig. 15, the results agree with those of the first set, confirming that the mixer measurements have sensed the fundamental and not a higher harmonic.

Fig. 16 plots the simulated and measured oscillation frequencies of theprototypes. It is interesting that the intrinsic BSIM4 capacitances are relatively accurate for frequencies approaching $f_{\max}$. Table I summarizes the fundamental frequencies reported recently in CMOS technology.

VI. Conclusion

Fundamental oscillators can provide quantitative insight into the speed limitation of IC technologies. This paper has demonstrated the potential of the buffer-feedback oscillator for high-frequency operation. It is shown that the losses due to the inductors, gate resistance, and the output resistance become significant at very high frequencies, making it desirable to "distribute" them on multiple nodes—the distinguishing factor between the XCO and the BFO. Measurements indicate oscillation frequencies from 205 GHz to 300 GHz in 65-nm CMOS technology.

Appendix I

Consider the cross-coupled pair equivalent circuit shown in Fig. 17. We have

$$Y_X(s) = \frac{R_G C_{GS} C_{GD} s^2 + [C_{GS} + (4 + g_m R_G) C_{GD}]\, s - g_m}{2\,[R_G (C_{GS} + C_{GD}) s + 1]} \tag{18}$$

and hence

$$Re\{Y_X\} = \frac{-g_m + R_G \omega^2 \left[C_{GS}^2 + (4 + g_m R_G) C_{GD} (C_{GS} + C_{GD})\right]}{2\,[1 + R_G^2 (C_{GS} + C_{GD})^2 \omega^2]} \tag{19}$$

$$Im\{Y_X\} = \frac{2(2 + g_m R_G) C_{GD} + (1 + g_m R_G) C_{GS} + R_G^2 (C_{GS} + C_{GD}) C_{GS} C_{GD} \omega^2}{2\,[1 + R_G^2 (C_{GS} + C_{GD})^2 \omega^2]} \omega. \tag{20}$$

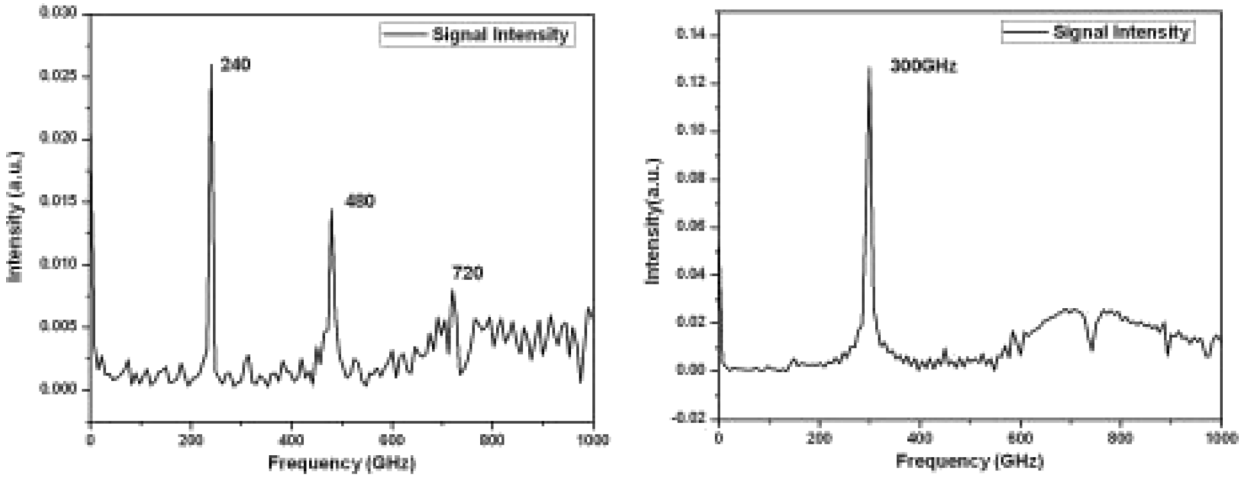

Fig. 15. Spectra obtained by a spectrometer for the (a) 240-GHz and (b) 300-GHz prototypes.

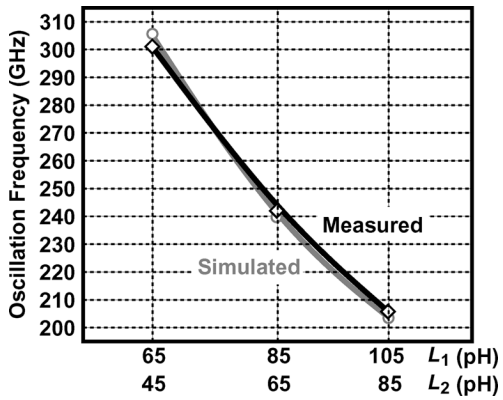

Fig. 16. Simulated and measured oscillation frequencies of the prototypes.

TABLE I
RECENT FUNDAMENTAL OSCILLATION FREQUENCIES OBTAINED IN CMOS TECHNOLOGY

	Fundamental Frequency	Power Dissipation	CMOS Technology
[13]	81 GHz	12 mW	90 nm
[15]	205 GHz	7 mW	45 nm
[19]	218 GHz	16.8 mW	65 nm
This Work	300 GHz	3.7 mW	65 nm

If $R_G^2(C_{GS}+C_{GD})^2\omega^2 \ll 1$, then

$$Re\{Y_X\} \approx -\frac{g_m}{2} + R_G\omega^2\frac{C_{GS}^2+(4+g_mR_G)C_{GD}(C_{GS}+C_{GD})}{2} \quad (21)$$

i.e., $Re\{Y_X\}$ consists of a negative resistance of $-2/g_m$ in parallel with a positive resistance equal to $2/(R_GC_{GS}^2\omega^2)$

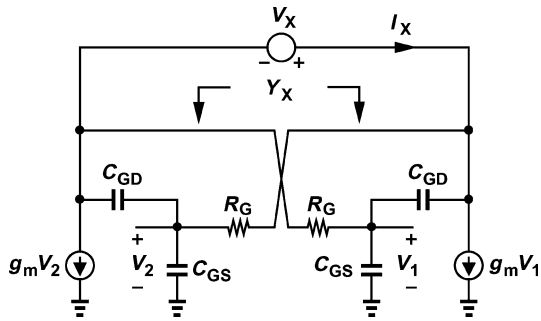

Fig. 17. Equivalent circuit of cross-coupled pair including gate-drain capacitance.

and another positive resistance equal to $2/[R_G\omega^2(4+g_mR_G)C_{GD}(C_{GS}+C_{GD})]$. Moreover,

$$Im\{Y_X\} \approx \frac{2(2+g_mR_G)C_{GD}+(1+g_mR_G)C_{GS}+R_G^2(C_{GS}+C_{GD})C_{GS}C_{GD}\omega^2}{2}\omega. \quad (22)$$

as if C_{GS} were enlarged by a factor of $1+g_mR_G$ and C_{GD} by a factor of $(2+g_mR_G)$, with an additional capacitance equal to $[R_G^2(C_{GS}+C_{GD})C_{GS}C_{GD}]/2$.

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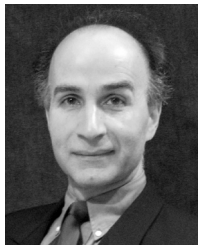
REFERENCES

[1] M. Banu, "MOS oscillators with multi-decade tuning range and gigahertz maximum speed," *IEEE J. Solid-State Circuits*, vol. 23, pp. 474–479, Apr. 1988.
[2] B. Razavi *et al.*, "A 3-GHz 25-mW CMOS phase-locked loop," in *Dig. of Symposium on VLSI Circuits*, Jun. 1994, pp. 131–132.

[3] M. Soyuer *et al.*, "A 3-V 4-GHz nMOS voltage-controlled oscillator with integrated resonator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2042–2045, Dec. 1996.
[4] B. Kleveland *et al.*, "Monolithic CMOS distributed amplifier and oscillator," in *ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 70–71.
[5] H. Wang, "A 50-GHz VCO in 0.25- μm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 372–373.
[6] L. Franca-Neto, R. Bishop, and B. Bloechel, "64 GHz and 100 GHz VCOs in 90 nm CMOS using optimum pumping method," in *ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 444–445.
[7] E. Seok *et al.*, "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 472–473.
[8] B. Razavi, "A 300-GHz fundamental oscillator in 65-nm CMOS technology," in *Symposium on VLSI Circuits Dig. of Tech. Papers*, Jun. 2010, pp. 113–114.
[9] S. P. Voinigescu *et al.*, "CMOS SOCs at 100 GHz: System architectures, device characterization, and IC design examples," in *Proc. ISCAS*, May 2007, pp. 1971–1974, and presentation slides.
[10] B. Razavi, "Multi-decade carrier generation for cognitive radios," in *VLSI Circuits Symp. Dig. Tech. Papers*, Jun. 2009, pp. 120–121.
[11] B. Catli and M. M. Hella, "A 1.94 to 2.55 GHz, 3.6 to 4.77 GHz tunable CMOS VCO based on double-tuned, double-driven coupled resonators," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2463–2477, Sep. 2009.
[12] B. Razavi and J. Sung, "A 6-GHz 60-mW BiCMOS phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1560–1565, Dec. 1994.
[13] D. Huang *et al.*, "A 324 GHz CMOS frequency generator using a linear superposition technique," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 476–477.
[14] B. Catli and M. Hella, "Triple-push operation for combined oscillation/division functionality in millimeter-wave frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1575–1589, Aug. 2010.
[15] E. Seok *et al.*, "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 472–473.
[16] B. Razavi, R. H. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits and Systems—Part I*, pp. 750–754, Nov. 1994.
[17] B. Razavi, "Cognitive radio design challenges and techniques," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1542–1553, Aug. 2010.
[18] C. K. Liang and B. Razavi, "Systematic transistor and inductor modeling for millimeter-wave design," *IEEE J. Solid-State Circuits*, vol. 44, pp. 450–457, Feb. 2009.
[19] Q. Gu *et al.*, "Generating terahertz signals in 65 nm CMOS with negative-resistance resonator boosting and selective harmonic suppression," in *Symposium on VLSI Circuits Dig. of Tech. Papers*, Jun. 2010, pp. 109–110.



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