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The Bridged T-Coil

The bridged T-coil, often simply called the T-coil, is a circuit topology that extends the bandwidth by a greater factor than does inductive peaking. Many high-speed amplifiers, line drivers, and input/output (I/O) interfaces in today's wireline systems incorporate on-chip T-coils to deal with parasitic capacitances. In this article, we introduce and analyze the basic structure and study its applications.

Brief History

The T-coil circuit can be traced back to the 1948 classic paper on distributed amplifiers by Ginzton et al. [1]. The authors call the structure the "bridged-tee connection" and present it along with its equivalent circuits, as shown in Figure 1.

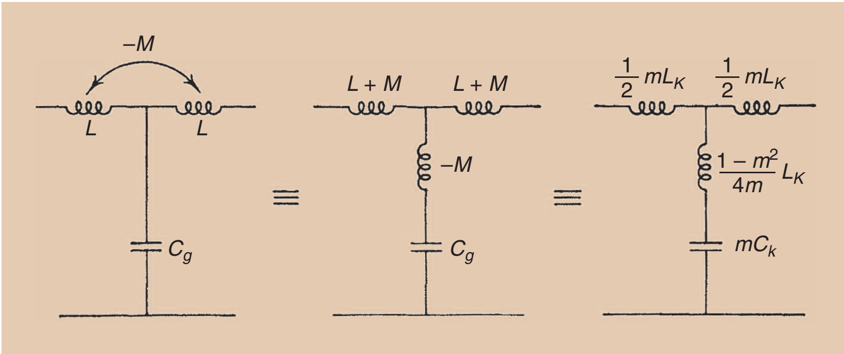

FIGURE 1: A bridged T-coil circuit described by Ginzton et al. in 1948 [1].

The use of T-coils for bandwidth enhancement was pioneered by Tektronix engineers in the late 1960s [2]. The need for fast "vertical" amplifiers for the front end of oscilloscopes had led to many new wide-band circuit techniques, and Tektronix designers saw the significant advantage of T-coils. The instrumentation manufacturer guarded the design details of T-coil circuits as a trade secret for many years [2]. It was only in 1990 that Dennis Feucht, a former Tektronix engineer, provided the T-coil design equations in his book [3].

The early T-coil implementations were based on discrete, off-chip inductors or transformers, suffering from board parasitics, bond wire inductances, and unwanted couplings to and from other signals. A few integrated GaAs realizations appeared in the late 1980s and early 1990s [4], [5]. With the RF circuits revolution in the 1990s and the tremendous work on integrated inductors, the T-coil was bound to find its way to CMOS chips as well. Of course, the finite Q and parasitic capacitances of on-chip structures would introduce new issues. Moreover, a well-defined coupling factor would need to be created between two spiral inductors. In 2003, two papers described the design of integrated T-coils and their use in broadband drivers [6] and electrostatic discharge (ESD) protection circuits [7].

Basic Idea

The bridged T-coil is a special case of two-port bridged-T networks. It consists of two mutually coupled inductors and a bridge capacitor (Figure 2). The coupling polarity matters and the two inductances are commonly chosen to be equal. With certain loads attached to this circuit, the impedance seen at node 1 or 2 and the transfer function from either of these nodes to node 3 present interesting properties.

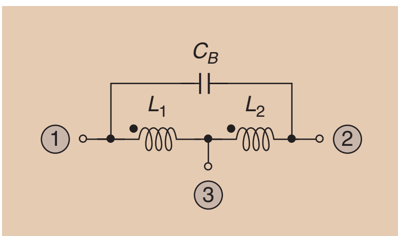

FIGURE 2: A basic bridged T-coil structure.

As an example, consider the simple common-source stage shown in Figure 3(a) with a load capacitance C_L. At high frequencies, the small-signal drain current of M_1 is shunted by C_L, causing $|V_{out}|$ to fall. We can place an inductor in series with R_D [Figure 3(b)] so that the series impedance of R_D and L_D increases with frequency, thereby forcing a greater current through C_L and lessening the gain roll-off. Alternatively, we can insert a T-coil circuit in the signal path as illustrated in Figure 3(c). We are interested in the transfer function V_{out}/V_{in} and its behavior as a function of component values.

The transfer function can be derived using the extra element theorem [8] or the Δ-Y transformation [9] and is as follows:

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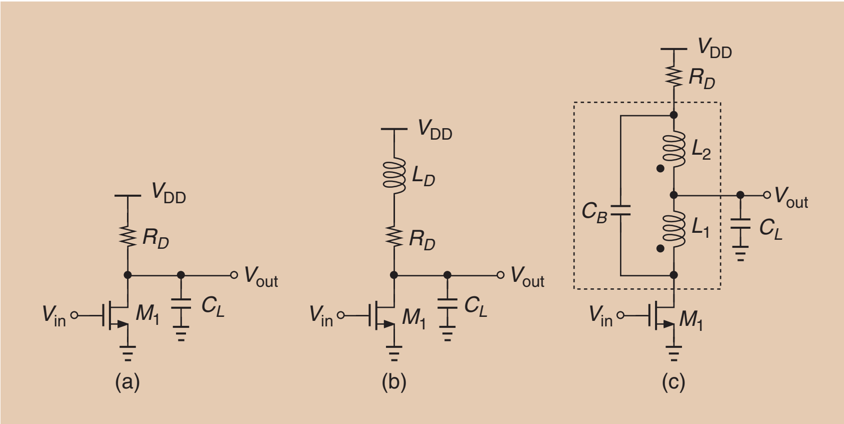

FIGURE 3: A common-source stage with (a) a simple resistive load, (b) inductive peaking, and (c) T-coil peaking.

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \times \frac{a_2 s^2 + a_1 s + 1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1}, \quad (1)$$

where

$$a_2 = (L_1 + L_2 + 2M)\,C_B \quad (2)$$
$$a_1 = (L_2 + M)/R_D \quad (3)$$
$$b_4 = C_B C_L (L_1 L_2 - M^2) \quad (4)$$
$$b_3 = C_B C_L R_D (L_1 + L_2 + 2M) \quad (5)$$
$$b_2 = C_B (L_1 + L_2 + 2M) + C_L L_2 \quad (6)$$
$$b_1 = R_D C_L. \quad (7)$$

Here, M denotes the mutual inductance between L_1 and L_2 with the polarity shown in Figure 3(c). This transfer function does not offer much intuition but a special case thereof is more mathematically manageable and practically attractive. We assume $L_1 = L_2 = L$ and choose the values such that the zeros in (1) are canceled by two of the poles. As shown in [8], this can be accomplished if two conditions hold, namely,

$$\frac{C_B}{C_L} = \frac{1}{4}\,\frac{1-k}{1+k}, \quad (8)$$

where k is the coupling factor and equal to $M/\sqrt{L_1 L_2} = M/L$, , and

$$\frac{k}{1+k} C_L = \frac{(1+k)L}{R_D^2} - 2C_B. \quad (9)$$

The resulting second-order transfer function assumes the form [8]

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -g_m R_D \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \quad (10)$$

where

$$\omega_n^2 = \frac{2}{(1-k)LC_L} \quad (11)$$
$$\zeta = \frac{R_D C_L - (1+k)L/R_D}{\sqrt{2(1-k)LC_L}}. \quad (12)$$

For design purposes, we select a value for the damping factor, ζ, and wish to determine the other circuit parameters. Solving the above equations, [8] finds that

$$L_1 = L_2 = \frac{R_D^2 C_L}{4}\left(1 + \frac{1}{4\zeta^2}\right) \quad (13)$$
$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \quad (14)$$
$$C_B = \frac{C_L}{16\zeta^2}, \quad (15)$$

which agree with those in [3]. It is interesting to note that ζ increases with k, i.e., a tighter coupling translates to a more damped response.

Bandwidth Advantage

As mentioned above, the bridged T-coil improves the speed to a greater extent that does inductive peaking. We formulate this advantage by considering the 3-dB bandwidths in the two cases. From (10), the T-coil bandwidth is expressed as

$$\omega_{BW,T-\text{coil}}^2 = \left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 1}\,\right]\omega_n^2 \quad (16)$$
$$= \left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 1}\,\right] \times \frac{2}{(1-k)LC_L}. \quad (17)$$

We replace k from (14) and L from (13), obtaining

$$\omega_{BW,T-\text{coil}}^2 = 4\zeta\left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2+1}\,\right]\frac{1}{R_D C_L}. \quad (18)$$

For example, if $\zeta = \sqrt{2}/2$, then $\omega_{BW,T-\text{coil}}^2 = 2\sqrt{2}/(R_D C_L) \approx 2.83/(R_D C_L)$. Remarkably, the T-coil multiplies the original bandwidth by a factor of 2.83. By comparison, the inductively peaked stage of Figure 3(b) exhibits a bandwidth of approximately $1.8/(R_D C_L)$ for $\zeta = \sqrt{2}/2$. (A more accurate comparison should take the time-domain overshoot into account as well.)

ESD Protection

In addition to broadening the bandwidth, T-coils can also create a constant, resistive input impedance in the presence of a heavy load capacitance, a situation commonly encountered in ESD protection circuits. For example, in the input network shown in Figure 4(a), where R_T is a termination resistor, the ESD device capacitance, C_{ESD}, degrades the input matching, thus causing reflections. On the other hand, if a bridged T-coil is inserted as shown in Figure 4(b), Z_{in} can be made equal to R_T at *all* frequencies [7]. We can intuitively see

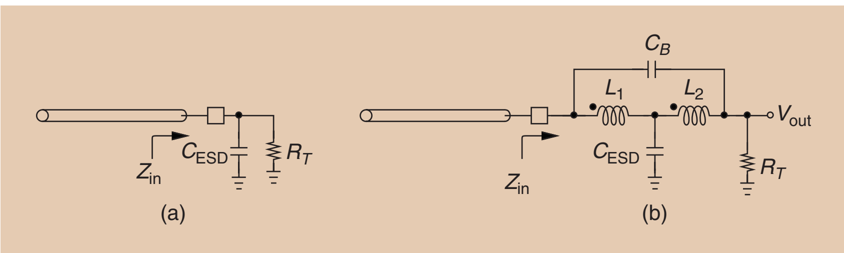

FIGURE 4: (a) An input network with an ESD device and (b) an input network using a T-coil for broadband matching.

this property at the two extremes: at very low frequencies, L_1 and L_2 short R_T to the input, and at high frequencies, C_B does the same. It can be proved that $Z_{\text{in}} = R_T$ at all frequencies if $L_1 = L_2$ and the pole-zero cancellations leading to (10) also hold. In other words, the conditions stipulated by (13)–(15) apply here as well.

An intuitive argument can explain why the T-coil network cannot have zeros in this case. If the circuit does contain a zero, then Z_{in} must still be equal to the termination resistance at the zero frequency, s_z. Now suppose we drive the circuit of Figure 3(c) with an input of the form $\exp(s_z t)$, obtaining $V_{\text{out}} = 0$. Thus, C_L can be removed. In other words, at $s = s_z$, the drain load reduces to R_D in series with the parallel combination of C_B and $L_1 + L_2 + 2M$. This combination cannot have a zero impedance at $s \neq 0$ and hence $Z_{\text{in}} \neq R_D$.

Output drivers using ESD protection can benefit from T-coils in a similar manner. Shown in Figure 5, such an arrangement assumes an infinite output impedance for the driver stage and presents a resistance equal to R_T to the outside world. If the output impedance, R_{out}, is not sufficiently high, a small resistance, R_2, can be placed in series with L_2 to compensate for its effect [10], [7]. This resistance is given by $R_T/(R_{\text{out}}/R_T - 1)$.

T-Coil Implementation

In the special case where $L_1 = L_2$, the inductors lend themselves to a simple implementation in the form of a symmetric spiral [Figure 6(a)] [7]. Here, the line spacing is chosen to yield the desired mutual coupling, and the outer dimension and the number of turns to provide the required inductance. To include the parasitic resistances and capacitances of the spiral in simulations, a distributed model can be constructed as shown in Figure 6(b). Note that the interwinding capacitance is also taken into account. As a first-order approximation, this capacitance appears between E and F and can be subtracted from the bridge capacitance, C_B.

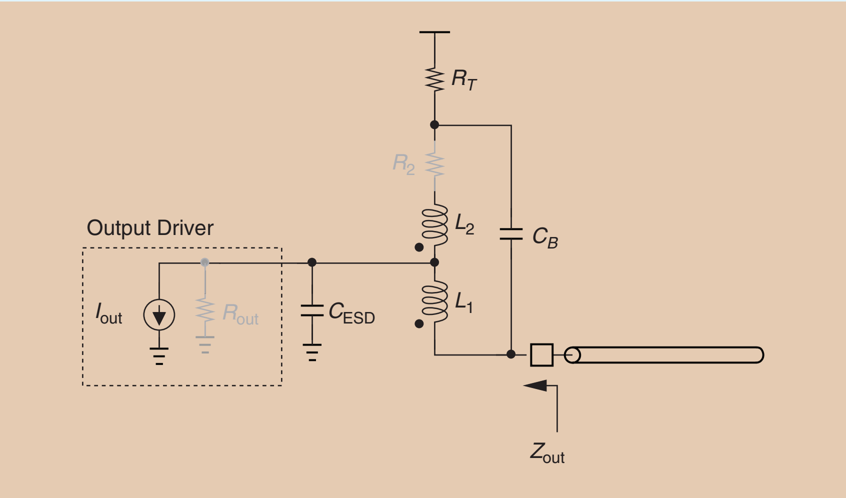

FIGURE 5: An output driver using a T-coil.

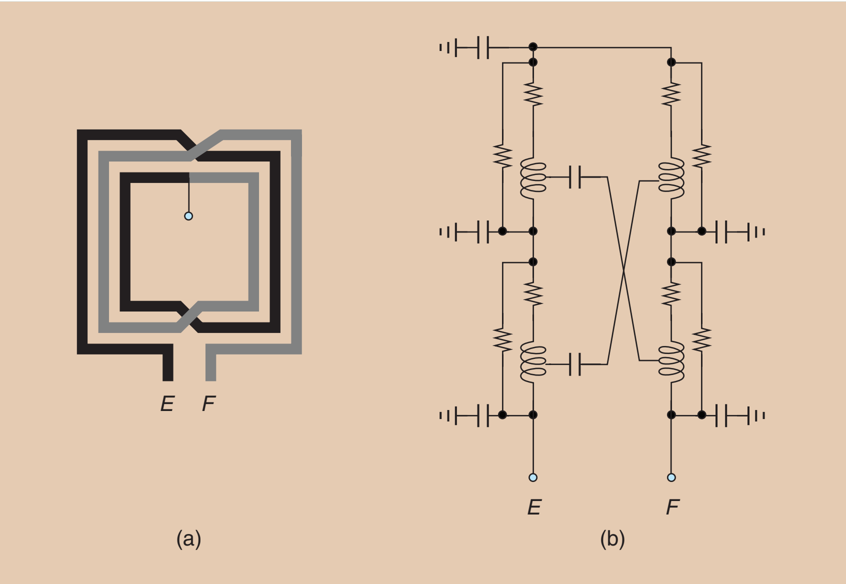

FIGURE 6: (a) The implementation of T-coil and (b) a distributed model for circuit simulations.

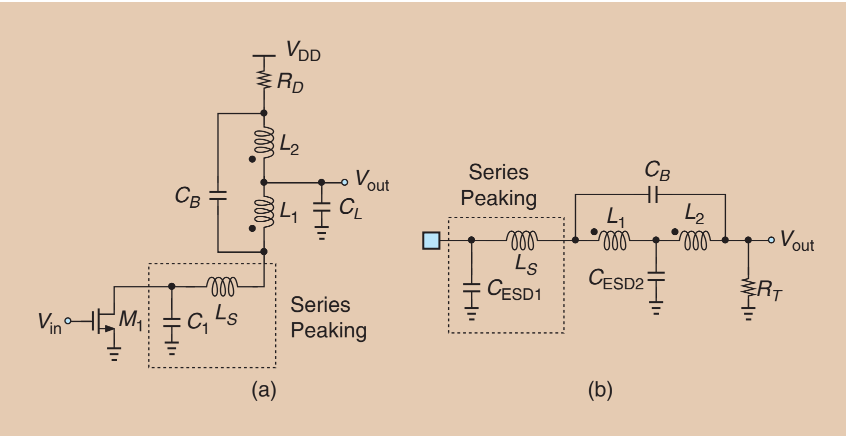

FIGURE 7: The use of series peaking and T-coils in (a) a gain stage with a high output capacitance and (b) an input network with high ESD capacitance.

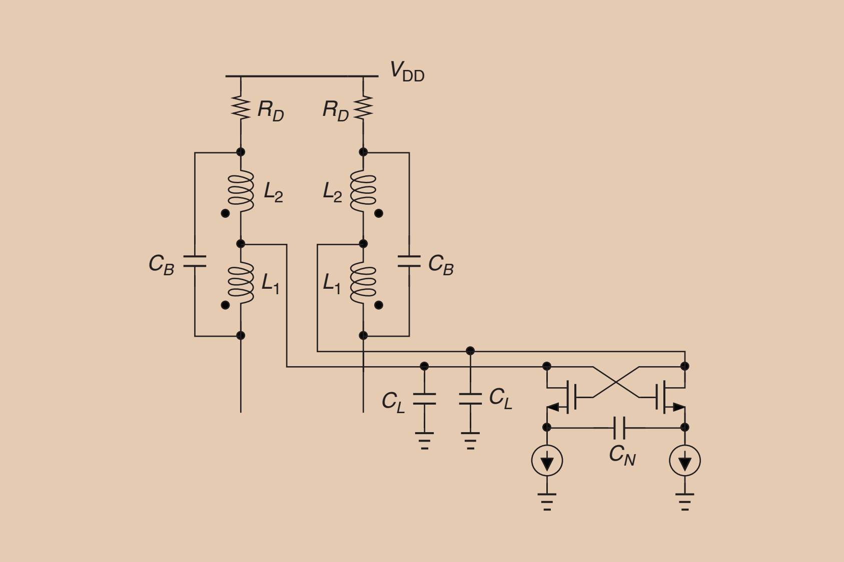

FIGURE 8: The addition of a negative capacitance generator to T-coil network.

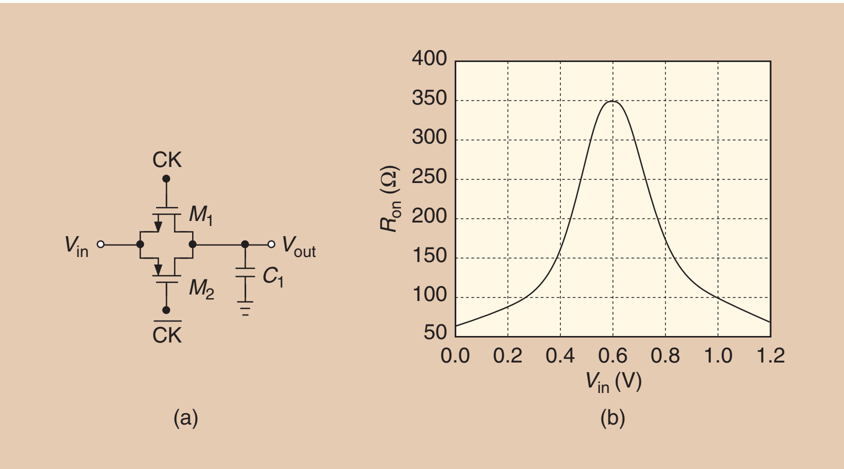

FIGURE 9: The on-resistance of complementary switches as a function of input voltage.

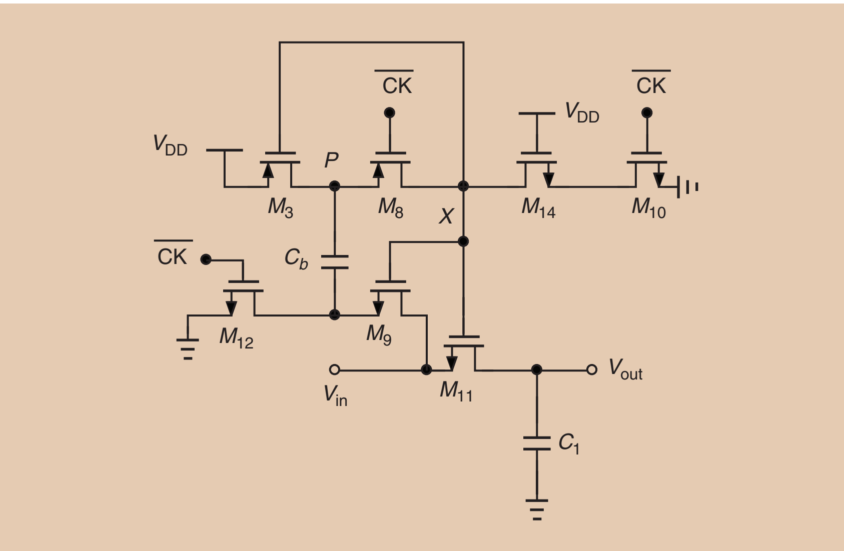

FIGURE 10: A bootstrap circuit.

Combination with Other Techniques

The bridged T-coil network can be combined with other high-speed topologies so as to achieve greater bandwidths. For example, since the input impedance of the second-order T-coil circuit is constant, one can readily add series peaking in the input signal path. Illustrated in Figure 7, this combination proves useful in two cases: 1) if a stage incorporates a large transistor [Figure 7(a)], suffering from a high output capacitance, C_1, or 2) if an input network must accommodate a large ESD capacitance [Figure 7(b)], in which case both capacitors can represent ESD devices. Series peaking can also be applied to output networks such as that in Figure 5.

Differential circuits can combine T-coils with other differential techniques. For example, as shown in Figure 8, a negative capacitance generator using a cross-coupled pair can be added in parallel with the load capacitance [6], thereby improving the overall speed. To avoid significant overshoot in the time response, we choose $C_N \approx C_B/4$.

Questions for the Reader

1) Use a power dissipation argument to determine the transfer function of the circuit shown in Figure 4(b).
2) In Figure 7(a), how should L_S be chosen if the damping factor of the series peaking network must remain around $\sqrt{2}/2$?

Answers to Last Issue's Questions

1) In Figure 9, we write $R_{on} = R_0 + R_1 \cos 2\omega_{in} t + R_2 \cos 4\omega_{in} t + \cdots$ and assume $R_1 \approx R_0$. Suppose we define the small-signal bandwidth of the sampler as $\omega_{3dB} = (R_0 C_1)^{-1}$. Determine the ratio of ω_{in} to this bandwidth if the third-order distortion given by $R_1 C_1 \omega_{in}/2$ must remain lower than −60 dB. This example demonstrates the severity of the variable on-resistance.

   For the distortion to remain below −60 dB, we must have $R_1 C_1 \omega_{in}/2 < 10^{-3}$. Replacing $R_1 C_1 \approx R_0 C_1$ with $1/\omega_{3dB}$, we have $\omega_{in}/\omega_{3dB} < 1/500$. This example shows that the sampler's small-signal bandwidth must be far greater than the input frequency.

2) To which node(s) should the n-wells of M_3 and M_8 in Figure 10 be connected?

They should be connected to node P to ensure the source and drain junctions of these transistors are not forward biased.

3) How high can V_X in Figure 10 go to avoid stressing M_{14}?

When M_{14} is off, its source voltage reaches approximately $V_{DD} - V_{TH}$. For the source-drain potential difference to remain less than V_{DD}, V_X must not exceed $2V_{DD} - V_{TH}$.

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EDITOR'S NOTE *(Continued from p. 4)*

- Willy Sansen, in "Minimum Power in Analog Amplifying Blocks: Presenting a Design Procedure," answers questions he received from his 2015 ISSCC plenary talk.
- Behzad Razavi continues his column series "A Circuit for All Seasons" by providing an article that discusses the bridged T-coil. This article fits well into this issue's feature of wireline communications due to the use of the T-coil for extending the bandwidth of a circuit.
- Ali Sheikholeslami provides another piece in his well-received series, "Circuit Intuitions." In this issue, he continues discussing Miller's theorem, its uses and shortcomings when analyzing circuits. As usual (and the e-mail we receive would support this), the article provides useful insight into circuit analysis and design.
- Finally, Marcel Pelgrom discusses "The Next Hype" in his column, which is always an entertaining article that provokes thought. It's one of my favorite reads in each magazine issue. I hope you agree!

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CIRCUIT INTUITIONS *(Continued from p. 8)*

This equation, along with equations for f_{p1} and f_z, can now be used to form the equation for the overall voltage transfer function of the two-stage amplifier.

It is worth noting that as we increase C_{12}, f_{p1} and f_{p2} (as found by their respective equations) will move farther apart, a phenomenon referred to as pole splitting [1], [2].

In summary, Miller's approximation uses the dc gain of the amplifier to provide a relatively accurate estimation of its dominant pole (i.e., the circuit bandwidth). This approximation, however, becomes inaccurate when determining the second pole of the amplifier; other intuitive methods exist for this purpose.

For further discussions and intuition into Miller's theorem, we refer the readers to [3].

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