

Design of High-Speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS

Behzad Razavi, *Member, IEEE*, Kwing F. Lee, *Member, IEEE*, and Ran H. Yan

Abstract—Deep submicron CMOS technologies offer the high speed and low power dissipation required in multigigahertz communication systems such as optical data links and wireless products. This paper introduces the design of two communication circuits, namely a 1/2 frequency divider and a phase-locked loop, fabricated in a partially scaled 0.1 μm CMOS technology. Configured as a master-slave circuit, the divider achieves a maximum speed of 13.4 GHz with a power dissipation of 28 mW. The phase-locked loop employs a current-controlled oscillator and a symmetric mixer to operate at 3 GHz with a tracking range of ± 320 MHz, an rms jitter of 2.5 ps, and a phase noise of -100 dBc/Hz while dissipating 25 mW.

I. INTRODUCTION

THE EVER-GROWING popularity of CMOS devices has made them the mainstream technology for designing complex monolithic systems with dense logic, low power dissipation, low supply voltage, and highly automated synthesis. In high-speed applications, however, the relatively low transconductance of MOSFET's often imposes severe speed-power trade-offs, thereby limiting their advantage over silicon bipolar and III-V devices. These trade-offs are nonetheless relaxed as device dimensions scale down, making deep submicron CMOS attractive even for multigigahertz circuits. This can ultimately lead to monolithic integration of communication systems that include high-speed input and output interfaces as well as extensive intermediate signal processing.

This paper describes the design of two high-speed, low-power communication circuits fabricated in a partially scaled 0.1- μm CMOS technology. The first circuit is a 1/2 frequency divider that operates with input frequencies as high as 13.4 GHz while dissipating 28 mW [1]. The second is a phase-locked loop (PLL) achieving a center frequency of 3 GHz with 2.5 ps of rms jitter and 25 mW of power dissipation [2]. Serving as test vehicles to demonstrate the technology's potential, these circuits also find wide application in optical data links, clock recovery, and frequency synthesis. The design style for both circuits has been heavily influenced by the device characteristics and layout rules of the process.

The next section of the paper provides a brief overview of the 0.1 μm CMOS technology and the circuit design issues that arise in using this process. In Section III, the design and

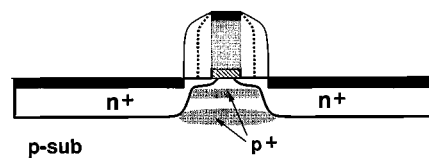


Fig. 1. Cross section of an NMOS device in partially scaled CMOS process.

experimental results of the frequency divider are described, and in Section IV the PLL circuit details and measured performance are presented.

II. TECHNOLOGY OVERVIEW AND DESIGN ISSUES

Scaling MOSFET's to deep submicron dimensions entails many difficulties originating from limitations due to both device physics and fabrication technology. High subthreshold conduction, low-voltage bulk punchthrough, increased gate-source and gate-drain overlap capacitance, and higher gate resistance are undesirable effects that manifest themselves as sub-half micron features are approached. Moreover, definition of device and interconnect lateral dimensions requires increasingly higher precision in lithography and processing steps.

Fig. 1 shows the cross section of an NMOS transistor in our CMOS technology [3]. Employing various processing techniques such as vertical doping engineering, two-step sidewall spacers, and platinum gate silicidation, the technology alleviates the device physics issues mentioned above. Furthermore, to improve the yield and reduce the turnaround time, the first generation of the technology scales only two dimensions: the channel length to 0.1 μm and the gate oxide thickness to 40 Å. The remaining dimensions roughly correspond to a typical 1 μm process, yielding a minimum source/drain area of 2.2 $\mu\text{m} \times 2.2 \mu\text{m}$ [Fig. 2(a)].

Since the contribution of source/drain junction capacitance is substantial, the regular structure of Fig. 2(a) does not take full advantage of the drive capability provided by partial scaling. To resolve this issue, ring-shaped transistors such as that in Fig. 2(b) can be used. In this geometry, the ratio of the equivalent width and the drain junction capacitance is approximately four times that of Fig. 2(a). Also, the effect of distributed gate resistance is reduced, an important issue in wide, short-channel MOSFET's [4].

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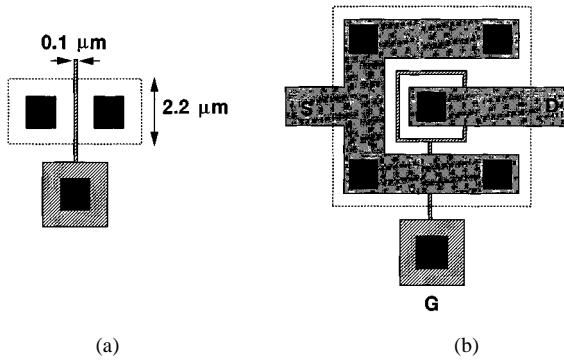


Fig. 2. MOS device structures, (a) regular, (b) ring-shaped.

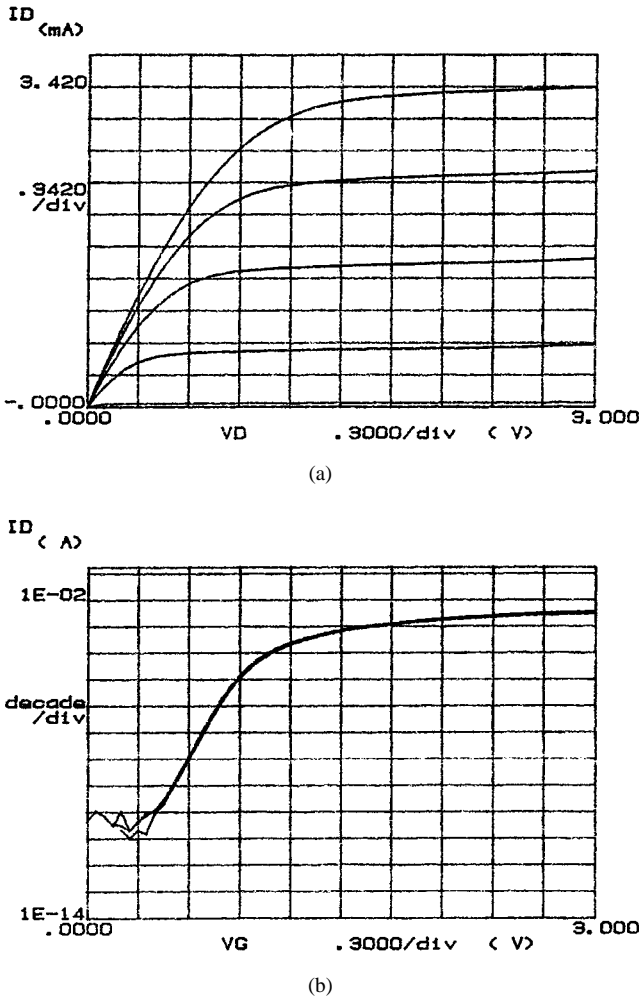


Fig. 3. Ring-shaped NMOS device characteristics, (a) I_D versus V_{DS} (V_{GS} from 0 to 3 V in 0.5 V steps), (b) I_D versus V_{GS} (V_{DS} from 1 V to 3 V in 1 V steps).

Figs. 3 and 4 depict the measured IV characteristics of ring-shaped NMOS and PMOS devices with drawn dimensions $W/L = 8.8 \mu\text{m}/0.1 \mu\text{m}$. We note that $V_{\text{THN}} = 850 \text{ mV}$, $V_{\text{THP}} = 500 \text{ mV}$, and the NMOS and PMOS subthreshold slopes are 85 mV/dec and 90 mV/dec, respectively. While the devices and circuits have been successfully characterized for supply voltages as high as 3 V, long-term reliability issues such as hot electron effects and gate tunneling currents typically limit the operating voltage to approximately 2 V.

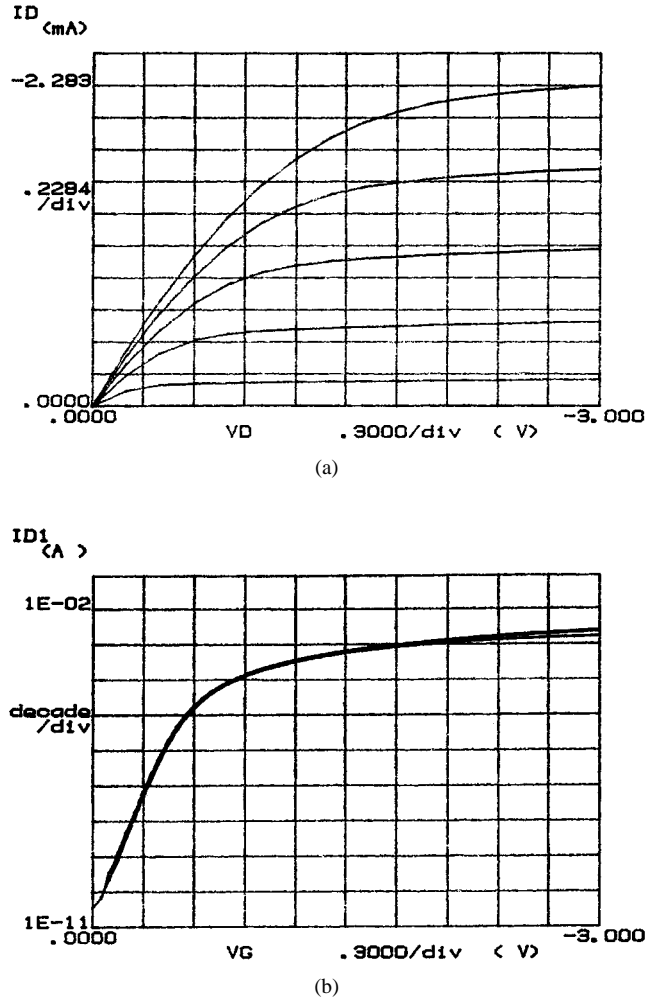


Fig. 4. Ring-shaped PMOS device characteristics, (a) I_D versus V_{DS} (V_{GS} from 0 to -3 V in 0.5 V steps), (b) I_D versus V_{GS} (V_{DS} from -1 V to -3 V in 1 V steps).

Since the ring-shaped geometry of Fig. 2(b) suffers from a large source junction capacitance, it proves beneficial if only the drain terminal appears in the critical signal path. Thus, circuit topologies such as pass transistors or stacked devices cannot be used efficiently. This observation can be summarized as a design constraint for circuits using ring-shaped structures: no path from high-speed nodes to the supply rails may include series devices. In addition, it is desirable to avoid the gate-channel capacitance of PMOS transistors in the critical path because the trade-off between their transconductance and input capacitance limits the maximum achievable speed.

The principal challenge in designing the circuits described here has been to develop topologies that perform the required functions while complying with the above constraints.

III. FREQUENCY DIVIDER

A. Architecture

The $1/2$ frequency divider employs two D -latches in a master-slave configuration with negative feedback. In high-

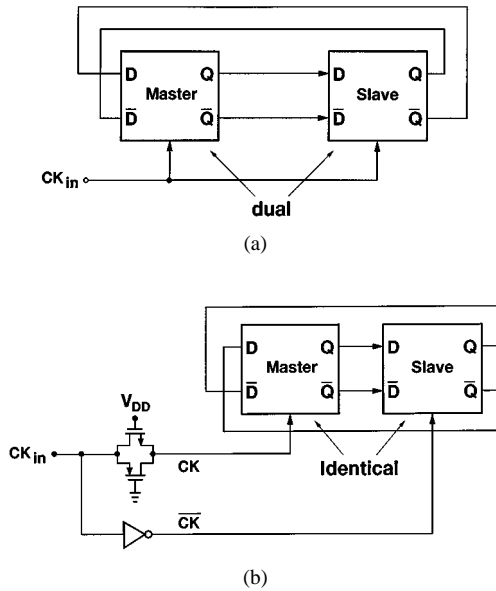


Fig. 5. Master-slave dividers with, (a) single clock, (b) complementary clocks.

speed master-slave dividers, it is common practice to design the slave as the “dual” of the master [Fig. 5(a)] so that they can be both driven by a single clock [5]. However, duality requires one of the latches to incorporate PMOS devices in the signal path, hence lowering the maximum speed. To avoid this difficulty, as shown in Fig. 5(b), the divider utilizes two identical D -latches that are driven by complementary clocks CK and \bar{CK} . In order to minimize the skew between CK and \bar{CK} , the noninverted phase is delayed by means of a complementary pass gate having devices identical with those in the master. Although the skew increases as the input transition time becomes comparable with the period, simulations indicate that it is less than 10 ps for a 13 GHz sinusoidal input. Note that the pass gate used here is not in the divider loop and hence does not violate the constraint described in Section II. The capacitance seen at the input of this gate simply contributes latency to the circuit.

B. Circuit Details

Fig. 6 depicts the divider circuit. Each latch consists of two sense devices (M_1 and M_2 in the master and M_7 and M_8 in the slave), a regenerative loop (M_3 and M_4 in the master and M_9 and M_{10} in the slave), and two pull-up devices (M_5 and M_6 in the master and M_{11} and M_{12} in the slave). When CK is high, M_5 and M_6 are off and the master is in the sense mode, while M_{11} and M_{12} are on and the slave is in the store mode. When CK goes low, the reverse occurs. Note that the circuit uses no stacked or pass transistors. Also, the gate-channel capacitance of the PMOS transistors hardly affects the critical path because these devices are (velocity) saturated almost for the entire voltage swing at nodes X_1 , Y_1 , X_2 , and Y_2 . (At maximum speed, these swings are not rail-to-rail.)

In contrast with conventional latch topologies, the D -latch circuit used in this divider does *not* disable its input devices when it goes from the sense mode to the store mode. While this would pose timing problems in a general digital circuit,

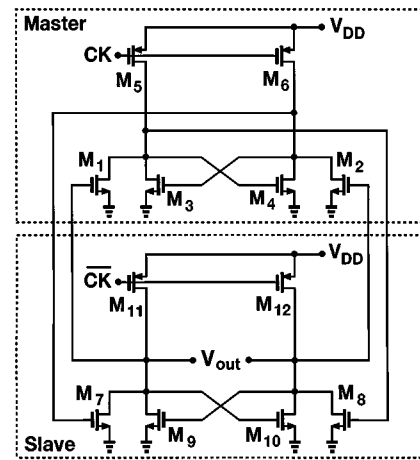


Fig. 6. Divider circuit.

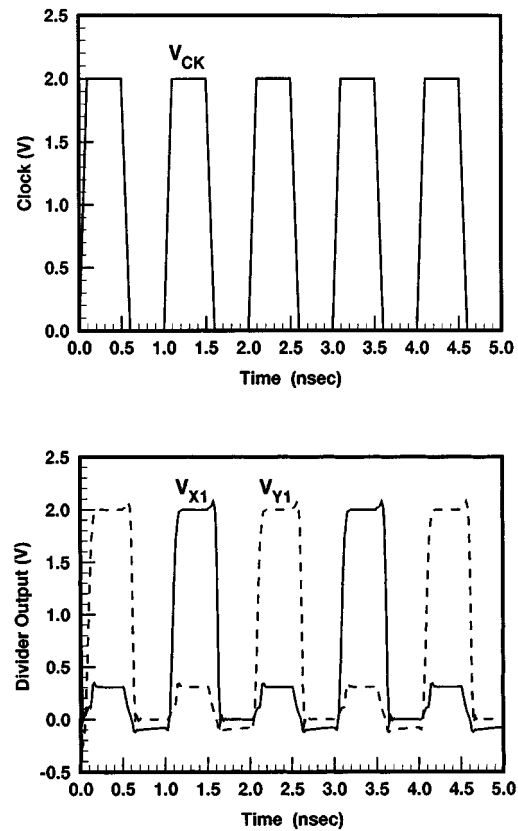


Fig. 7. Divider simulated waveforms.

it does not prevent the divider from functioning properly. To explain the reason, we make two observations. First, since the input devices of each latch are N -type, they can change the state only if one of the inputs goes from low to high (and the other from high to low). Second, when each latch is in the sense mode, neither of its outputs can go from low to high because the PMOS pull-up devices are off. Thus, if, for example, the master is in the sense mode and the slave in the store mode, the master's outputs can only go from high to low and hence cannot override the state stored in the slave.

Shown in Fig. 7 are the divider's simulated waveforms at 1 GHz clock frequency. When the PMOS devices are on, they

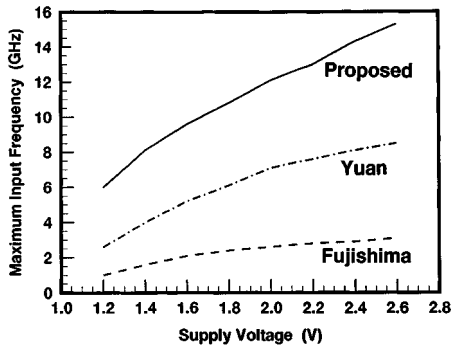


Fig. 8. Simulated speed of three divider topologies versus supply voltage.

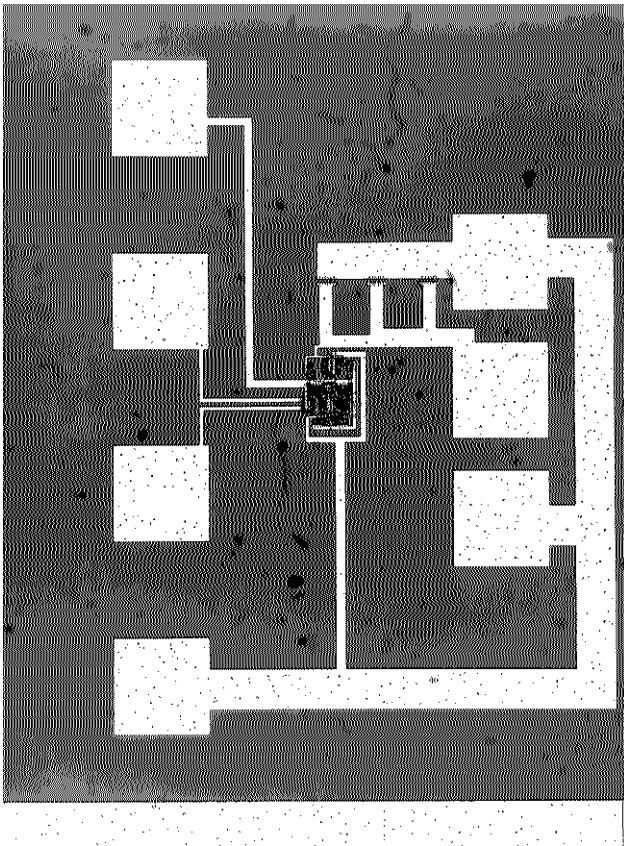


Fig. 9. Divider die photograph.

slightly degrade the logic low level and also provide a current path from V_{DD} to ground, thereby dissipating static power. Note that in the sense mode, both outputs of each latch are low, one being pulled low by an input device and the other maintaining a low state from the previous cycle.

Using simulations based on our CMOS device models, we have compared the performance of the proposed divider topology with that of two high-speed dividers reported in [5] and [6]. Plotted in Fig. 8 is the maximum clock frequency of each circuit, f_{max} , as a function of supply voltage, indicating at least a factor of two improvement in speed. The higher speed of the proposed divider is due to the strong positive feedback in each latch as well as fewer stages in the critical signal path. Note that if regular, rather than ring-shaped, devices are used here, the speed decreases by approximately 20%.

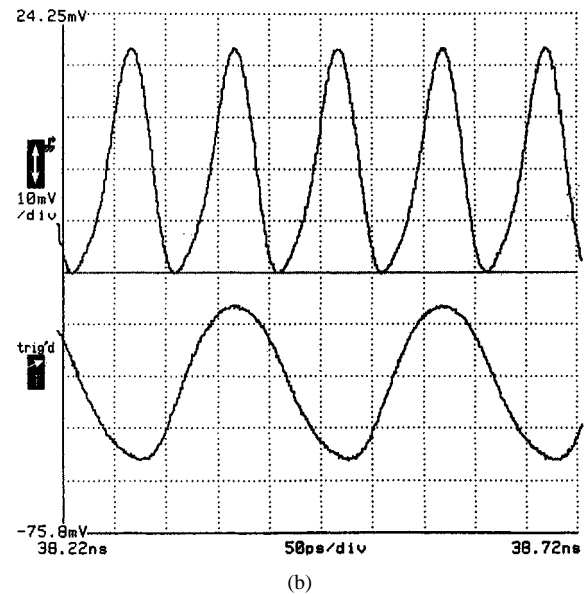
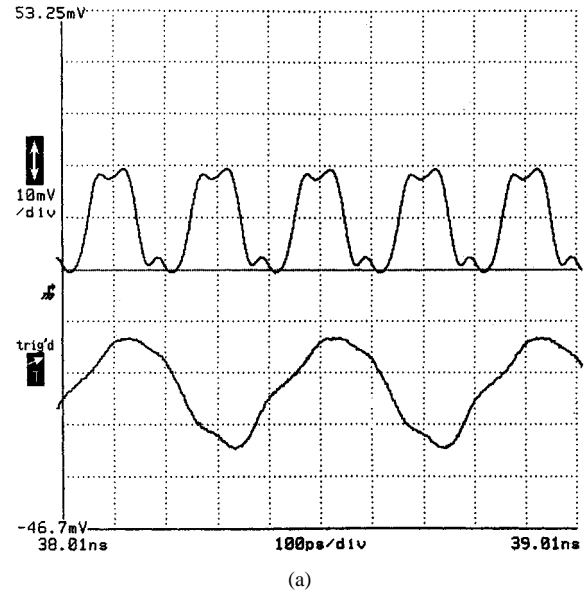


Fig. 10. Measured divider input/output waveforms for (a) $f_{in} = 5$ GHz, (b) $f_{in} = 10$ GHz.

C. Experimental Results

The divider has been fabricated in our $0.1 \mu\text{m}$ CMOS technology. Fig. 9 shows a photograph of the die, whose active area measures approximately $50 \mu\text{m} \times 70 \mu\text{m}$. For input termination, three n -well resistors are used in parallel so that they can be disconnected one by one to provide an approximate value of 50Ω . The circuit has been tested on wafer (at room temperature) using a high-speed Picoprobe to apply the input and a Cascade multicontact probe to measure the output as well as provide power and ground connections. No attempt has been made to generate large output swings off the chip as the setup provides sufficiently high signal-to-noise ratio, allowing direct measurement of amplitudes in the millivolt range. The output stage of the circuit is simply a $3 \mu\text{m}/0.1 \mu\text{m}$ NMOS transistor driving a 50Ω load.

Shown in Fig. 10(a), (b), and (c) are the measured input and output waveforms of the divider at $f_{in} = 5, 10, \text{ and } 13.4$ GHz,

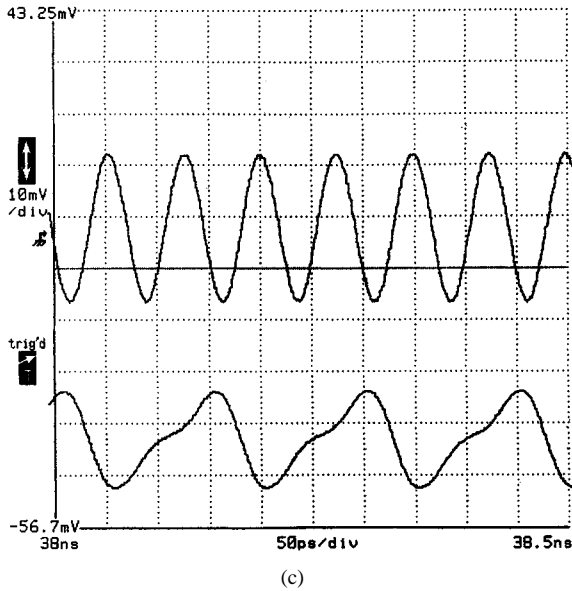
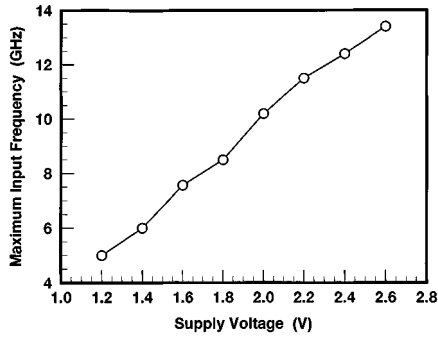

 Fig. 10. Continued (c) $f_{in} = 13.4$ GHz (input amplitude not to scale).


Fig. 11. Measured divider speed versus supply voltage.

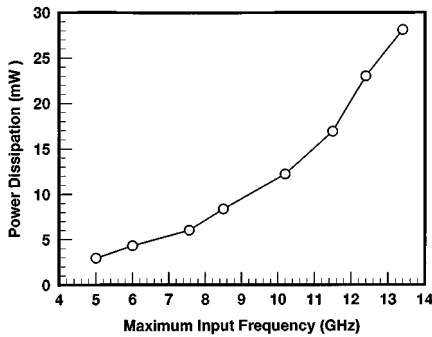


Fig. 12. Divider power-speed trade-off.

respectively. In this measurement, the supply voltage is 2.6 V and the input amplitude is rail-to-rail. For $f_{in} > 13.4$ GHz, the circuit begins to miss pulses and divides by three.

In order to assess the low-voltage performance of the circuit, the supply voltage was varied from 1.2 to 2.6 V, yielding the f_{max} variation depicted in Fig. 11. The divider exhibits an f_{max} of 5 GHz at $V_{DD} = 1.2$ V and 10 GHz at $V_{DD} = 2$ V. As a comparison, the 0.1 μm SOI implementation in [5] achieves an f_{max} of 2.6 GHz at $V_{DD} = 2$ V. The slight difference between simulated and measured results of Figs. 8 and 11 is attributed to inaccuracies in the device models used in simulations.

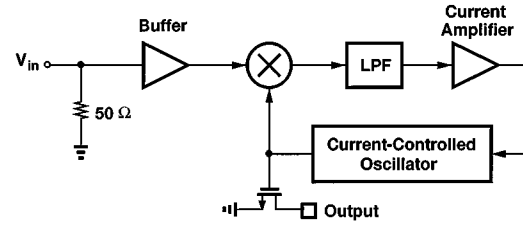


Fig. 13. Phase-locked loop architecture.

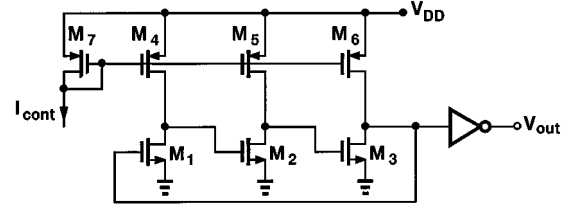


Fig. 14. Current-controlled oscillator.

The measured speed-power trade-off of the prototype (including I/O buffers) is shown in Fig. 12. The circuit dissipates 2.6 mW at 5 GHz (with $V_{DD} = 1.2$ V) and 28 mW at 13.6 GHz (with $V_{DD} = 2.6$ V).

Since the primary goal of this design has been to achieve a high speed, all the devices are ring-shaped and hence have a minimum width of 8.8 μm . For clock frequencies below 10 GHz, a design employing smaller devices can further reduce the power.

IV. PHASE-LOCKED LOOP

A. Architecture

The PLL architecture is shown in Fig. 13. It consists of an input buffer and a loop comprising a mixer, a low-pass filter (LPF), a current amplifier, and a current-controlled oscillator (CCO). The oscillator output drives an open-drain NMOS device, delivering a few milliamperes of current to an external 50 Ω load.

The input buffer is designed so as to present the same waveform and impedance to the mixer as does the VCO. This reduces the static phase error because at high speeds, the output of mixers becomes sensitive to both the waveform and the driving impedance seen at their inputs.

While it is desirable to implement the PLL in differential form so as to suppress the effect of common-mode noise, low supply voltages (< 3 V) limit the headroom, making it difficult to utilize differential control for CMOS oscillators. Thus, the PLL circuit is single-ended, but it employs current-mode control signals to lower the sensitivity to supply and substrate noise.

B. Circuit Details

Fig. 14 shows the current-controlled oscillator circuit. Using a three-stage ring oscillator with controlled PMOS current sources as loads, the CCO achieves both a wide tuning range and a maximum speed relatively independent of PMOS device

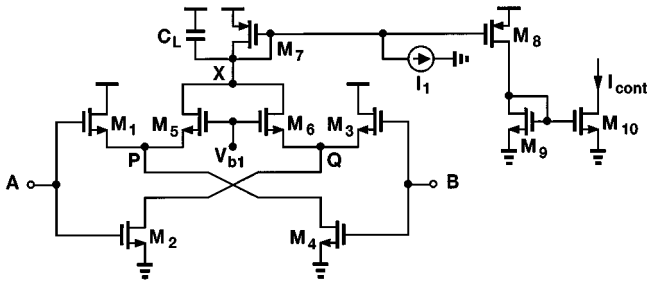


Fig. 15. Mixer-LPF-current amplifier.

characteristics. Since the voltage swings in the CCO are not rail-to-rail, the PMOS loads are in saturation for the most part and hence their gate-channel capacitance has negligible effect on the speed. Also, with a small speed penalty, the transconductance of the PMOS transistors can be minimized to reduce their contribution to the CCO phase noise. Note that all the devices are ring-shaped here.

As the oscillator employs a current-mode control signal, it achieves a relatively low sensitivity to common-mode effects. Simulations indicate that the sensitivity of the oscillation period to the supply noise is 30 times less than that of the case where the PMOS loads are controlled by a voltage.

Fig. 15 depicts the mixer-LPF-amplifier cascade. Transistors M_1 – M_6 constitute an exclusive NOR (XNOR) gate, M_7 and C_L form the LPF, and M_8 – M_{10} operate as a current amplifier. The bias voltage V_{b1} is approximately equal to $V_{DD}/2$ and I_1 functions as coarse frequency control. To understand the operation of the XNOR gate, note that when A is low, only M_4 and M_5 are active and $V_X = \bar{B}$. Similarly, when B is low, $V_X = \bar{A}$. Thus, $V_X = \bar{A} \oplus \bar{B}$.

In contrast to the conventional CMOS XOR [3], the proposed mixer has two advantages: 1) it is inherently symmetric with respect to inputs A and B , and hence free from systematic phase error; 2) it does not require complementary inputs, relaxing the design with high-speed CMOS signals. The circuit incorporates the ring-shaped geometry for all the devices, with their low-capacitance terminals connected to nodes P and Q . Employing only NMOS transistors for high speed and high mixing gain, this topology dissipates some static power when A or B is high, a nonetheless minor issue at an operating speed of 3 GHz.

An interesting issue related to mixing arises in deep sub-micron CMOS technologies. While for channel lengths of approximately 1 μm and above, it is possible to design small-signal mixers based on the square-law MOS I-V characteristics [8], velocity saturation in submicron CMOS makes it difficult to achieve small-signal mixing. This is because the small-signal transconductance of short-channel MOSFET's is relatively independent of their bias current [9] and hence can hardly be modulated by small-signal variations in that current. Thus, short-channel MOS mixers require large input signals at least at one of their inputs, an important issue in designing and interfacing the CCO and the mixer. (In contrast, bipolar transistors can perform small-signal mixing even in highly scaled technologies because their I-V characteristics remain close to exponential.)

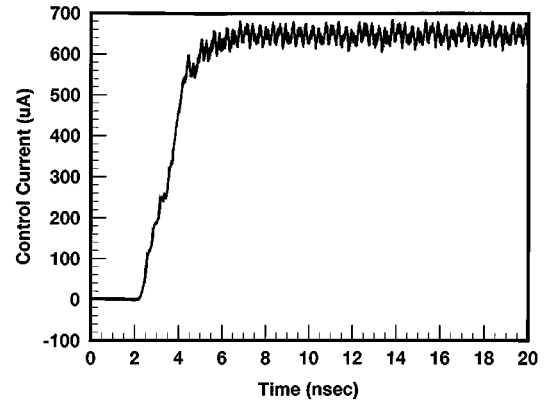


Fig. 16. Simulated control current of PLL during capture.

C. Design Considerations

An important issue in the design of PLL's is the choice of the closed-loop bandwidth and the loop filter. In addition to the capture range, two sources of noise must be considered in setting the bandwidth: the input phase noise and the oscillator phase noise. To reduce the input phase noise, the PLL must operate as a narrow-band filter, whereas to suppress the oscillator phase noise, the loop must be sufficiently fast so it can correct random variations in the oscillator period.

From the above observation, we note that the choice of the loop bandwidth depends on the application as well as the technology. For example, if the oscillator incorporates high- Q resonant devices, its (free-running) phase noise can be small and the PLL may be designed as a narrow-band filter to minimize the input phase noise. On the other hand, fully-monolithic oscillators without high- Q components exhibit substantial phase noise, demanding a large loop bandwidth. In this design, a (simulated) closed-loop bandwidth of approximately 200 MHz has been chosen to lower the CCO noise.

The loop filter determines both the bandwidth and the settling behavior of the PLL. In the circuit of Fig. 15, the loop filter transfer function, defined as the small-signal drain current of M_8 divided by the output current of the mixer, is given by

$$\frac{I_{D8}(s)}{I_X} = \frac{A_0}{1 + s/\omega_0} \quad (1)$$

where $A_0 = g_{m8}/g_{m7} \approx 2$ and $\omega_0 = g_{m7}/C_L \approx 2\pi$ (20 MHz). The simulated capture behavior of the PLL is depicted in Fig. 16. Since the nondominant poles of the loop are quite large, they have little effect on the closed-loop settling behavior. While higher order poles can be cancelled by adding zero(s) to the loop filter, this PLL includes no zeros because, at the time it was designed, neither resistors nor accurate device models were available.

D. Experimental Results

The PLL has been fabricated in our 0.1- μm CMOS process. Shown in Fig. 17 is a die photograph. The active area (excluding the loop capacitor) is approximately 60 $\mu\text{m} \times 100 \mu\text{m}$. For

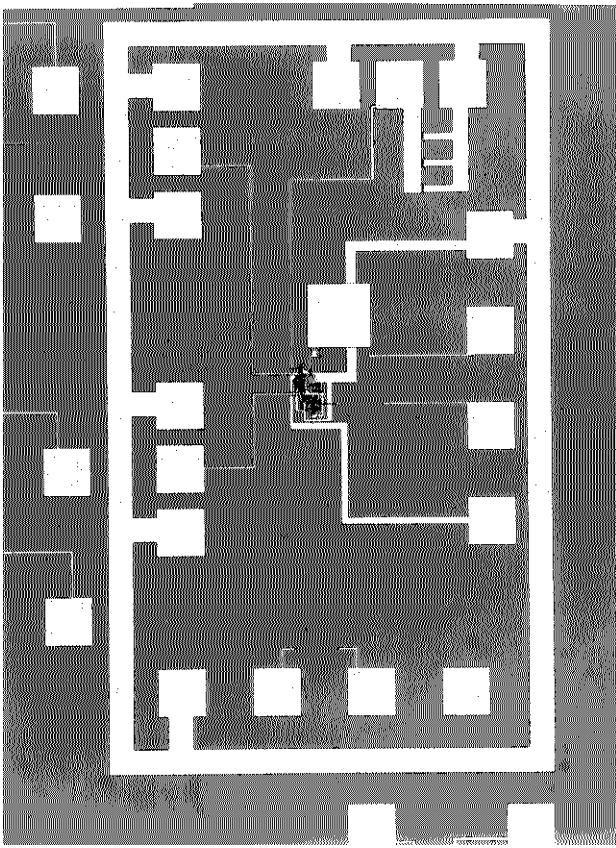


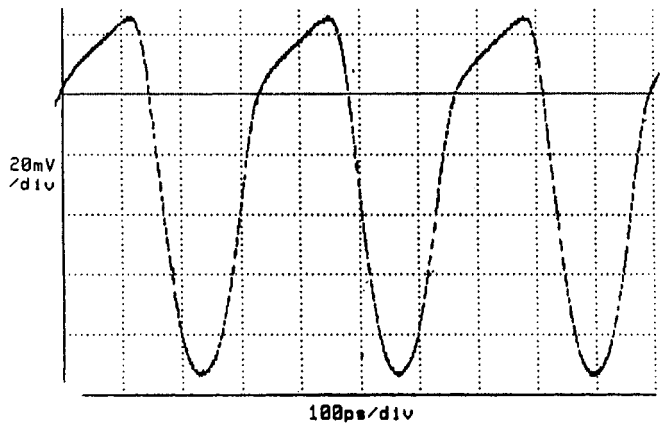
Fig. 17. PLL die photograph.

input termination, the same arrangement as the divider has been used. The circuit has been tested on wafer using high-speed Picoprobes to apply the input and sense the output and a Cascade multi-contact probe to provide power and ground connections. All tests are performed at room temperature with a supply voltage of 2.8 V.

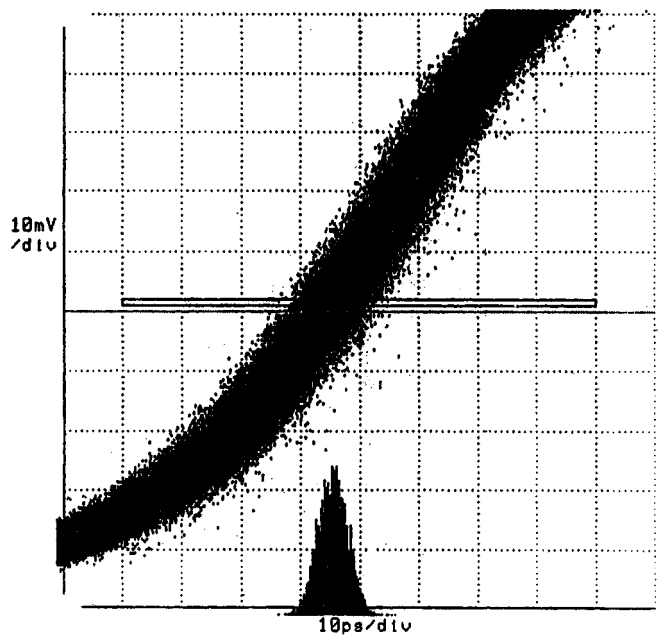
Fig. 18(a) and (b) shows the 3 GHz output waveform and its jitter histogram, respectively. The jitter is 2.5 ps rms and 20 ps peak-to-peak. The PLL (including the I/O buffers) dissipates 25 mW at this frequency.

For a 1.5-V_{pp} input signal, the tracking range is ± 320 MHz and the capture range is ± 300 MHz. The PLL speed and the upper end of the tracking range are limited by the CCO maximum frequency. As the control current increases, the PMOS loads enter the triode region for a greater part of the swing, the equivalent gain of each stage drops, and the circuit eventually fails to oscillate. Fig. 19 plots the maximum achievable operating frequency of the PLL versus the supply voltage and Fig. 20 shows the corresponding power dissipation. The measured capture range at 3 GHz as a function of the input signal power is depicted in Fig. 21.

The PLL output has also been examined in the frequency domain. Fig. 22 illustrates the CCO free-running output, indicating a relatively wide spectrum and high phase noise. The output is dramatically improved in the lock mode, as shown in Fig. 23, exhibiting a sharp spectral line at 3 GHz. The phase noise can be measured from Fig. 24 to be approximately -100 dBc/Hz at 40 kHz offset.



(a)



(b)

Fig. 18. PLL output at 3 GHz, (a) time-domain waveform, (b) jitter histogram.

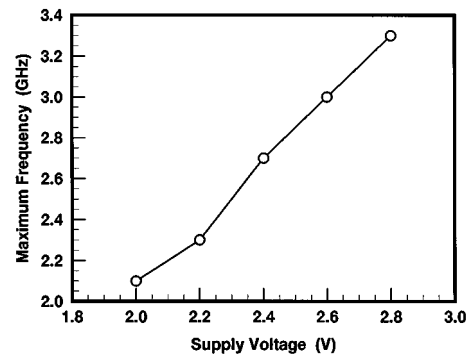


Fig. 19. Maximum achievable operating frequency of PLL versus supply voltage.

V. CONCLUSION

Deep submicron CMOS devices exhibit promising capabilities for high-performance communication circuits. The low supply voltage and low power of CMOS technologies have

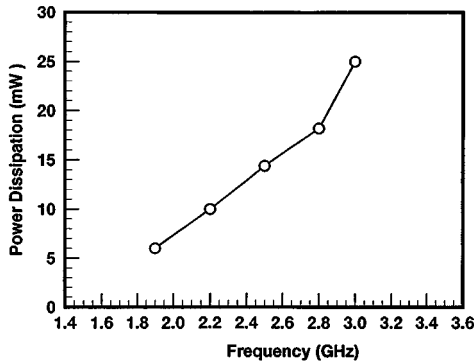


Fig. 20. PLL power-speed trade-off.

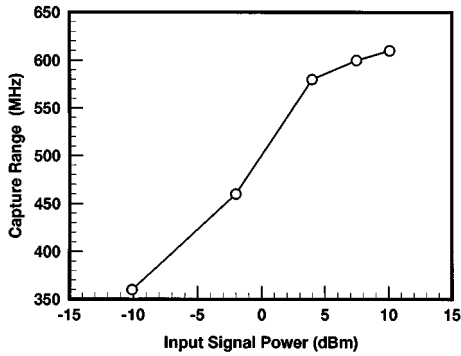


Fig. 21. PLL capture range versus input signal power at 3 GHz.

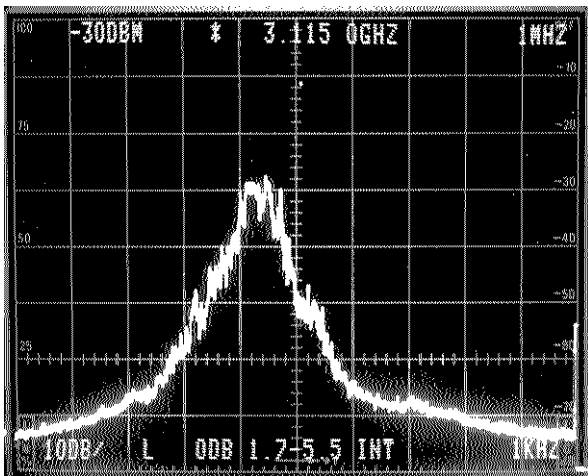


Fig. 22. PLL output spectrum with free-running CCO (horizontal scale = 1 MHz/div., vertical scale = 10 dB/div., resolution bandwidth = 1 kHz).

made them contenders to silicon bipolar and III-V devices even at multi-gigahertz speeds. We have demonstrated this potential in a 13.4 GHz 28 mW frequency divider and a 3 GHz 25 mW phase-locked loop. Using a master-slave configuration, the divider can operate with supply voltages as low as 1.2 V, at which its maximum speed is 5 GHz. The PLL incorporates a current-controlled oscillator and a fully symmetric mixer to achieve a tracking range of ± 320 MHz and an rms jitter of 2.5 ps.

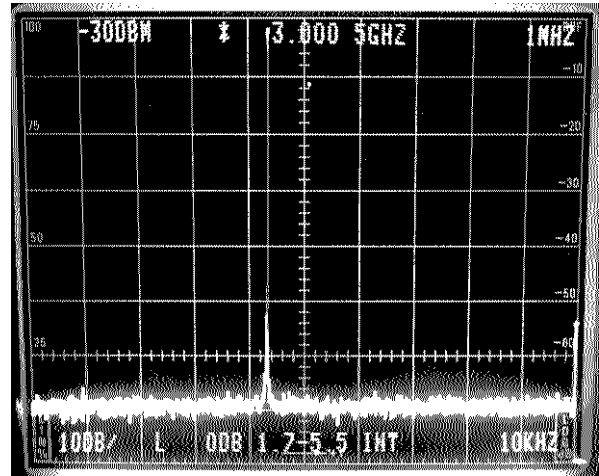


Fig. 23. PLL output spectrum in the lock mode (horizontal scale = 1MHz/div., vertical scale = 10 dB/div., resolution bandwidth = 10 kHz).

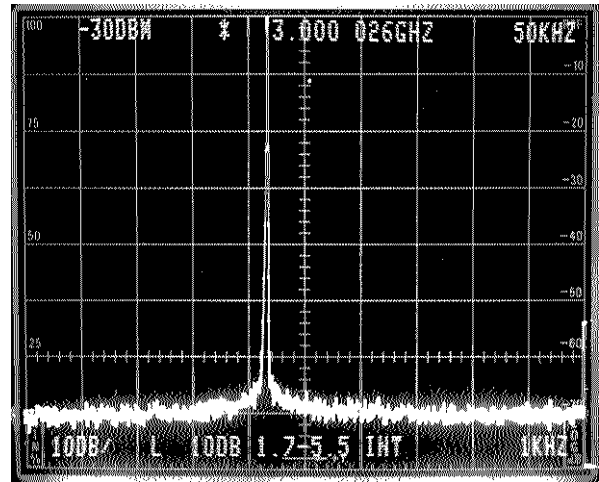


Fig. 24. PLL output spectrum in the lock mode (horizontal scale = 50kHz/div., vertical scale = 10 dB/div., resolution bandwidth = 1 kHz).

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