Brief Papers

A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's

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***Abstract*— This paper describes a radio-frequency receiver targeting spread-spectrum wireless local-area-network applications in the 2.4-GHz band. Based on a direct-conversion architecture, the receiver employs partial channel selection filtering, dc offset removal, and baseband amplification. Fabricated in a 0.6-μm CMOS technology, the receiver achieves a noise figure of 8.3 dB, IP_3 of -9 dBm, IP_2 of +22 dBm, and voltage gain of 34 dB while dissipating 80 mW from a 3-V supply.**

***Index Terms*—Low noise amplifier (LNA's), mixers, receivers, RF CMOS, wireless local area networks (LAN's).**

I. Introduction

WIRELESS local area networks (WLAN's) in the 2.4-GHz range have rapidly emerged in the consumer market. Providing flexibility and reconfigurability, WLAN standards allow data rates of several megabits/s and serve as high-speed links in office buildings, hospitals, factories, etc. For high-volume portable applications such as laptop computers, both cost and power dissipation of WLAN transceivers become critical, necessitating compact and efficient solutions [1].

This paper describes a 2.4-GHz CMOS receiver designed for WLAN applications using the IEEE 802.11 spread-spectrum (SS) standard [2]. The standard recommends two SS techniques: a frequency-hopped technique with Gaussian minimum shift keying modulation (GMSK) and direct sequence (DS) technique with quadrature phase shift keying (QPSK) modulation. The receiver reported herein is designed for the latter type.

II. Architecture and Circuit Design

The DS-SS standard spreads a 2-MHz channel by a factor of eleven, generating an output channel 22 MHz wide. The required sensitivity across this bandwidth is -80 dBm for a frame error rate (FER) of 8×10^{-2}, indicating that the sum of the noise figure (NF) and the signal-to-noise ratio (SNR) is: NF + SNR = 174 dBm $-$ 10log(22 MHz) $-$ 80 dBm $=$ 20.6 dB. Assuming SNR $\approx$ 10 dB for the required FER and 2 dB of loss in the front-end band-select filter, we arrive at a noise figure of 8.6 dB for the receiver.

Another specification of the standard is an adjacent channel (blocker) rejection of 40 dB when the desired channel is at -74 dBm. This translates to a 1-dB compression point of roughly -30 dBm.

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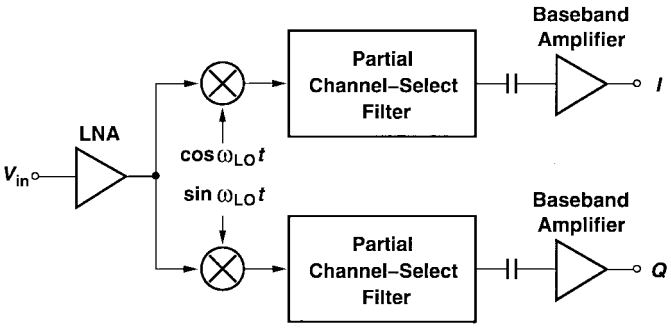

Fig. 1. Receiver architecture.

The receiver employs a direct-conversion architecture, a choice particularly suited to the DS-SS standard because of the wide channel bandwidth. Recent work using this architecture [3]–[5] suggests that the effect of various imperfections [6], [7] can be alleviated by means of circuit techniques. The two principal difficulties of direct conversion, namely, dc offsets and flicker noise, are treated here to impact the performance negligibly.

Fig. 1 shows the receiver architecture. In addition to a low-noise amplifier (LNA) and quadrature downconversion mixers, the circuit incorporates partial channel-selection filtering, ac coupling, and baseband amplification.

A. RF Section

The design of the LNA and the mixers is determined by not only noise, linearity, and gain requirements, but also effects related to direct conversion: local oscillator (LO) leakage to the antenna and second-order distortion in the RF path. The configuration depicted in Fig. 2 addresses these issues. The cascode LNA reduces the LO leakage while the inductive loading in the LNA and capacitive degeneration in the mixer minimize the products of second-order nonlinearity. The value of C_2 ($=$ 4 pF) is chosen such that it exhibits a negligible impedance at 2.4 GHz, but a relatively high impedance at frequencies below 11 MHz. If two large interferers accompany the desired signal, then second-order distortion in the RF path creates a low-frequency beat that, in the presence of asymmetries in the mixer, experiences direct feedthrough to the baseband without frequency translation [8]. Such asymmetries arise from random mismatches in the mixer itself and the deviation of the LO duty cycle from 50%. If the spacing between the interferers

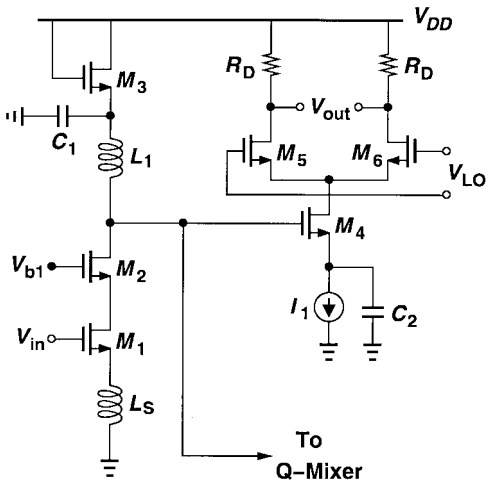

Fig. 2. LNA/mixer circuit.

is less than 11 MHz, then the direct feedthrough component falls in the baseband, thereby corrupting the downconverted signal. In this design, on the other hand, low-frequency beats generated by the LNA are suppressed by both L_1 (= 8 nH) and C_2. Furthermore, the input transistor of the mixer M_4 creates negligible beat components because of the large impedance of C_2 at low frequencies. The effectiveness of these techniques is evident from the measured second intercept point (IP_2) (+22 dBm). The LNA is biased at 6 mA and each mixer at 3 mA.

B. Baseband Section

The LNA/mixer combination exhibits a gain of approximately 24 dB, mandating high linearity in the baseband amplifiers. To relax this constraint, partial channel selection filtering is interposed between the mixers and the baseband amplifiers, thus lowering the magnitude of adjacent-channel interferers. The channel-select filter must contribute little flicker noise and tolerate several tens of millivolts of dc offset that appear at the output of the mixer due to the self-mixing of the LO. A filter topology satisfying these conditions is the Sallen and Key configuration depicted in Fig. 3(a), where the amplifier is connected in unity gain and can therefore withstand large dc offsets. The amplifier must introduce few devices in the signal path to achieve low flicker noise, but it must also exhibit high linearity. For this reason, the amplifier is realized as a source follower incorporating a relatively large transistor ($W/L = 1000\ \mu$m$/1.2\ \mu$m).

The interface between the mixer and the subsequent filter would typically require a buffer stage with low output impedance so that the filter characteristics remain unaltered, but at the cost of substantial noise and power dissipation due to the buffer. We recognize that, since the output signal of the mixer is available in the current domain, the input network of the filter can be replaced by a Norton equivalent and merged with the mixer. Depicted in Fig. 3(b), this technique obviates the need for interstage buffers. The bottom-plate parasitic of C_1 is placed at nodes X and Y to suppress the LO feedthrough, which would otherwise desensitize the source follower.

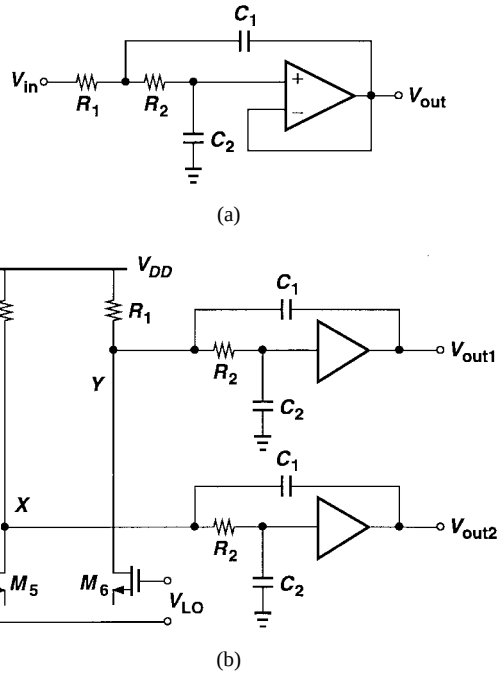

Fig. 3. (a) Simple sallen and key filter. (b) Filter merged with output of mixer.

The dc offsets resulting from the self-mixing of LO must be removed to avoid saturating the baseband amplifier. However, since QPSK signals translated to the baseband contain significant energy in the vicinity of zero frequency, the dc notch filter must exhibit a very low corner frequency f_C. Thus, the choice of f_C is determined by three questions.

1) How does the notch filter affect the downconverted signal?
2) How *high* can f_C be without excessive degradation of the signal?
3) How can a notch filer with such a low f_C be integrated?

The first two questions are answered by simulations of a QPSK signal that is modulated with raised-cosine filtered baseband pulses,[1] translated to dc and applied to a first-order high-pass RC filter. For the sake of clarity, the bit rate in each of the I and Q paths is equal to 1 b/s, and only one path is shown here. (In the actual design, each of the I and Q outputs carries a data stream at 11 Mchips/s.) Fig. 4(a) shows the eye diagram of a raised-cosine binary stream with no high-pass filtering, which indicates that if the data is sampled at $T = 1.0, 2.0, \ldots$, then an exact value of $+1.0$ or -1.0 is obtained. Fig. 4(b) depicts the output of the high-pass filter if $f_C = 0.01$ Hz, i.e., 1% of the bit rate. The waveform suffers from substantial intersymbol interference and the sampled values at $T = 1.0, 2.0, \ldots$, are degraded by about 3.6 dB. Fig. 4(c) provides the same output if $f_C = 0.001$ Hz, revealing a signal degradation of approximately 0.54 dB.

This design incorporates a first-order high-pass filter with a nominal f_C of 10 kHz, i.e., about 0.1% of the chip rate in each of the I and Q paths. Setting the maximum allowable value

[1]The standard does not specify the type of pulse shaping for DS-SS, but raised-cosine filtering is usually used to achieve efficiency.

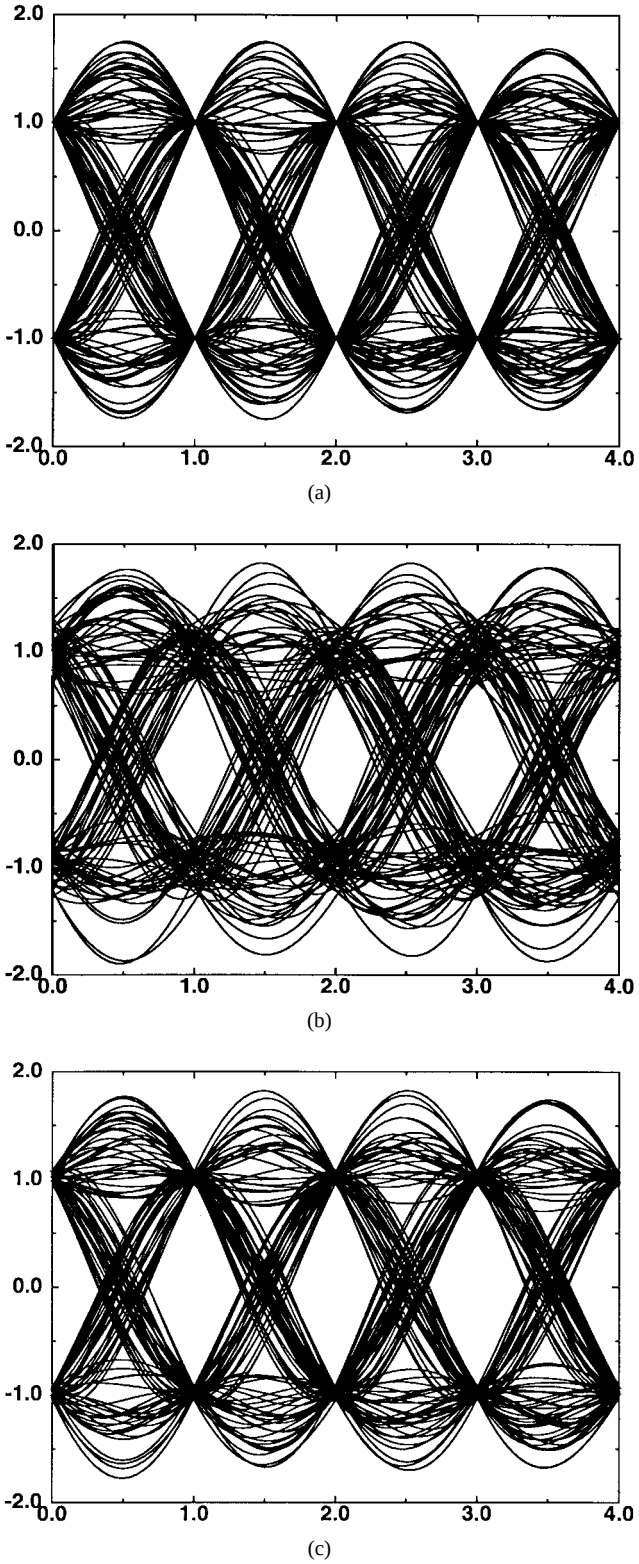

Fig. 4 Eye diagrams. (a) With no high-pass filtering. (b) With f_C equal to 1% of bit rate. (c) With f_C equal to 0.1% of bit rate. (Horiz. scale normalized to bit period, vert. scale in V.)

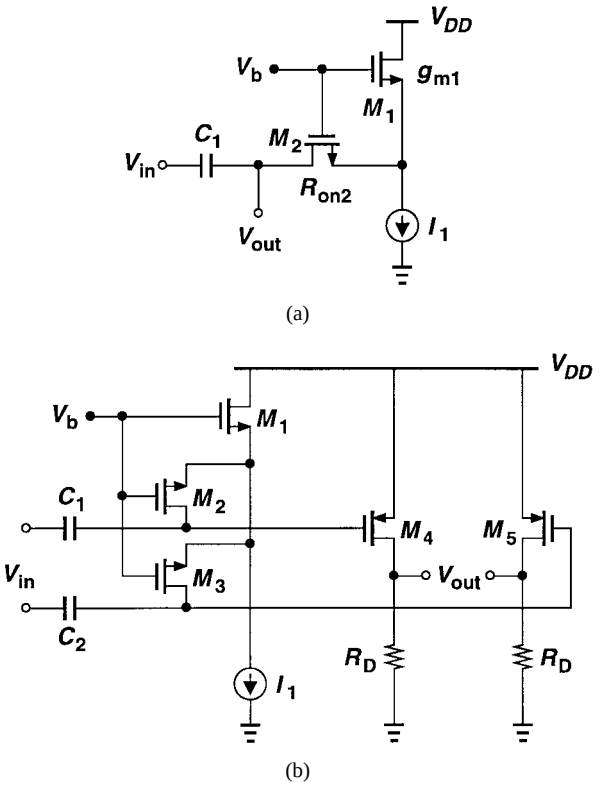

Fig. 5. (a) High-pass filter with $R_{\mathrm{on}\,2} = g_{m\,1}^{-1}$. (b) Differential high-pass filter along with baseband amplifier.

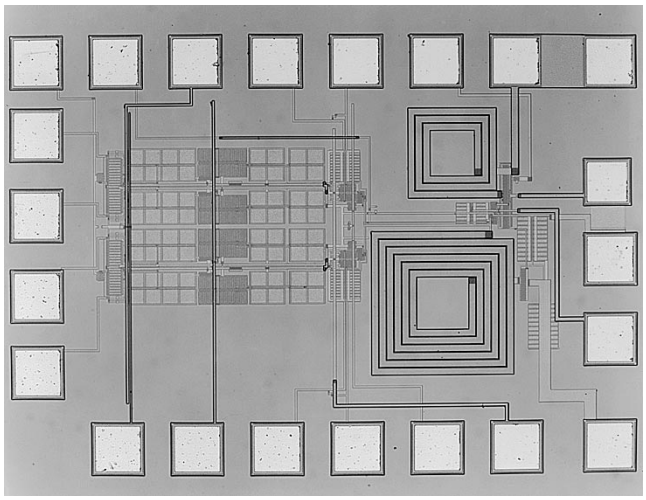

Fig. 6. Receiver die photograph.

of the coupling capacitor to 10 pF (i.e., a total of 40 pF for differential I and Q signals), we arrive at a resistance of 1.6 MΩ. Even using n-well material, such a resistor would suffer from enormous capacitance to the substrate, much greater than 10 pF! To resolve this issue, we employ MOS devices operating in deep triode region with a well-controlled gate-source overdrive voltage $V_{\mathrm{GS}} - V_{\mathrm{TH}}$. Illustrated in Fig. 5(a), the idea is based on the observation that, for long-channel devices, the transconductance of a saturated MOSFET (M_1) is expressed by the same equation, $g_{m1} = \mu C_{ox}(W/L)(V_{\mathrm{GS}} - V_{\mathrm{TH}})$, as the inverse of the on-resistance of a similar device in deep triode region (M_2): $R_{\mathrm{on}2}^{-1} = \mu C_{ox}(W/L)(V_{\mathrm{GS}} - V_{\mathrm{TH}})$. That is, if a saturated device and a linear device have equal overdrive voltages and equal dimensions, the on-resistance of the latter is equal to the inverse transconductance of the former. Since the transconductance of MOSFET's can be defined by

TABLE I
MEASURED PERFORMANCE OF RECEIVER AT 2.4 GHz

Input Frequency	2.4 GHz
Noise Figure	8.3 dB
IP2	+22 dBm
In–Channel IP3	–9 dBm
1–dB Compression Point	–21 dBm
Out–of–Channel IP3	–4 dBm
Voltage Gain	34 dB
LO Leakage	–47 dBm
Output Offset Voltage	7 mV
Power Dissipation	80 mW

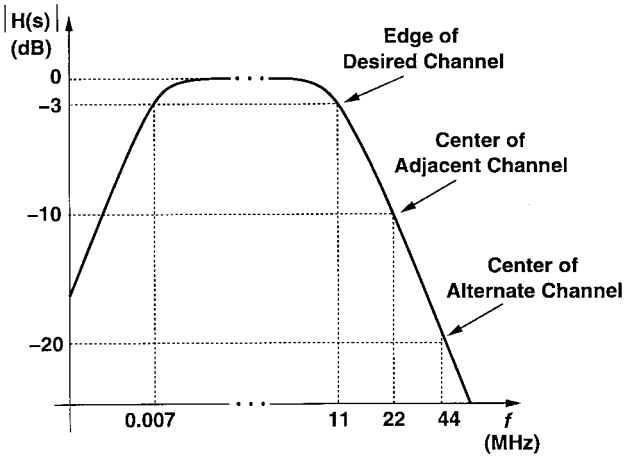

Fig. 7. Measured baseband transfer function. (Axes not to scale.)

means of various analog techniques, this technique makes it possible to achieve a very high on-resistance.

The design of Fig. 5(a) must nonetheless deal with two issues. First, the threshold voltage mismatch between M_1 and M_2 yields some inaccuracy in the definition of R_{on2}. For this reason, an overdrive voltage of 200 mV is chosen for the transistors, suppressing the effect of mismatches. Second, the variation of the on-resistance of M_2 with the input signal level leads to distortion. Fortunately, however, the tolerable in-channel distortion is quite high (several percent) because of the nature of the signal waveform, and the out-of-channel distortion is low because the coupling capacitor exhibits a low impedance at adjacent-channel frequencies. Simulated and measured in-channel and out-of-channel two-tone tests of the receiver confirm these results. Fig. 5(b) shows the differential implementation of the high-pass filter and the baseband amplifier. In this design, $(W/L)_1 = 2(1.5\ \mu\text{m}/40\ \mu\text{m})$ and $(W/L)_{2,3} = 1.5\ \mu\text{m}/40\ \mu\text{m}$. Also, $I_1 \approx 0.2\ \mu\text{A}$ and $I_{D4} = I_{D5} = 1$ mA.

The flicker noise in the baseband section corrupts the downconverted signal. However, since the baseband signal occupies a bandwidth of 11 MHz, flicker noise corner frequencies as high as several hundred kilohertz affect the performance negligibly. With a corner frequency of 200 kHz, we can write: $S_{1/f}(200\ \text{kHz}) = S_{th}$, where $S_{1/f}$ and S_{th} denote the power spectral densities of $1/f$ noise and thermal noise, respectively. Assuming $S_{1/f} = K/f$, where $K = (200\ \text{kHz}) \times S_{th}$, and integrating the total noise from 10 kHz to 11 MHz, we have

$$\overline{V_n^2} = \int_{10\ \text{kHz}}^{200\ \text{kHz}} \frac{K}{f}\,df + \int_{200\ \text{kHz}}^{11\ \text{MHz}} S_{th}\,df \tag{1}$$

$$= K \ln 20 + (10.8\ \text{MHz}) S_{th} \tag{2}$$

$$\approx (11.4\ \text{MHz}) S_{th}. \tag{3}$$

By contrast, if the circuit contained no flicker noise, the total noise power would be $\overline{V_n^2} = (11\ \text{MHz})\ S_{th}$, only 0.2 dB lower. Note that even if flicker noise frequencies as low as 100 Hz are taken into account, the maximum degradation in SNR is less than 0.6 dB. This is a pessimistic estimate because, owing to the relatively high gain in the RF section and hence amplification of thermal noise, the $1/f$ noise corner in the baseband is expected to be quite lower than 200 kHz.

III. EXPERIMENTAL RESULTS

The receiver has been fabricated in a 0.6-μm CMOS technology in an area of 680 μm $\times$ 980 μm. Fig. 6 shows a photograph of the die. Both inductors used in the cascode LNA are integrated on-chip with no process modifications, exhibiting a Q of approximately three. The circuit is tested with a 3-V supply.

Table I summarizes the measurement results. The out-of-channel IP_3 is measured by applying two tones 22 MHz apart such that they fall at 22 and 44 MHz after downconversion, and their intermodulation product appears near zero frequency. Fig. 7 plots the measured transfer function of the baseband section, obtained by (manually) sweeping the RF input. Note that the corner frequency of the baseband dc-notch filter is approximately equal to 7 kHz, confirming the feasibility of the circuit topology shown in Fig. 5(b).

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