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The Bootstrapped Switch

Field-effect transistors (FETs) have been used as switches, particularly for analog signals, since the 1950s. In the early days of analog sampling, it was discovered that such devices exhibit an input-dependent on-resistance, thereby introducing distortion. This issue can be resolved by "bootstrapping," a circuit technique that minimizes the switch on-resistance variation in the presence of large input and output voltage swings. In this article, we study the bootstrapped switch topology and appreciate its role in nanometer designs.

Brief History

To maintain a relatively constant on-resistance for a switch, we wish to fix its gate-source voltage as the input varies. In a patent filed in 1966 [1], Russell proposes the circuit shown in Figure 1, where the P-type source follower 15 shifts the input up by a relatively constant amount, $|V_{GS15}|$, and drives the gate of the N-type switch, 10. Thus, $V_{GS10} = V_{in} + |V_{GS15}| - V_{in} = |V_{GS15}|$, and the switch acts as a linear resistance. We can view the source follower's role as a battery that sets V_{GS15}.

The idea of a "continuous-time" level shift between V_{in} and the gate of the switch became popular in the 1970s and appeared in other patents [2], [3] in forms similar to Russell's. But as analog CMOS circuits employed increasingly more switches, the power dissipated by the level shift circuit, which cannot be shared among switches, proved undesirable. Also, the voltage headroom occupied by the source follower and its bias current source limited the allowable input range as the supplies scaled down. It was time to devise a more versatile "passive" level shift arrangement that would consume no static power.

The notion of realizing the level shift battery by a precharged capacitor can be traced to [4]. A number of modifications followed [5], [6], culminating in the topology described in [7] in 2001, which forms the foundation for our study here.

Switch Nonidealities

Nanometer MOS switches suffer from a number of imperfections, but we focus here on two that can be alleviated through bootstrapping. In the simple circuit of Figure 2(a), CK is at V_{DD} when M_1 is on, leading to an on-resistance, R_{on}, approximately equal to $[\mu_n C_{ox}(W/L)(V_{DD} - V_{in} - V_{TH})]^{-1}$. Since $R_{on} \to \infty$ as V_{in} approaches $V_{DD} - V_{TH}$, the input range is quite limited. To remedy the situation, we can resort to the complementary topology shown in Figure 2(b), where M_2 accommodates higher input levels. Due to MOS nonidealities (notably, degradation of mobility with the vertical field in the channel), the net on-resistance of this structure still varies considerably with V_{in}. Plotted in Figure 2(c) is an example for $(W/L)_1 = 5\,\mu m/40\,nm$ and $(W/L)_2 = 25\,\mu m/40\,nm$, so chosen to *minimize* the variation. The nearly sevenfold change in R_{on} modulates the phase shift of the circuit in Figure 2(b), distorting the signal that appears across C_1. This can be seen by expressing the input as

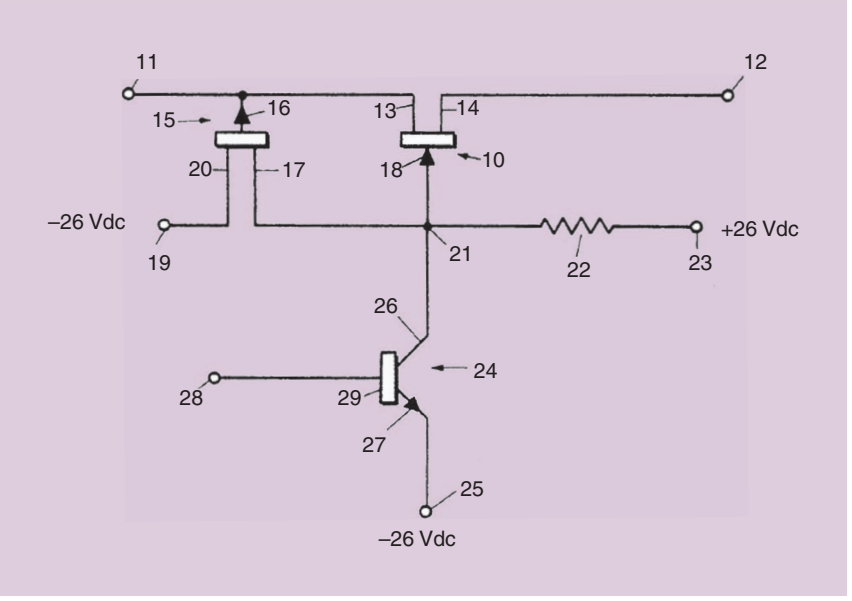

FIGURE 1: An early bootstrapped switch.

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$V_{in}(t) = V_0 + V_0 \cos \omega_{in} t$ and approximating the output as

$$V_{out}(t) = V_0 + V_0 \cos [\omega_0 t - \tan^{-1}(R_{on} C_1 \omega_{in})] \quad (1)$$
$$\approx V_0 + V_0 \cos \omega_0 t + V_0 R_{on} C_1 \omega_{in} \sin \omega_{in} t, \quad (2)$$

where the signal attenuation is neglected and the phase shift is assumed much lower than 1 rad. For a periodic input, R_{on} also varies periodically and can therefore be expanded as a Fourier series. In fact, the roughly symmetric behavior depicted in Figure 2(c) suggests that R_{on} completes *two* cycles for one input cycle. Writing the Fourier series of R_{on} as $R_0 + R_1 \cos 2\omega_{in} t + R_2 \cos 4\omega_{in} t + \cdots$, we obtain the following output:

$$V_{out}(t) \approx V_0 + V_0 \cos \omega_{in} t + V_0 \times C_1 \omega_{in} (R_0 + R_1 \cos 2\omega_{in} t + \cdots) \sin \omega_{in} t. \quad (3)$$

The third harmonic in the output assumes an amplitude of $V_0 C_1 \omega_{in} R_1 / 2$ and, if normalized to the first harmonic, yields

$$\text{Normalized Third Harmonic} \approx \frac{R_1 C_1 \omega_{in}}{2}. \quad (4)$$

As an example, for a distortion level below –60 dB, we must ensure $\omega_{in} < 2000/(R_1 C_1)$, facing severe bandwidth limitations.

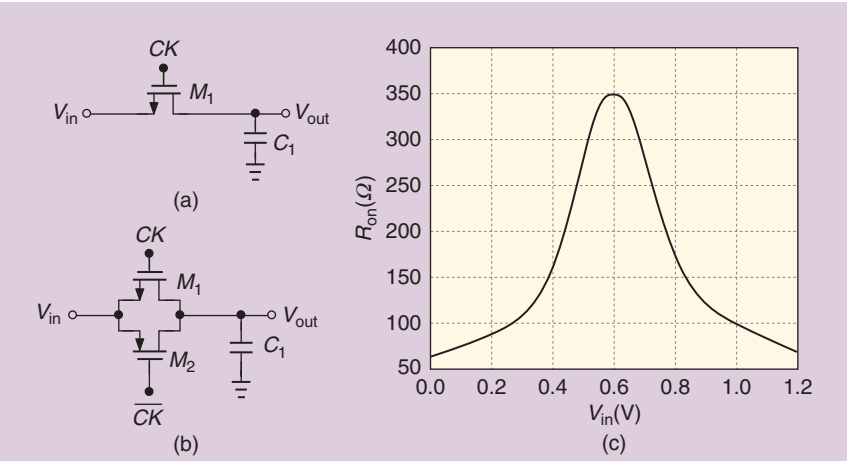

FIGURE 2: (a) A simple sampling circuit, (b) a sampling circuit with complementary switches, and (c) simulated on-resistance of complementary switches as a function of input voltage.

What if we make the switches in Figure 2(b) much wider so that R_{on} and R_1 scale down proportionally? Then, the drain junction capacitance of these switches contributes a significant nonlinear component to C_1, causing distortion. These observations indicate that a complementary switch proves inadequate for linearities above approximately 6 b.

Another issue in the sampling circuits of Figure 2(a) and (b) relates to the inversion layer charge stored in the transistors when they are on. Upon turning off, the MOSFETs inject some of this charge onto C_1, thus adding an error to the sampled signal. The principal difficulty is that this charge is a function of V_{in}; e.g., $Q_{ch} = WLC_{ox}(V_{GS} - V_{TH}) = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$ for the NMOS device. Bootstrapping also suppresses this dependence by fixing V_{GS} (but V_{TH} is a function of the input due to body effect).

Basic Bootstrapping

We have surmised that a battery tied between the gate and source of a switch can keep the device on with a constant V_{GS}. As shown in Figure 3(a), such an arrangement "bootstraps" the gate to the source, allowing the two to change in unison. Interestingly, V_G can rise *above* the supply voltage in this case, a valuable property in low-voltage design.

Let us approximate the battery by a precharged capacitor as depicted in Figure 3(b). In the sampling mode, C_b keeps M_{11} on. In the hold mode, two actions must be completed: M_{11} must be turned off and C_b must be recharged, e.g., to V_{DD}. We therefore add five switches to the

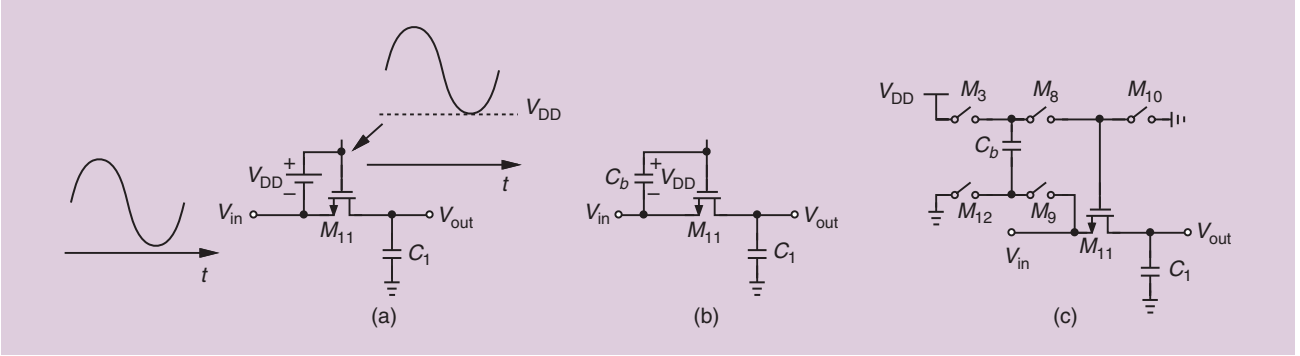

FIGURE 3: (a) Bootstrapping the gate to the input by a battery, (b) the use of a capacitor to approximate the battery, and (c) the addition of other switches to allow M_{11} to turn off and C_b to recharge.

circuit [Figure 3(c)]: M_{10} turns M_{11} off, M_8 and M_9 disengage C_b from M_{11}, and M_3 and M_{12} precharge C_b to V_{DD}. We observe that each sampling circuit requires at least five more transistors and one capacitor for bootstrapping.

Complete Bootstrapped Switch

We now determine the type of MOSFETs that can be used for the switches in Figure 3(c). Since M_{10} and M_{12} connect their respective drains to ground, they must be realized as NMOS devices. Also, since M_8 ties the top plate of C_b (a high voltage) to the gate of M_{11}, it must use a PMOS transistor. We assume these three switches are driven by $\overline{CK}$ [Figure 4(a)], and hence the circuit enters the hold mode when CK falls and $\overline{CK}$ rises.

The choice of M_3 and M_9 entails interesting points. Precharging the top plate of C_b to V_{DD}, M_3 must be a PMOS switch, but can we drive its gate by CK? In such a case, M_3 must be turned off by raising its gate to V_{DD}, yielding the simplified circuit of Figure 4(b) in the sampling mode. Recall that V_p can rise *above* V_{DD} because it contains both the precharge voltage and the input swing. Consequently, as V_p rises, the source and drain of M_3 exchange roles, the new source reaches a voltage exceeding the gate voltage by more than one threshold, and M_3 turns on. To avoid this difficulty, we bootstrap the gate of M_3 to V_{in} as shown in Figure 4(c).

Transistor M_9 senses the input in the sampling mode and must therefore be the same type as M_{11}. If the gate voltage of M_9 is at V_{DD} in this mode, then the transistor turns off or at least exhibits a large on-resistance for high values of V_{in}. We address this issue by bootstrapping the gate of this switch as well, arriving at the topology illustrated in Figure 4(c).

While performing well and providing a high linearity, the sampling circuit of Figure 4(c) entails one drawback: when V_X rises above V_{DD} in the sampling mode, M_{10} experiences drain-source and drain-gate voltages greater than V_{DD}. The resulting "stress" shortens the device lifetime and must be avoided. This can be accomplished by shielding M_{10} through the use of a cascode device [Figure 4(d)] [7]. Now, M_{14} limits V_{DS10} and V_{GS10} to about $V_{DD} - V_{TH14}$ (when M_{10} is off).

The bootstrapping topology studied above has been used in a number of analog-to-digital converters with resolutions ranging from 8 b to 12 b [8], [9]. It has proved to be a robust solution affording both high linearity and high speed.

Questions for the Reader

1) In Figure 2(c), $R_1 \approx R_0$. Suppose we define the small-signal bandwidth of the sampler as $(2\pi R_0 C_1)^{-1}$. Determine the ratio of ω_{in} to this bandwidth if the third-order distortion given by (4) must remain lower than –60 dB. This example

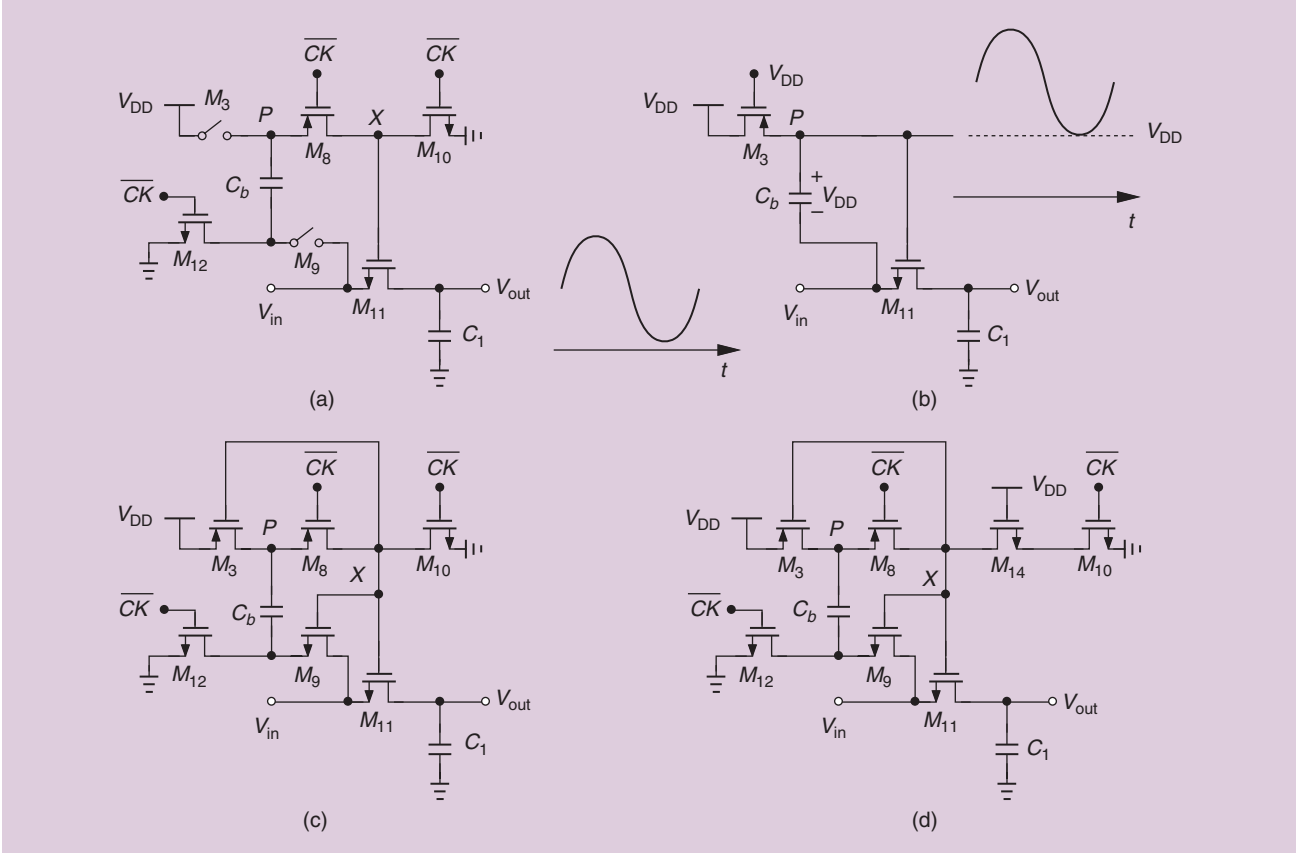

FIGURE 4: (a) A bootstrapping circuit with some switches implemented by MOSFETs, (b) a turn-on issue of M_3, (c) avoiding M_3 turn-on by tying its gate to X, and (d) the use of M_{14} to minimize stress on M_{10}.

demonstrates the severity of the variable on-resistance.

2) To which node(s) should the n-wells of M_3 and M_8 in Figure 4(d) be connected?
3) How high can V_X in Figure 4(d) go to avoid stressing M_{14}?

Answers to Last Issue's Questions

1) Do V_P and V_Q in Figure 5 reach 0 V at the end of the regeneration phase?

   Yes, they do. We observe that M_1–M_3 are on but with zero drain current because both M_3 and M_6 (or M_4 and M_5) are off. Nodes P and Q are therefore discharged to zero.

2) Explain why M_3 and M_4 in Figure 5 can be omitted if the inputs have rail-to-rail swings.

   With rail-to-rail input swings, either M_1 or M_2 is off, cutting off the path from V_{DD} to ground. By contrast, if $|V_{in1} - V_{in2}|$ is small, then both M_1 and M_2 remain on.

3) Explain why the coupling through C_{GD7} in Figure 5 is less on the rising edge of CK than on the falling edge of CK.

   On the rising edge of the clock, M_7 begins from the off state and its C_{GD} is primarily due to the gate-drain overlap capacitance. On the falling edge, the transistor begins in the deep triode region, with $C_{GD7} \approx C_{GS7}$, exhibiting a greater feedthrough.

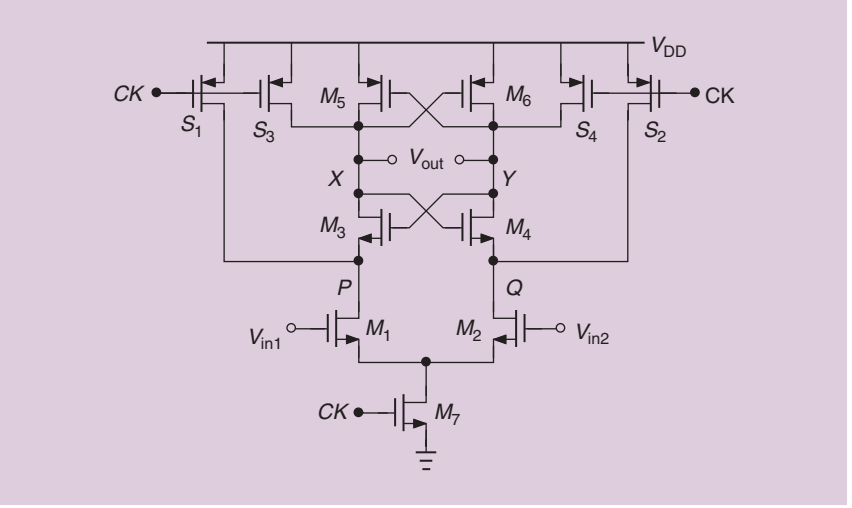

FIGURE 5: The StrongARM latch.

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