Behzad Razavi

The Switched-Capacitor Integrator

In the 1970s, CMOS technology was finding its way into analog design through switched-capacitor circuits. The availability of simple switches and high-impedance nodes in CMOS afforded more efficient sampling and holding of signals than in bipolar technologies. The switched-capacitor integrator was a versatile function developed in that era as a building block for filters, but it later found usage in such systems as $\Delta\Sigma$ modulators as well. In this article, we study the operation and properties of this circuit.

Background

It had been recognized since the concept of the operational amplifier (op amp) was articulated in the 1940s that a continuous-time integrator could be realized as shown in Figure 1(a). Maxwell also recognized that a capacitor periodically switched between two nodes could approximate a resistor [Figure 1(b)]. Thus, one would naturally replace R_1 with a switched capacitor to arrive at a discrete-time integrator [Figure 1(c)].

Digital Object Identifier 10.1109/MSSC.2016.2624178
Date of publication: 23 January 2017

Here, C_2 first samples the input voltage and then delivers its charge to C_1 through the virtual ground. As a result, C_1, which is not reset, integrates discrete values of V_{in} over time, generating, after each clock period, an output voltage change equal to $-(C_2/C_1)V_0$, where V_0 is the sampled value of V_{in}.

The circuit of Figure 1(c) is sensitive to the parasitic capacitance at node N. For example, if C_2 itself incurs a fringe capacitance of C_f from N to ground, then the integrator "gain" changes from $-C_2/C_1$ to $-(C_2+C_f)/C_1$. More importantly, the source/drain junction capacitances associated with S_1 and S_2 contribute a nonlinear component to this parasitic, distorting the integration.

It had been recognized since the concept of the operational amplifier (op amp) was articulated in the 1940s that a continuous-time integrator could be realized.

For example, if we express C_2 as a voltage-dependent capacitor $C_0(1+\alpha V)$ and note further that, for any capacitor, $dQ = CdV$, we can determine the charge deposited on C_2 by V_{in} as

$$Q = \int_0^{V_{in}} C_0(1+\alpha V)\,dV \qquad (1)$$

$$= C_0 V_{in} + \frac{1}{2}\alpha C_0 V_{in}^2. \qquad (2)$$

That is, the charge received by C_1 contains a term proportional to V_{in}^2.

A third issue in the integrator of Figure 1(c) relates to the input-dependent channel charge of S_1. Upon turning off, this switch injects some of its charge onto C_2, introducing additional nonlinearity.

In the late 1970s, the "parasitic-insensitive" integrator was proposed by several different workers in the field. A patent filed by Gregorian in September 1978 [1] proposes the filter implementation shown in Figure 2, which includes one such integrator. A related paper by Gregorian et al. was presented at the International Solid-State Circuits Conference (ISSCC) in February 1979 [2]. At that year's ISSCC, the same topology was proposed by

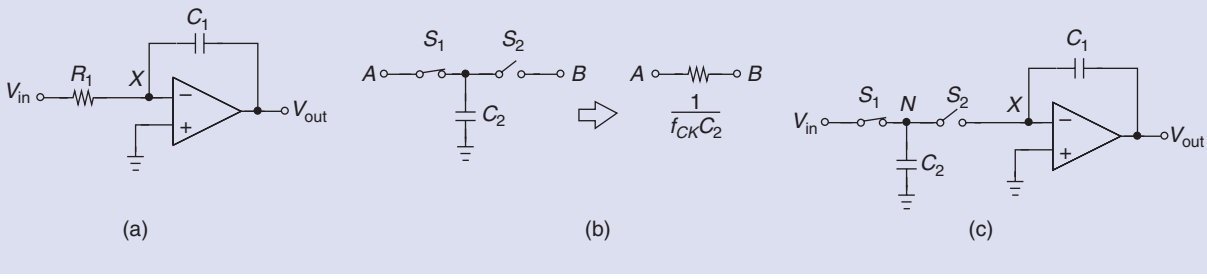

FIGURE 1: (a) A continuous-time integrator, (b) a switched capacitor acting as a resistor, and (c) a switched-capacitor integrator.

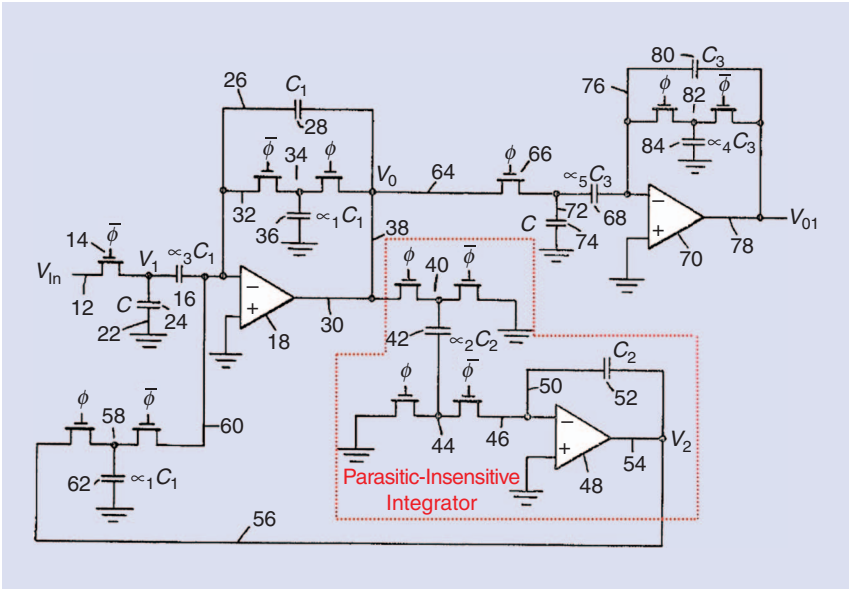

FIGURE 2: The filter described by Gregorian in 1978, showing a parasitic-insensitive integrator.

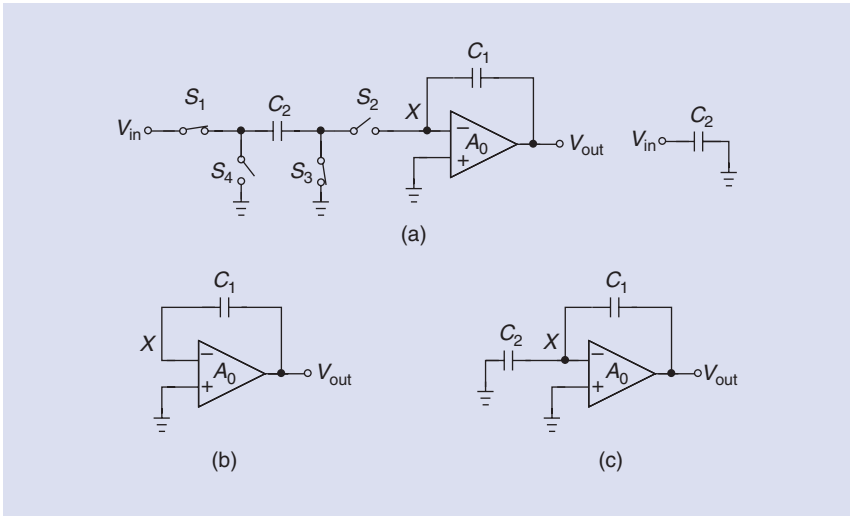

FIGURE 3: (a) A basic parasitic-insensitive integrator, (b) its operation in the sampling mode, and (c) its operation in the integration mode.

Allstot et al. [3] and White et al. [4]. In addition, Martin and Sedra describe the circuit in *Electronics Letters* in June 1979 [5]. It is interesting that all these groups developed the same concept at around the same time.

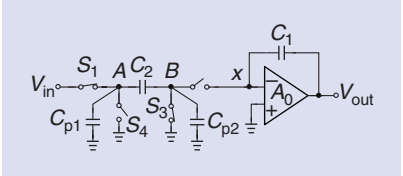

FIGURE 4: The effect of parasitic capacitances on an integrator's operation.

Basic Structure

Depicted in Figure 3(a), the parasitic-insensitive integrator controls the sampling capacitor by four switches and two nonoverlapping clocks. First, S_1 and S_3 are on, allowing C_2 to charge to V_{in} [Figure 3(b)]. Next, these switches turn off, and S_2 and S_4 turn on, forcing the charge on C_2 to travel to C_1 [Figure 3(c)]. It is worth noting that the snapshots of this circuit in the sampling and integration modes look the same as those of the topology in Figure 1(c), but the nonidealities have different effects.

Suppose C_2 has a parasitic capacitance from each plate to ground. As shown in Figure 4, the left-plate parasitic, C_{p1}, does charge to V_{in} in the sampling mode, but it is discharged to ground by S_4 in the integration mode. The right-plate parasitic, C_{p2}, is charged only slightly in the integration mode due to the finite gain of the op amp. In other words, the charge delivered to C_1 has no contribution from C_{p1} and very little from C_{p2}. This point also applies to the nonlinearities arising from these parasitics.

The use of nonoverlapping clocks for $S_{1,3}$ and $S_{2,4}$ in Figure 3(a) is necessary for avoiding the simultaneous activation of 1) S_3 and S_4, which would corrupt the value stored on C_2, and 2) S_1 and S_2, which would allow V_{in} to momentarily charge C_1 through C_2, reducing the integrator gain as explained in the following.

The integrator of Figure 3(a) also avoids channel charge-injection effects by proper sequencing of the switch controls. Specifically, if S_3 turns off before S_1 does, then the charge injected by S_1 is not deposited on C_2 (because S_2 is off) and hence plays no role in the integration process. Switch S_2 does inject charge onto C_1, but this charge is independent of the input and introduces only a constant offset, an effect unimportant in differential implementations.

The structure shown in Figure 3(a) is a noninverting integrator. To see this point, suppose V_{in} is constant and equal to V_0, placing on the right plate of C_2 a charge amount equal to $-C_2 V_0$ in the sampling mode. This charge moves to the left plate of C_1 in the integration mode, causing a change of $+C_2 V_0/C_1$ in V_{out}. An inverting integrator can be realized by changing the switch controls so that S_1 and S_2 turn on together, as do S_3 and S_4 [6].

As shown in Figure 5, in one mode, V_{in} charges C_1 through C_2; in the other mode, C_2 is reset. The circuit resembles an inverting amplifier in the first mode, but, in fact, it integrates because C_1 is not reset. [We can now see why simultaneous turn

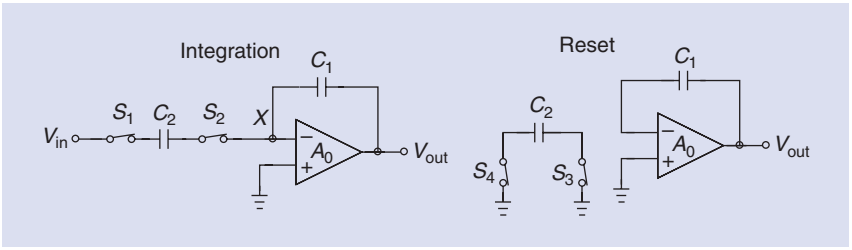

FIGURE 5: An inverting integrator in integration and reset modes.

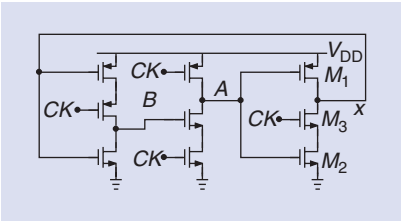

FIGURE 6: A true single-phase clock frequency divider.

on of S_1 and S_2 in Figure 3(a) would briefly create an inverting integrator.] This configuration is less popular because its op amp must provide a high slew rate to ensure that V_{out} can faithfully track V_{in} while V_{in} is changing. By contrast, in the circuit of Figure 3(a), the op amp is not exposed to the time-varying input, and its slewing is benign if the integration mode is long enough.

The finite gain of the op amp leads to nonideal integration.

Imperfections

The design of the integrator in Figure 3(a) begins with the values of C_2 and C_1, their ratio chosen for a desired gain. Capacitor C_2 experiences kT/C noise in both the sampling and the integration phases, yielding a total output noise of $(2kT/C_2)(C_2/C_1)^2$. In a differential implementation, this value must be doubled.

With C_1 and C_2 known, the op amp is designed to provide, in the integration mode, sufficient linearity and settling speed with acceptable noise. If driving a load capacitance of C_L, the circuit exhibits a small-signal time constant equal to $(C_1 C_2 + C_1 C_L + C_2 C_L) / (G_m C_1)$, where G_m denotes the op amp's transconductance.

The finite gain of the op amp leads to nonideal integration. This is because, in Figure 3(a), C_1 cannot maintain its charge if X is not a perfect virtual ground. To understand this point, let us assume that the circuit begins with an initial condition of V_0 on C_1, while $V_{in} = 0$. When C_2 switches into X, C_1 loses some charge because C_2 must sustain a voltage equal to V_X. Consequently, C_1 reaches a voltage given by $(A_0 + 1) V_0 / (A_0 + 1 + C_2/C_1)$, where A_0 is the op amp's open-loop gain.

We observe that the voltage on C_1 is attenuated by a factor of $(A_0 + 1)/(A_0 + 1 + C_2/C_1)$. This phenomenon repeats in every clock cycle—as if C_1 experienced leakage (hence the term "leaky integrator"). We can attribute a time constant to this loss by equating the voltage on C_1 after n clock cycles to a decaying exponential:

$$\left(\frac{A_0+1}{A_0+1+C_2/C_1}\right)^n V_0 = V_0 e^{-nT_{CK}/\tau}. \quad (3)$$

It follows that

$$\tau = \frac{T_{CK}}{\ln\left[1+\dfrac{C_2}{(A_0+1)C_1}\right]} \quad (4)$$

$$\approx (A_0+1)\frac{C_1}{C_2}T_{CK} \quad (5)$$

if $C_2 \ll (A_0 + 1) C_1$. We can say that the loss has moved the integrator's pole from the origin to $1/\tau$.

This result can also be obtained by approximating the discrete-time integrator shown in Figure 1(c) by its continuous-time counterpart in Figure 1(a) and recognizing that the circuit contains a pole at X given by

$$[R_1(A_0+1)C_1]^{-1} = [(f_{CK}C_2)^{-1}(A_0+1)C_1]^{-1} = f_{CK}/[(A_0+1)C_1/C_2].$$

Questions for the Reader

1) In the circuit shown in Figure 4, C_{p2} appears in series with C_2 when S_3 turns off. Does the charge injected by S_1 corrupt the sampled value in this case?
2) Given that the op amp in Figure 3(a) is placed in an inverting configuration, how do we intuitively explain the noninverting operation of the integrator?

Answers to Last Issue's Questions

1) Can the third stage in the frequency divider shown in Figure 6 be a simple, unclocked inverter?

   No. In this case, the circuit toggles between $A = 1, X = 0, B = 1$ and $A = 0, X = 1, B = 0$ as the clock swings between low and high levels, failing to divide.
2) Can the frequency divider shown in Figure 6 generate an output with a 50% duty cycle?

   Yes. Node X provides a 50% duty cycle (but not nodes A and B).

References

[1] R. Gregorian, "High pass switched capacitor filter section," U.S. Patent 4 210 872, July 1, 1980.
[2] R. Gregorian, Y. Haque, R. Mao, and W. Nicholson, "CMOS switched-capacitor filter for a two-chip PCM voice coder," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1979, pp. 28–29.
[3] D. J. Allstot, R. W. Brodersen, and P. R. Gray, "An electrically programmable analog NMOS second-order filter," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1979, pp. 76–77.
[4] B. J. White, G. M. Jacobs, and G. F. Landsburg, "A monolithic dual tone multi-frequency receiver," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1979, pp. 36–37.
[5] K. Martin and A. S. Sedra, "Strays-insensitive switched-capacitor filters based on bilinear z-transform," *Electron. Lett.*, vol. 15, pp. 365–366, June 1979.
[6] R. Gregorian and G. Temes, *Analog CMOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

SSC