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The Design of An LDO Regulator

Many mixed-signal systems incorporate LDO regulators to generate local supply voltages for various building blocks. LDOs isolate the circuits from one another's noise and from the noise on the global supply, V_{DD}. For optimum performance, the design of each LDO is tailored to the particular cell that it feeds. For example, an LDO developed for a flash analog-to-digital converter is quite different from one serving a VCO.

In this article, we design an LDO for a 5-GHz *LC* VCO and target the following specifications:

- Input voltage: 1.2 V
- Output voltage: 1 V
- Maximum output current: 5 mA
- Power supply rejection> 40 dB up to 10 MHz
- Output noise voltage $<50\,\text{nV}/\sqrt{\text{Hz}}$ at 1 MHz.

The PSRR and tolerable output noise are chosen according to the VCO's supply sensitivity. We elaborate on these points in the next section. We also target a maximum LDO power consumption of 1 mW beyond the $5\,\text{mA}\times 1.2\,\text{V} = 6\,\text{mW}$ that it provides to the load. The design is carried out in the slow-slow corner of 28-nm technology at $T = 75^\circ\text{C}$. The reader is referred to the LDO literature for background information [1]–[5].

LDO/VCO Interface

We wish to regulate the supply voltage of a 5-GHz VCO that operates within a PLL. We assume the VCO is designed for a phase noise of –110 dBc/Hz at a 1-MHz offset and must incur no more than 1 dB of noise penalty due to the LDO. The VCO implementation is shown in Figure 1, along with the LDO. The former employs two capacitor banks, B_1 and B_2, for digital tuning, and MOS varactors, M_{V1} and M_{V2}, for analog control. As phase-noise optimization dictates a PLL bandwidth of no more than a few megahertz, the VCO gain, K_{VCO}, should typically not exceed $2\pi(50\,\text{MHz/V})$. Noting that low-frequency perturbations on V_{out} and V_{cont} have approximately the same effect on the VCO output phase, we express the phase noise due to the LDO random noise, $S_{V,LDO}$, as

$$S_{\phi n}(f) = \frac{K_{VCO}^2}{4\pi^2 f^2} S_{V,LDO}, \tag{1}$$

where f denotes the frequency offset from the carrier. At a 1-MHz offset, this value must be sufficiently below –110 dBc/Hz so as to introduce only 1 dB of penalty. That is, we must have

$$10\log\frac{\frac{K_{VCO}^2}{4\pi^2 f^2} S_{V,LDO} + 10^{-110/10}}{10^{-110/10}} = 1\,\text{dB} \tag{2}$$

at $f = 1\,\text{MHz}$. It follows that $S_{V,LDO} \le 32\,\text{nV}/\sqrt{\text{Hz}}$.

The PSRR is defined as $|V_{out}/V_{DD}|$ in Figure 1 and must remain less than –40 dB. The –40-dB requirement translates to two assumptions as to how "clean" V_{DD} should be. First, its random noise must be less than $100\times 32\,\text{nV}/\sqrt{\text{Hz}}$. Second, any periodic perturbation on V_{DD} must be so small that, with 40 dB of attenuation, it introduces sufficiently low spur levels at the VCO output. If we

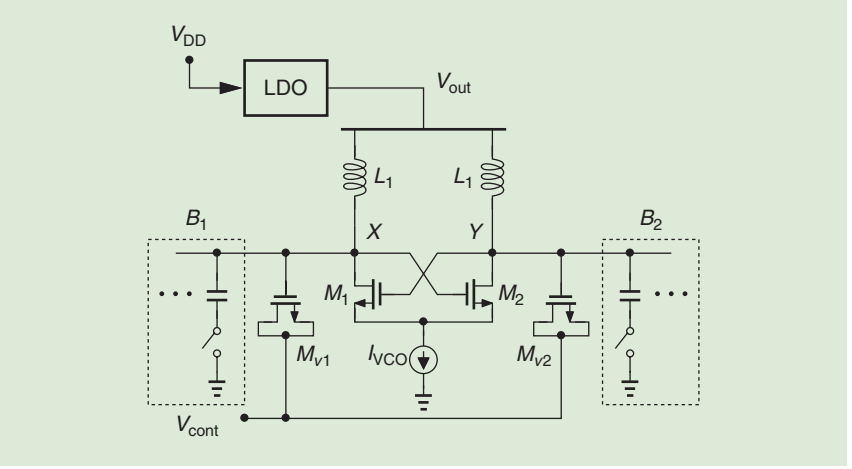

FIGURE 1: A VCO circuit fed by an LDO.

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approximate the V_{DD} perturbation by $V_m \cos \omega_m t$, the normalized spur level is equal to $0.01 K_{VCO} V_m/(2\omega_m)$ at an offset frequency of ω_m. For example, a spur level 60 dB below the carrier at $\omega_m = 2\pi(10\,\text{MHz})$ requires that V_m be less than 40 mV if $K_{VCO} = 2\pi(50\,\text{MHz/V})$.

General Considerations

With a drop of only 200 mV from V_{DD} to V_{out}, the LDO must employ a pass transistor that acts as a current source (rather than a source follower) [5]. The basic topology is displayed in Figure 2(a), where operation amplifier (op amp) A_1 regulates V_{out} by adjusting the gate voltage of M_0. For $V_{out} = 1\,\text{V}$, we have $V_{REF} = (1\,\text{V})R_2/(R_1 + R_2)$; this is the general case. If $V_{REF} = 1\,\text{V}$ is available, we can omit R_1 and R_2 and tie the op-amp input directly to V_{out}.

For analysis and design of the LDO, we wish to attach to its output a simplified model of the VCO. Returning to Figure 1, we observe that the LDO provides a bias current equal to I_{VCO} and sees the two capacitor banks, varactors, and common-mode (CM) parasitics at X and Y. We then model the VCO as depicted in Figure 2(b), where $C_{VCO} = 2C_B + 2C_{var} + 2C_{CM}$ and C_B, C_{var}, and C_{CM} denote the bank, varactor, and CM capacitances, respectively. We assume $I_{VCO} \le 5\,\text{mA}$ and $C_{VCO} = 0.5\,\text{pF}$.

Pass Transistor Design

Transistor M_0 in Figure 2(a) must provide a maximum load current of 5 mA plus that which flows through R_1 and R_2. We should then select $(W/L)_0$ large enough so as to obtain a reasonable V_{GS} for this device. Specifically, as $|V_{DS0}| = 0.2\,\text{V}$, the transistor's overdrive must not exceed this value. For $|I_{D0}| \approx 6\,\text{mA}$, this translates to $(W/L)_0 \ge 100\,\mu\text{m}/30\,\text{nm}$. As explained in [5], the coupling of V_{DD} through this transistor's output resistance, r_{O0}, to V_{out} negligibly affects the PSRR, allowing the minimum length for this device. Such a length is preferable as the capacitances of M_0 contribute to poles at both P and X in Figure 2(a).

Op-Amp Requirements

The LDO's performance hinges upon that of the op amp. The low-frequency PSRR is given by

$$\frac{V_{out}}{V_{DD}} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_1}, \tag{3}$$

where the loop gain is assumed to be much greater than unity [5]. If, for example, $V_{REF} = 0.9\,\text{V}$, we have $1 + R_1/R_2 = 1/0.9$ and hence $A_1 > 100/0.9 \approx 110 \equiv 41\,\text{dB}$ for $\text{PSRR} = -40\,\text{dB}$.

As the LDO is to provide a rejection of 40 dB up to 10 MHz, we conclude that the op amp's open-loop 3-dB BW must exceed this value. For a one-pole design, therefore, the unity-gain BW amounts to $110 \times 10\,\text{MHz} = 1.1\,\text{GHz}$. It is interesting that a seemingly low-frequency LDO demands a fairly wideband op amp. For this reason, we prefer to use only thin-oxide (low-voltage) transistors in the op amp's signal path.

The feedback loop consisting of the pass transistor and the op amp contains several poles, possibly requiring frequency compensation. The output node in Figure 2(a) presents several tradeoffs in this regard. First, if we add capacitance to X so as to improve the supply rejection at high frequencies, the loop becomes less stable, exhibiting peaking in the PSRR. Second, if we reduce $R_1 + R_2$ and hence raise the associated pole frequency, power consumption climbs. In the VCO example of interest here, C_{VCO} and $(R_1 + R_2) \| r_{O0}$ appear to establish an upper bound for the pole frequency at X. For example, $C_{VCO} = 0.5\,\text{pF}$ and $(R_1 + R_2) \| r_{O0} = 1\,\text{k}\Omega$ yield $\omega_X = 2\pi(318\,\text{MHz})$. If ω_X is the first nondominant pole of the loop,

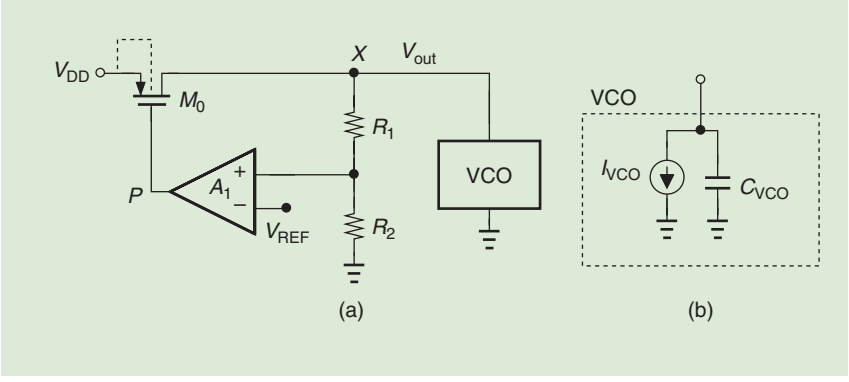

FIGURE 2: (a) A basic LDO topology and (b) the VCO model.

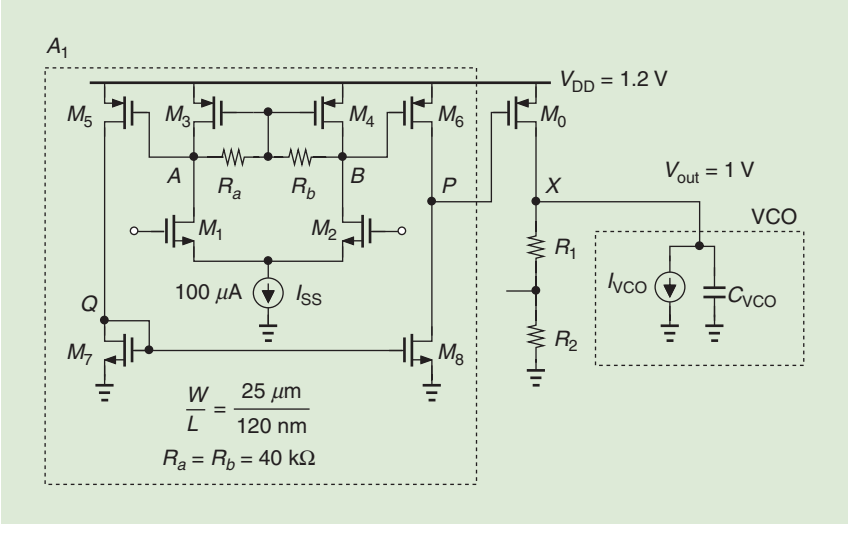

FIGURE 3: A two-stage op amp used in the LDO.

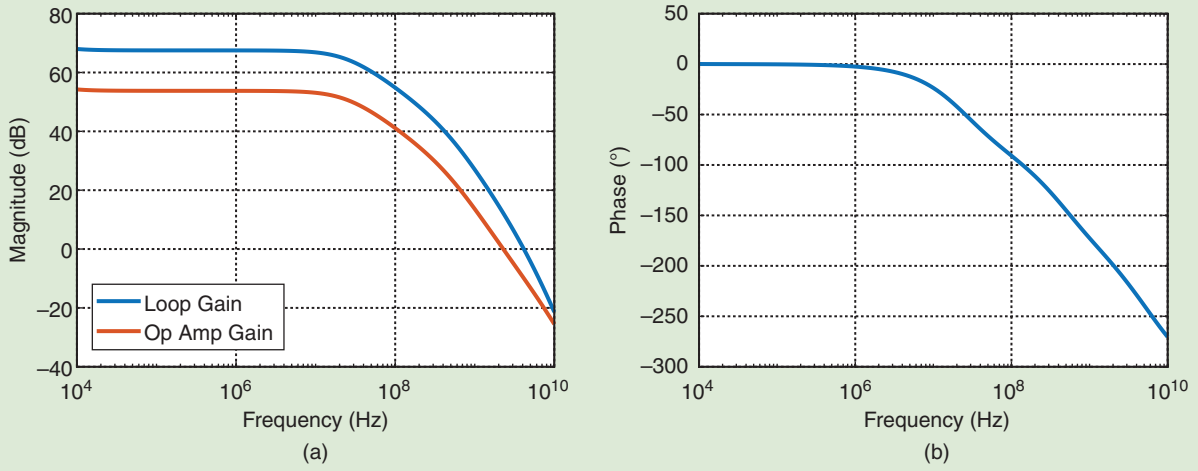

FIGURE 4: The magnitude and phase response of the uncompensated op amp.

the unity-gain bandwidth cannot exceed this value after frequency compensation is applied. It then appears that the 1.1-GHz target stipulated previously is far from reach. Fortunately, pole splitting and pole-zero cancellation resolve this issue.

Op-Amp Design

To obtain the widest bandwidth for a given gain, we should incorporate a cascode op amp, but, in view of the low supply voltage, we opt for a simple two-stage structure. The circuit consists of a differential pair and a stage with a current-mirror load, as shown in Figure 3. Resistors R_a and R_b set the CM level at A and B, respectively, while minimally loading these nodes. This topology avoids cascodes and creates well-defined bias currents for both stages (e.g., I_{D5} is copied from I_{D3}), thus serving as a robust solution. A transistor length of 120 nm provides a high voltage gain, and a large channel area reduces the flicker noise. The op amp draws a supply current of 200 μA.

The LDO loop consisting of A_1 and M_0 contains poles at A (and B), Q, P, and X. We therefore predict the need for frequency compensation.

We simulate the open-loop LDO circuit and arrive at the frequency response depicted in Figure 4. Also shown is the op-amp gain, i.e., from the gates of M_1 and M_2 to node P. From this, we me make two observations. 1) The loop gain falls to unity at $f = 4.1$GHz, where the

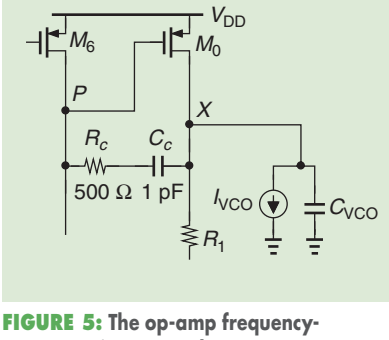

FIGURE 5: The op-amp frequency-compensation network.

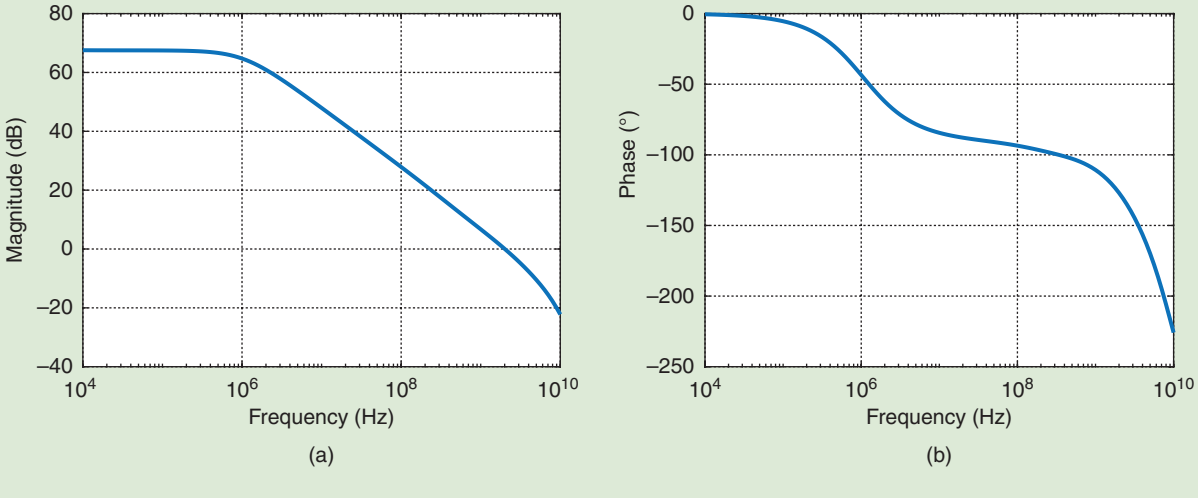

FIGURE 6: The magnitude and phase response of the compensated op amp.

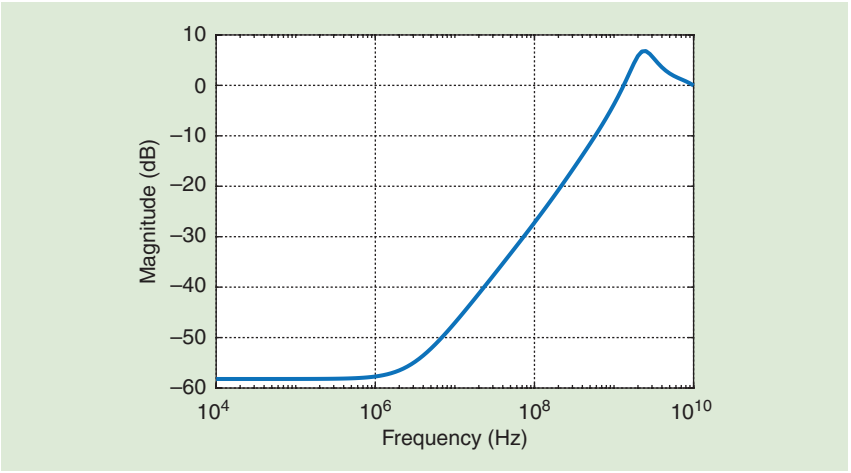

FIGURE 7: The LDO PSRR versus frequency.

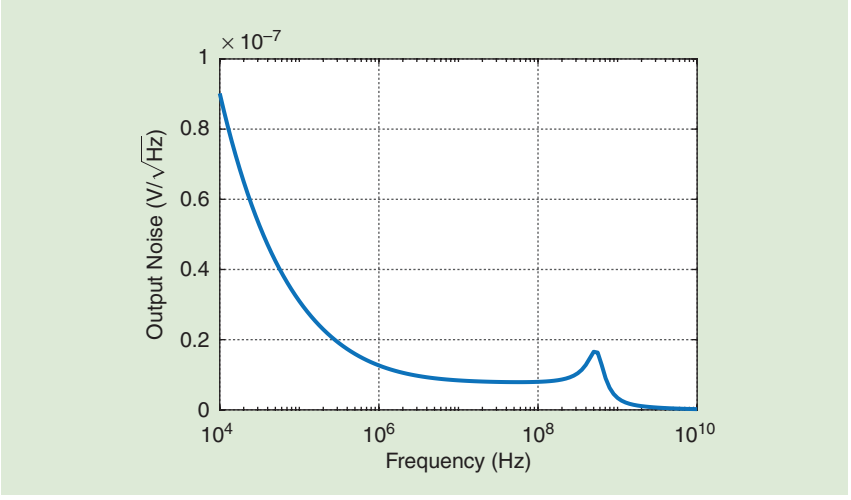

FIGURE 8: The output noise spectrum of the LDO.

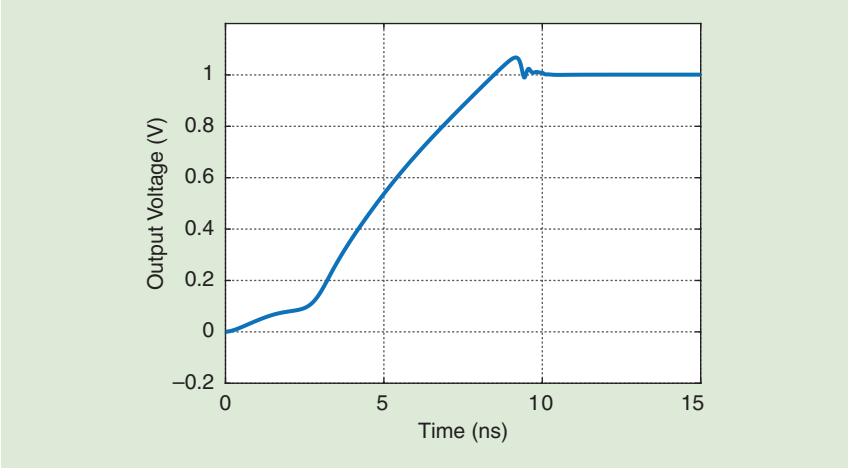

FIGURE 9: The LDO output voltage in response to a ramp on V_{DD}.

phase reaches −230°. The closed-loop LDO is thus unstable. 2) The op amp provides a low-frequency gain of 54 dB and, according to (3), a corresponding PSRR of 53 dB if $1 + R_1/R_2 = 1/0.9$.

Our principal task at this point is to compensate the op amp, e.g., for a phase margin (PM) of approximately 60°. The dominant pole at node P should be lowered. This can be accomplished as shown in Figure 5, where C_c both establishes a dominant pole at P and causes pole slitting. That is, the magnitude of the pole at X now rises to roughly g_{m0}/C_{VCO}. We also insert R_c so as to introduce a zero that cancels the first nondominant pole. The new response is plotted in Figure 6, exhibiting a unity-gain bandwidth of 2 GHz and a PM of 53°.

The Miller compensation method illustrated in Figure 5 is sensitive to the capacitance at node X. We must then ponder what happens if the VCO's discrete capacitor units are switched out so as to increase its oscillation frequency. In such a scenario, the pole at X rises in magnitude, improving the PM. Thus, the worst-case scenario occurs when the tank capacitances are at their maximum.

The closed-loop PSRR is plotted in Figure 7. We observe that the LDO maintains a rejection of at least 40 dB up to 23 MHz.

Output Noise

As explained in the previous section, the output noise voltage of the LDO must be no more than 32 nV/$\sqrt{\text{Hz}}$ at 1 MHz for a 1-dB penalty in the VCO phase noise. At low frequencies, the noise is given by

$$\overline{V_{n,\text{out}}^2} \approx \left(1 + \frac{R_1}{R_2}\right)^2 \overline{V_{nA1}^2}, \qquad (4)$$

where $\overline{V_{nA1}^2}$ denotes the op-amp input-referred noise [5]. Figure 8 plots the output noise spectrum, revealing that it is less than 20 nV/$\sqrt{\text{Hz}}$ beyond a few hundred kilohertz. The phase-noise penalty is therefore negligible.

Transient Response

Although our design has achieved an adequate small-signal PM, we must still examine the circuit's large-signal response. Specifically, we should study the output when the global

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Quantum computing is one of the next frontiers ahead of us, but this area, too, is all about controlling electrons. Here, we are interested in controlling the state of a quantum bit, or qubit for short. There are many types of qubits around today. Figure 12 shows the electronics we use to control a superconducting qubit [3]. The qubit can also be in the form of the spin of a single electron that we trap in a semiconductor well. However, the electronics that control their state are similar. Here, the blocks in red are used to control the state of the qubit. The blocks in green are used to interrogate the qubit, that is, to read the qubit. These building blocks are digital-to-analog converters, analog-to-digital converters, low-pass filters, VCOs, mixers, and amplifiers. What is important here is that, in the semiconductor spin qubit, we use the charge of electrons to control and read the spin of a single electron carrying information. It is, again, about controlling electrons, their charge, and their spin!

What is important here is that, in the semiconductor spin qubit, we use the charge of electrons to control and read the spin of a single electron carrying information.

To summarize, we define *electronics* as the art of controlling electrons for the purpose of information storage, processing, and communication. To store information, we trap electrons on a floating gate or capacitor; to process information, we use transistor circuits to manipulate electrons; and to communicate information, we use circuits to create waves along a wire or in the air. Finally, to put electrons in good use, please scan the QR code in this article with your cell phone to explore videos from Circuit Insights on the SSCS YouTube channel [1].

References

[1] SSCS, *Circuit Insights Playlist*. (2022). [Online Video]. Available: https://www.youtube.com/IEEESolidStateCircuitsSociety/playlists

[2] A. Sheikholeslami, "A circuit to remember [Circuit Intuitions]," *IEEE Solid-State Circuits Mag.*, vol. 14, no. 1, pp. 13–83, Winter 2022, doi: 10.1109/MSSC.2021.3127066.

[3] J. Bardin, "Cryogenic CMOS integrated circuits for control of superconducting quantum computers: Status and challenges," in *Proc. Forum 4, ISSCC*, 2021, pp. 1–62.

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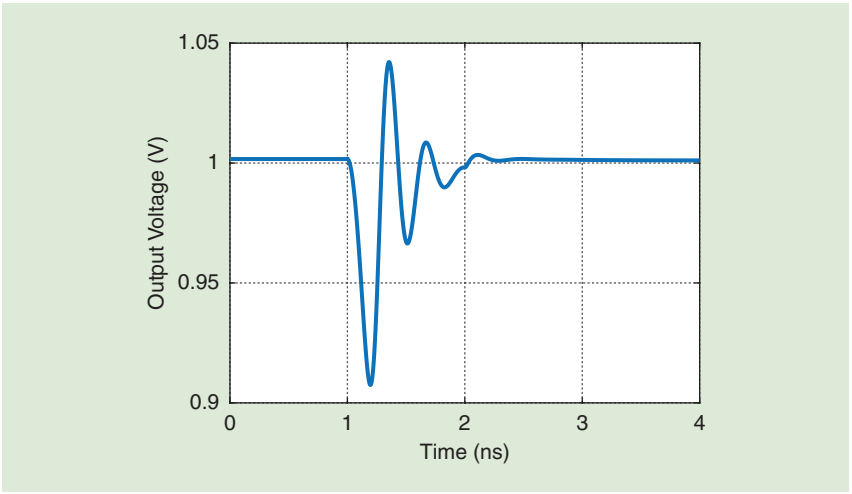

FIGURE 10: The LDO output voltage in response to a ramp in I_{VCO}.

supply or the VCO's tail current source ramps from zero to its nominal value.

Figure 9 plots V_{out} as V_{DD} goes from zero to 1.2 V in 10 ns, suggesting a small amount of ringing as this voltage settles. Similarly, Figure 10 shows the momentary change in V_{out} as I_{VCO} jumps from zero to 5 mA in 1 ns. The loop corrects the perturbation in approximately 2 ns.

References

[1] G. A. Rincon-Mora and P. E. Allen, "Optimized frequency-shaping circuit techniques for LDOs," *IEEE Trans. Circuits Syst., II*, vol. 45, no. 6, pp. 703–710, Jun. 1998, doi: 10.1109/82.686689.

[2] H. J. Shin, S. K. Reynolds, S. Gowda, and D. J. Pearson, "Low-dropout on-chip voltage regulator for low-power circuits," in *Proc. IEEE Symp. Low-Power Electron.*, 1994, pp. 76–77, doi: 10.1109/LPE.1994.573210.

[3] R. J. Miliken, J. Silva-Martinez, and E. Sanchez=Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst., I*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007, doi: 10.1109/TCSI.2007.902615.

[4] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1732–1742, Aug. 2007, doi: 10.1109/JSSC.2007.900281.

[5] B. Razavi, "The low-dropout regulator," *IEEE Solid-State Circuits Mag.*, vol. 11, no. 2, pp. 8–13, Spring 2019, doi: 10.1109/MSSC.2019.2910952.

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