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The Transimpedance Amplifier

Many of today's communication systems incorporate a transimpedance amplifier (TIA). Although the TIA concept is as old as feedback amplifiers [1], it was in the late 1960s and early 1970s that TIAs found widespread usage in optical coupling and optical communication receivers. In a patent filed in 1967, Miller proposes the circuit shown in Figure 1 [2], which consists of two TIAs for converting a photodiode's current to a differential output voltage. Additionally, these amplifiers have become popular in radio-frequency (RF) receivers in the past 10 years [3]. This article deals with TIA design for optical and RF applications.

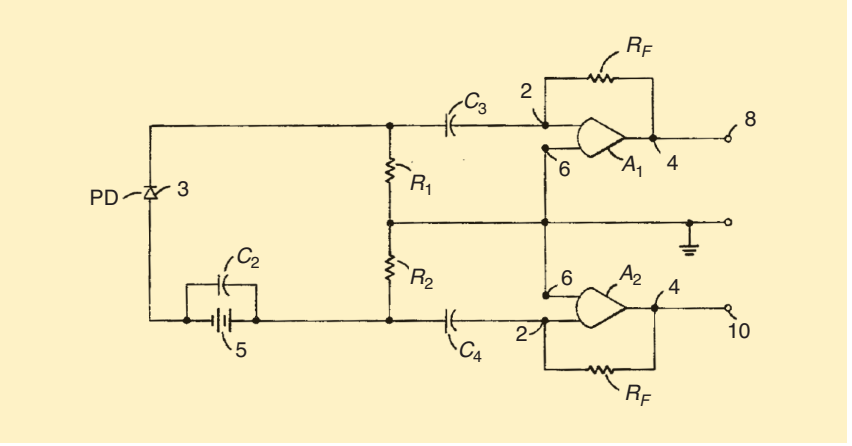

FIGURE 1: The TIA proposed by Miller. PD: photodiode.

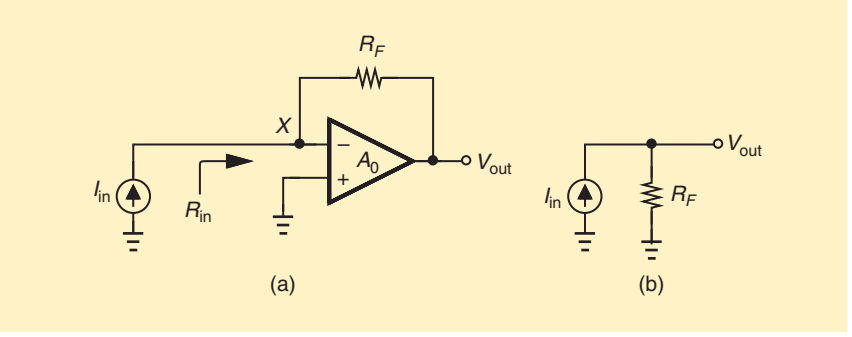

FIGURE 2: (a) The basic TIA structure and (b) use of a resistor to convert current to voltage.

Basic Idea

A TIA employs negative feedback to create a low input impedance. For example, a resistor R_F placed around an amplifier having an open-loop gain of $-A_0$ yields an input resistance equal to $R_{in} = R_F/(1 + A_0)$ [Figure 2(a)]. As such, the circuit is suited to sensing a current, thus acting as a current-to-voltage converter. We define the transimpedance gain as

$$R_T = \frac{V_{out}}{I_{in}} \quad (1)$$

$$= \frac{-I_{in} R_{in} A_0}{I_{in}} \quad (2)$$

$$= -\frac{A_0}{1 + A_0} R_F. \quad (3)$$

If $A_0 \gg 1$, we have $R_T \approx -R_F$.

Of course, a single grounded resistor can perform the same function [Figure 2(b)] and provide the same transimpedance gain. However, the principal difference is that I_{in} sees a low impedance in Figure 2(a) and a high impedance in Figure 2(b). The virtual ground introduced by the TIA proves useful in two cases:

1) If I_{in} incurs a large parasitic capacitance, C_p, to ground, in which case the pole at the TIA input is given by $[R_F C_p/(1 + A_0)]^{-1}$ and that in Figure 2(b) by $(R_F C_p)^{-1}$; i.e., the former potentially achieves a greater bandwidth.
2) If I_{in} suffers from nonlinearity for large voltage swings across it, the TIA reduces these swings by a factor of $1 + A_0$.

We describe in the following how these properties are exploited in receiver design.

TIA Design for Optical Communications

An optical receiver incorporates a photodiode to convert to current the information carried by modulated

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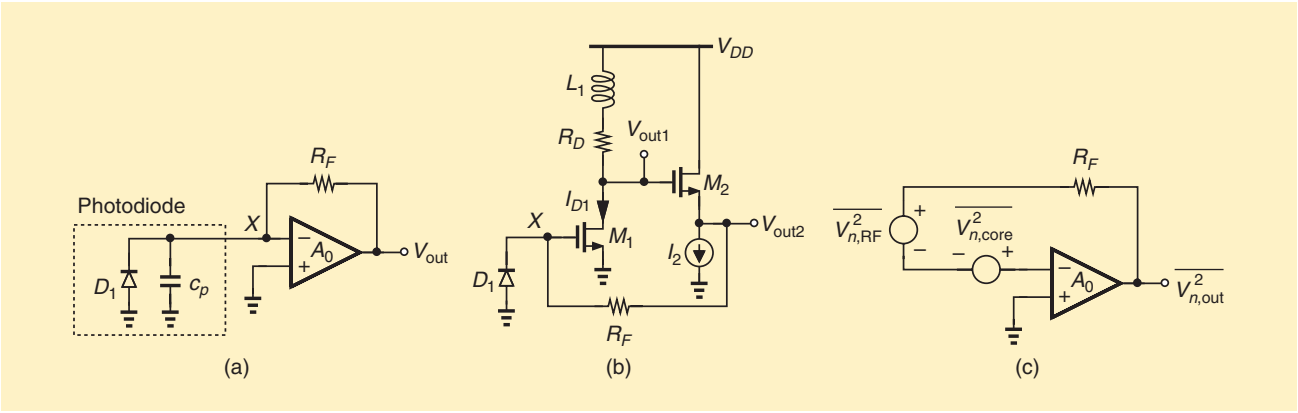

FIGURE 3: (a) A TIA receiving current from a photodiode, (b) circuit implementation, and (c) TIA noise model.

light. The diode suffers from a direct tradeoff between its output current and parasitic capacitance (because the light received by the diode is proportional to its area), necessitating a virtual-ground termination [Figure 3(a)]. Optical receiver TIAs must achieve a wide bandwidth, a low input-referred noise current, and a reasonable gain to minimize the noise contribution of the subsequent stages.

Although simple, the topology of Figure 3(a) faces several challenges. As a rule of thumb, we select the circuit's bandwidth equal to 70% of the data rate, e.g., equal to 28 GHz for a 40-Gb/s system (which implies the open-loop bandwidth must be quite large). This choice minimizes intersymbol interference but must deal with the noise integrated across such a large bandwidth. For these reasons, the core amplifier, A_0, typically includes only one gain stage and one main noise contributor.

Shown in Figure 3(b) is an example consisting of a common-source (CS) amplifier and a source follower. The CS stage can employ inductive peaking to increase the bandwidth. Assuming a voltage gain of about unity for the follower, we approximate the open-loop gain by $A_0 = g_{m1} R_D$, obtaining

$$R_T = \frac{-g_{m1} R_D}{1 + g_{m1} R_D} R_F \tag{4}$$

at low frequencies. The output voltage is available at V_{out1} and at V_{out2}, with the former exhibiting a more design-friendly dc level but also a higher output impedance.

To determine the input-referred noise current, we leave the input port open; model the noise of M_1, R_D, M_2, and I_2 by a voltage quantity $\overline{V_{n,core}^2}$ at the gate of M_1; and note that R_F also contributes noise [Figure 3(c)]. Calculating $\overline{V_{n,out}^2}$ and dividing it by R_T^2, we have

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,core}^2} + \overline{V_{n,RF}^2}}{R_F^2} \tag{5}$$

$$= \frac{\overline{V_{n,core}^2}}{R_F^2} + \frac{kT}{R_F}. \tag{6}$$

If we target, e.g., $I_{n,in} = 10\,\text{pA}/\sqrt{\text{Hz}}$ and choose $R_F = 1\,\text{k}\Omega$, then $V_{n,core}$ must not exceed $9.1\ \text{nV}/\sqrt{\text{Hz}}$. We prefer that only M_1 be the main noise contributor. In practice, however, the limited voltage drop across R_D makes this resistor's contribution significant as well.

The TIA topology of Figure 3(b) must satisfy the bias condition $V_{GS1} + V_{GS2} + I_{D1} R_D = V_{DD}$, a difficult issue at low supply voltages. Let us then omit the source follower [Figure 4(a)], recognizing that the voltage headroom equation reduces to $V_{GS1} + I_{D1} R_D = V_{DD}$. That is, this circuit can incorporate a greater R_D and achieve a higher open-loop gain. It can be shown that the input resistance rises to

$$R_{in} = \frac{R_D + R_F}{1 + g_{m1} R_D}, \tag{7}$$

and the transimpedance gain is given by

$$R_T = \frac{R_D(1 - g_{m1} R_F)}{1 + g_{m1} R_D}. \tag{8}$$

To further ameliorate the voltage headroom problem, we can inject a constant current, I_b, into R_F to create a voltage drop of, say, 300 mV [Figure 4(b)], obtaining $V_{GS1} - I_b R_F + I_{D1} R_D = V_{DD}$. As a result, R_D can sustain a greater voltage drop and yield a higher open-loop gain.

An alternative TIA topology employs a CMOS inverter as the core

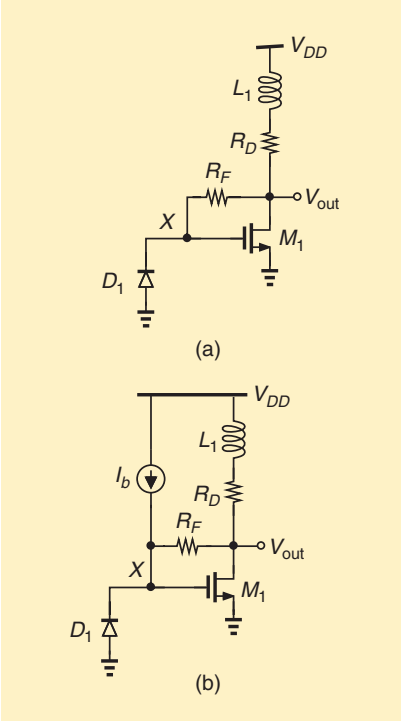

FIGURE 4: (a) A TIA using a common-source stage with feedback and (b) use of a constant current source to shift the output dc level down.

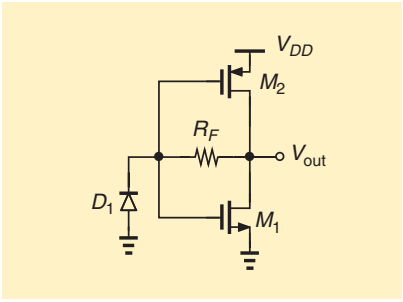

FIGURE 5: A TIA using an inverter.

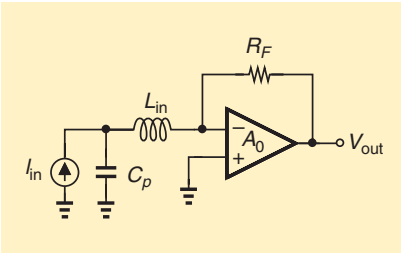

FIGURE 6: A TIA with series peaking.

amplifier [4]. Depicted in Figure 5, this structure eliminates the noise due to R_D in Figure 4(a). The input resistance and gain can be found from (7) and (8), respectively, if $R_D \to \infty$ and g_{m1} is replaced with $g_{m1} + g_{m2}$,

$$R_{in} \approx \frac{1}{g_{m1} + g_{m2}} \tag{9}$$

$$R_T \approx \frac{1}{g_{m1} + g_{m2}} - R_F. \tag{10}$$

This topology exhibits a lower input-referred noise current but a higher input capacitance.

Optical receiver TIAs often utilize series inductive peaking to increase the input bandwidth. As shown in Figure 6, an on-chip inductor, L_{in}, creates a second-order network at the input, yielding a bandwidth of

$$\omega_{-3dB} \approx \frac{\sqrt{2}(1 + A_0)}{R_F C_p}, \tag{11}$$

if the damping factor is chosen equal to $\sqrt{2}/2$.

TIA Design for RF Receivers

A common situation in RF design is that the receiver senses a weak desired signal along with a strong interferer (blocker). Upon traveling through the receive chain, the blocker is amplified and can introduce substantial distortion. The chain must therefore be designed for sufficient linearity up to the stage(s) where the blocker is filtered. In general, as the voltage swing at each interface is minimized, the linearity improves. We then contemplate the use of current-mode signals and low impedance levels to reduce the voltage swings.

A common situation in RF design is that the receiver senses a weak desired signal along with a strong interferer (blocker).

Figure 7(a) illustrates a typical modern RF receiver front end [3]. The signal and blocker combination sensed by the antenna drives a G_m stage (a voltage-to-current converter), and the resulting current I_{out} is applied to a passive mixer to generate a baseband current I_{BB}. The low impedance established by the TIA at Q and P reduces the voltage swings at these nodes, thus improving the linearity of the G_m stage and the mixer switches. This means that the large blocker can be tolerated at least up to node Q.

The TIA in Figure 7(a) must still meet stringent noise, linearity, and gain requirements. The input-referred noise current, given by (6) and divided by G_m^2, must be sufficiently smaller than the input-referred noise voltage of the G_m stage. The TIA must also handle large voltage swings at its output with negligible nonlinearity. Moreover, the TIA must provide enough gain to overcome the noise of the subsequent stages. The large blocker level still poses two tradeoffs in TIA design, i.e., one between the core amplifier's bandwidth and the linearity at point Q and another between the closed-loop gain and the output voltage headroom.

Let us consider the first tradeoff, recognizing that amplifier A_0 in Figure 7(a) generates V_{BB} such that $V_{BB}/R_F \approx I_{BB}$, and hence V_Q remains close to zero. In other words, if I_{BB} varies fast and Q, is to act as a virtual ground, then V_{BB} must track I_{BB}. This means that the amplifier must have a sufficiently wide bandwidth. Now, we note that the center frequencies of the desired channel and the blocker are translated by the mixer to zero and $f_1 - f_0$, respectively [Figure 7(b)]. Thus, the TIA must create a virtual ground at $f_1 - f_0$ to minimize the voltage swing at Q even though the desired channel extends to only $f = f_{ch/2}$. In GSM, for example, $f_1 - f_0$ can be 20 MHz while $f_{ch/2} = 100$ kHz, requiring that the TIA core amplifier provide enough gain at 20 MHz. As a numerical example, suppose the blocker swing reaches $0.5\,V_{pp}$ at the TIA output; then, for the swing at Q to remain below $50\,mV_{pp}$, we must have $A_0 = 10$ at 20 MHz. This

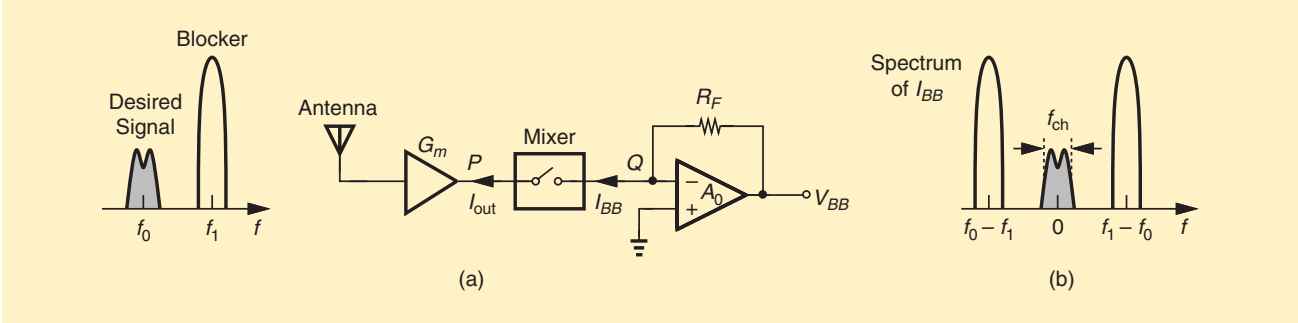

FIGURE 7: (a) An RF receiver using a TIA in the baseband and (b) the spectrum of baseband signal.

translates to a unity-gain bandwidth of about 200 MHz for the core amplifier. But an open-loop gain of 10 may not yield enough linearity for the amplifier at the blocker frequency. For this reason, A_0 is typically realized as a high-gain operational amplifier.

The second tradeoff in Figure 7(a) arises due to the large blocker current arriving from the mixer. Suppose, for example, $R_F = 2$ kΩ and I_{BB} has a peak value of 1 mA, demanding a peak voltage swing of 1 V at the TIA output. This makes the amplifier design more difficult. If R_F is reduced to ease the situation, its noise contribution and the noise of the following stages become problematic.

Both of the foregoing tradeoffs can be relaxed if we introduce filtering at the input and within the TIA. As shown in Figure 8, capacitor C_1 shunts most of the blocker current to ground, and capacitor C_2 reduces the TIA gain at frequencies beyond f_{ch}. These two effects lead to much smaller blocker-induced voltage swings at Q and in V_{BB}.

The use of C_1 at node Q raises a concern regarding the stability of the TIA feedback loop. In fact, without C_2, the feedback resistor and C_1 form a pole that can significantly degrade the phase margin. Capacitor C_2 adds a zero in the feedback path, improving the stability to some extent. We can express the feedback factor as

$$\frac{V_Q}{V_{BB}}(s) = \frac{R_F C_2 s + 1}{R_F (C_1 + C_2) s + 1}, \quad (12)$$

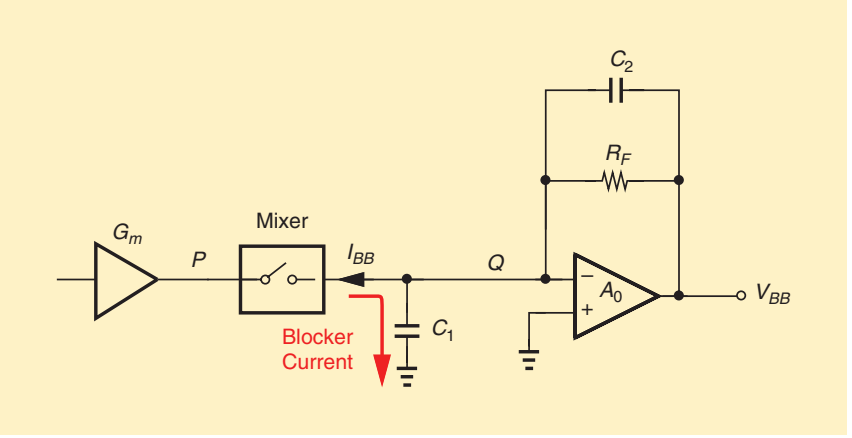

FIGURE 8: The use of capacitors to suppress blocker.

where we have assumed that the mixer presents an infinite output impedance. The TIA phase margin changes by an amount equal to

$$\theta = \tan^{-1}(R_F C_2 \omega_u) - \tan^{-1}[R_F (C_1 + C_2)\omega_u], \quad (13)$$

where ω_u denotes the frequency at which the loop gain drops to unity. We have

$$\theta = -\tan^{-1}\frac{R_F C_1 \omega_u}{1 + R_F^2 (C_1 + C_2) C_2 \omega_u^2} \quad (14)$$

$$\approx -\tan^{-1}\frac{C_1}{R_F (C_1 + C_2) C_2 \omega_u}, \quad (15)$$

because $R_F^2 (C_1 + C_2) C_2 \omega_u^2$ is typically much greater than unity. Due to this degradation, C_1 and C_2 generally cannot remove the blocker entirely, which means A_0 must still handle large swings at its output.

Questions for the Reader

1) Calculate the input-referred noise current of the TIA shown in Figure 5. Does this noise increase or decrease if we consider channel-length modulation?
2) How should L_{in} be chosen in Figure 6 so that we have $\omega_{-3dB} \approx [\sqrt{2}(1 + A_0)] R_F C_p$?

Answers to Last Issue's Questions

1) How does the counterintermodulation (CIM) result in Figure 9(c) change if the lower mixer's output is added to that of the top mixer's?

   If the lower signal is added, $X_{out}(f)$ contains a component at $\omega_{LO} - \omega_{BB}$ and another at $3\omega_{LO} + 3\omega_{LO} + \omega_{BB}$. As a result of nonlinearity in the amplifier, $X_m(f)$ exhibits a CIM product at $\omega_{LO} + 3\omega_{BB}$.

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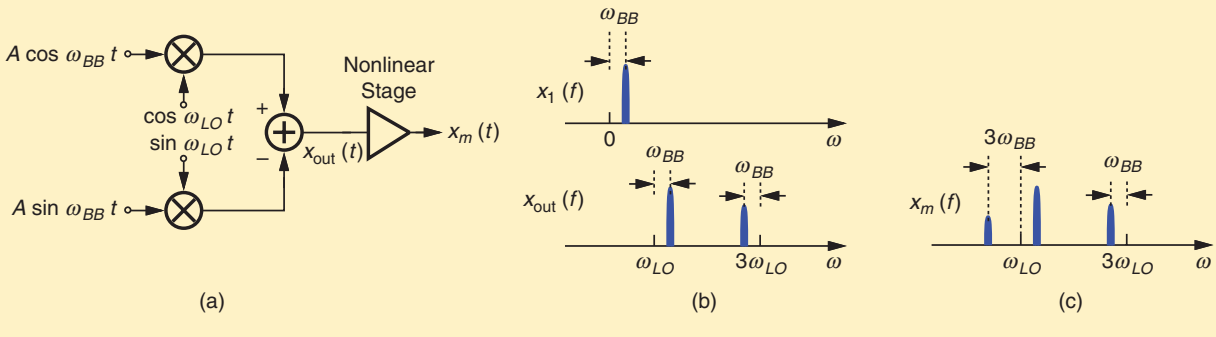

FIGURE 9: The counterintermodulation due to amplifier nonlinearity.

Claire Chen Speaks at WiC Networking Luncheon at A-SSCC

The IEEE Solid-State Circuits Society Women in Circuits (WiC) Committee hosted a networking luncheon in conjunction with the Asian Solid-State Circuits Conference (A-SSCC) in Tainan, Taiwan, on 6 November 2018. The event attracted 10 attendees from both academia and industry. Dr. Claire Chen, director of power management BD, TSMC, gave an inspiring talk during the event, sharing her career and life experiences. Connections were made, and delicious food was consumed.

—Ping-Hsuan Hsieh

(From left) Tanja Chen, Marvis Wu, Chia-Hsin Lee, Chia-Ling Wei, Ping-Hsuan Hsieh, Claire Chen, Neha Priyadarshini, Debby Wu, and Vita Pi-Ho Hu.

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A CIRCUIT FOR ALL SEASONS

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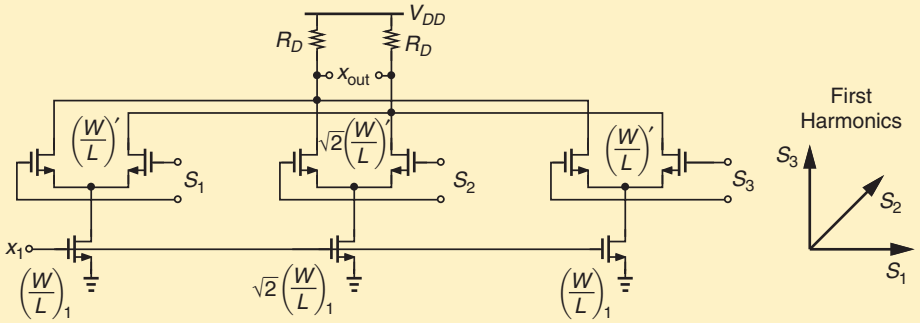

FIGURE 10: An active implementation of a harmonic-rejection mixer.

2) Calculate the gain of the mixer shown in Figure 10 with the aid of the first harmonic phasors shown.

For a single active mixer cell with load resistors equal to R_D and an input transconductance of g_m, the conversion gain is equal to $(2/\pi)g_m R_D$. In Figure 10, we have three cells with transconductances equal to g_m, $\sqrt{2}\,g_m$, and g_m and outputs that are summed with 0º, 45º and 90º phases. The overall gain is thus given by

$$A_v = (\sqrt{2} + \sqrt{2})(2/\pi)g_m R_D. \quad (16)$$

By comparison, if all three cells are driven by the same local oscillator phase, then the total gain is equal to $(1 + 1 + \sqrt{2})(2/\pi)g_m R_D$, about 1.6 dB higher.

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