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The Design of a Biquadratic Filter

Biquadratic filters ("biquads") are commonly used in radio frequency (RF) receivers to remove unwanted signals ("blockers") and noise. We have studied the basic properties of such filters in [1] and pointed to the Tow-Thomas (TT) biquad as an efficient implementation. In this article, we design a continuous-time low-pass filter (LPF) based on this topology for Wi-Fi receivers. We aim for the following performance:

- bandwidth (BW): programmable from 10 MHz to 80 MHz
- adjacent-channel rejection: 25 dB
- alternate-adjacent channel rejection: 50 dB
- output 1-dB compression point: $P_{1dB} \equiv 1.2\,V_{pp}$
- input-referred noise: $10\,nV/\sqrt{Hz}$
- power consumption $< 5\,mW$.

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The reasons for these performance targets become clear below. We should remark that the 1-dB compression point results from nonlinearity and represents the peak-to-peak output voltage at which the in-band filter gain drops by 1 dB.

We carry out the design in the slow–slow corner of 28-nm CMOS technology, assuming a supply voltage of $1\,V - 5\%$ and $T = 75\,^{\circ}C$. The reader is referred to the literature for additional background information [2], [3], [4], [5].

The adjacent and alternate-adjacent channels may be occupied by other users and can carry power levels higher than the desired channel.

Filter Environment

Shown in Figure 1(a) is a generic direct-conversion RF receiver. The signal sensed by the antenna travels through a low-noise amplifier (LNA) and quadrature downconversion mixers, producing baseband signals x_I and x_Q. These components are then applied to LPFs and digitized by analog-to-digital converters (ADCs). We focus on the signal path between each mixer and the corresponding ADC.

To determine the performance required of the baseband filters, we begin with Wi-Fi specifications, specifically, the RF channel BW, BW_{ch}, and the blocker levels. Depicted in Figure 1(b), BW_{ch} can be as narrow as 20 MHz or as wide as 160 MHz around a carrier frequency, f_c, in the range of 6 GHz. The adjacent and alternate-adjacent channels may be occupied by other users and can carry power levels higher than

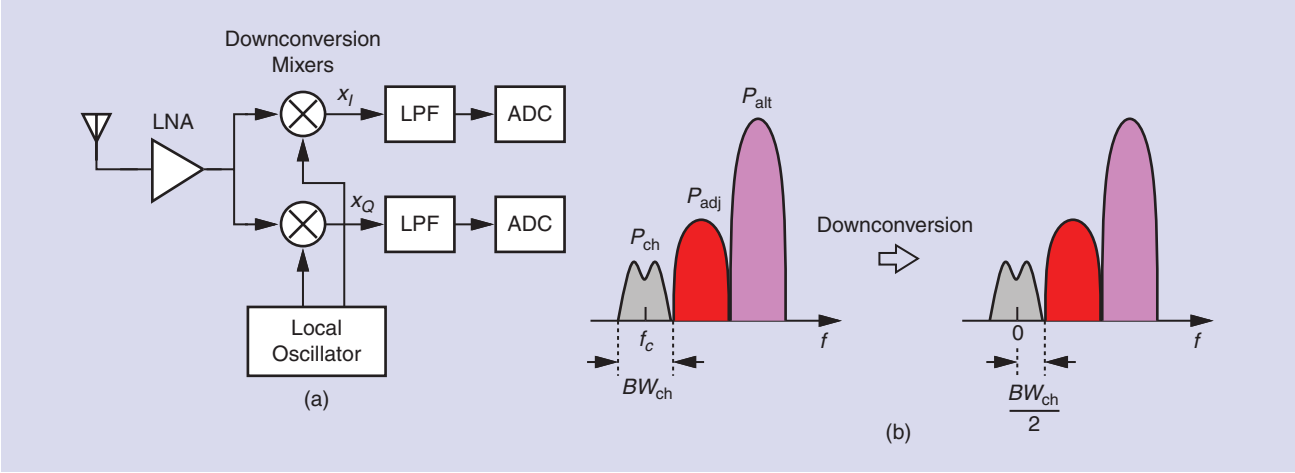

FIGURE 1: (a) A generic receiver environment and (b) illustration of adjacent and alternate-adjacent channel powers. ADC: analog-to-digital converter.

the desired channel. For example, for $BW_{ch} = 20\,\text{MHz}$ and a data rate, r_b, of 6 Mb/s, $P_{adj}/P_{sig} \equiv 16\,\text{dB}$ and $P_{alt}/P_{ch} \equiv 32\,\text{dB}$. For the same channel BW and $r_b = 54\,\text{Mb/s}$, the blocker levels are relaxed by 17 dB, but the selectivity of the filter is dictated by the former case. In recent generations of Wi-Fi, BW_{ch} can reach 160 MHz, while the blocker levels remain similar to the foregoing values.

For baseband filters to suppress blockers, a fourth- or fifth-order transfer function is typically necessary. We assume that the mixers in Figure 1(a) drive transimpedance amplifiers (TIAs) having a first-order response (Figure 2) and implement the following LPFs as a cascade of two biquads.

The next design target of interest is the filter linearity. We identify two mechanisms that can corrupt the desired signal if the filter's op amps are not linear enough. First, it is possible that third-order intermodulation between the adjacent and alternate channels gives rise to excessive noise in the desired channel [Figure 3(a)]. Second, the desired signal itself may be so large that it causes compression in the op amps, thus experiencing distortion the signal [Figure 3(b)]. In our design, the latter effect proves more stringent than the former and demands a sufficiently high 1-dB compression point at the output of the LPF.

We estimate the required P_{1dB} as follows. Wi-Fi signals exhibit a variable envelope characterized by a "peak-to-average ratio" of about 6 dB. This means that the stages processing such signals must provide a P_{1dB} about 6 dB greater than the "average" signal swing. (We say the *backoff* from P_{1dB} is 6 dB.) In addition, the baseband ADCs must avoid overrange (saturation) and, therefore, offer an input range about 6 dB wider than the average signal level. Assuming a value of $0.6\,V_{pp}$ for this level, we target a peak-to-peak differential swing of 1.2 V for both the ADCs' input range and the output 1-dB compression point of the filters.

The input-referred noise of the LPFs proves critical as well. Suppose the RF front end and the TIA in Figure 2 provide a voltage gain of 30 dB. Targeting an overall RX noise figure (NF) of 4 dB, we design the LPFs so that they do not raise the NF by more than 0.2 dB. We construct the equivalent circuit shown in Figure 4, where $A_1 = 30\,\text{dB}$ denotes the voltage gain from the antenna's Thevenin voltage to the TIA output, $\overline{V_{n1}^2}$ represents the total noise spectral density observed at the output of the TIA, and $\overline{V_{n2}^2}$ models the LPF input-referred noise.

The computation of the tolerable LPF noise proceeds as follows. Excluding $\overline{V_{n2}^2}$ in Figure 4, we write:

$$\text{NF} = \frac{1}{4kTR_s}\frac{\overline{V_{n1}^2}}{A_1^2} = 3.8\,\text{dB}. \qquad (1)$$

If $R_s = 50\,\Omega$ and $T = 375\,K$, we have $\overline{V_{n1}^2} = 2.5\times10^{-15}\,V^2/\text{Hz}$. We now include $\overline{V_{n2}^2}$ and write:

$$\frac{1}{4kTR_s}\frac{\overline{V_{n1}^2} + \overline{V_{n2}^2}}{A_1^2} = 4\,\text{dB} \qquad (2)$$

obtaining

$$\sqrt{\overline{V_{n2}^2}} = 10\,\text{nV}/\sqrt{\text{Hz}}\,. \qquad (3)$$

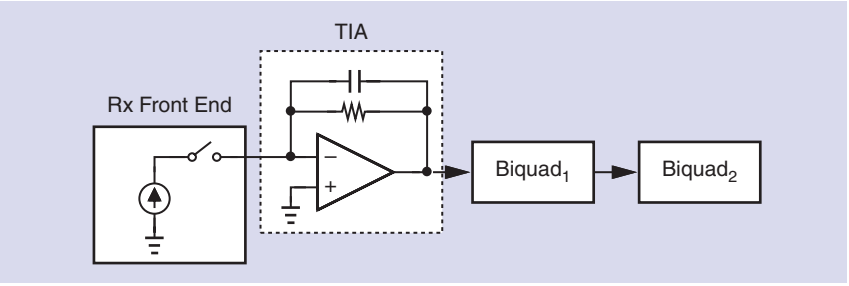

FIGURE 2: The interface between the RF front end and the baseband.

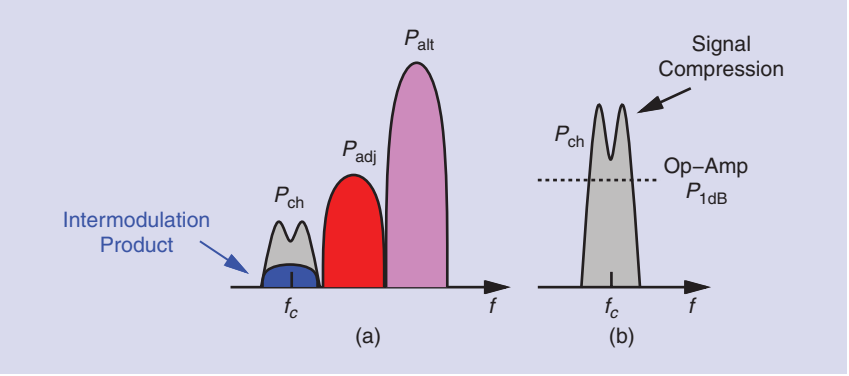

FIGURE 3: Effects of nonlinearity: (a) intermodulation and (b) signal compression.

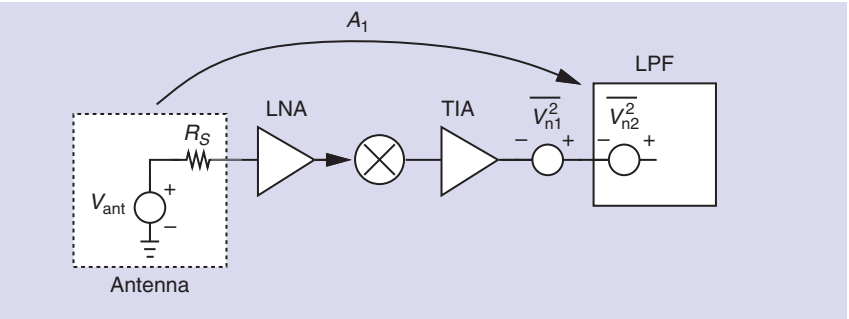

FIGURE 4: The receiver noise model.

Tow-Thomas Biquad

As explained in [1], the TT biquad can be viewed as a negative-feedback loop containing two integrators [Figure 5(a)]. Local feedback around one (indicated by α) introduces loss, thereby stabilizing the overall circuit. Shown in Figure 5(b) is the differential realization of the biquad. We write the transfer function as

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_v \omega_n^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \tag{4}$$

where

$$A_v = \frac{R_F}{R_1} \tag{5}$$

$$\omega_n = \frac{1}{\sqrt{R_3 R_F C_1 C_2}} \tag{6}$$

$$Q = R_2 \sqrt{\frac{C_1}{R_3 R_F C_2}}. \tag{7}$$

It can also be shown that the 3-dB BW is given by

$$\omega_{3dB} = \frac{\omega_n}{\sqrt{2}} \times \sqrt{-\left(\frac{1}{Q^2} - 2\right) + \sqrt{\left(\frac{1}{Q^2} - 2\right)^2 + 4}}. \tag{8}$$

We typically select Q in the range of $\sqrt{2}/2$ to 1. The corresponding 3-dB BW varies from ω_n to $1.27\omega_n$. The results expressed by (5) to (7) reveal two attributes of the TT biquad. First, resistor R_1 can define or adjust the passband gain, A_v, without affecting ω_n or Q. Second, ω_n is independent of R_2 whereas $Q \propto R_2$. We hereafter assume $Q = 1$.

Noise Considerations

The noise in the TT biquad arises from the resistors and the op amps. It is desirable to choose a fairly small value for R_1 in Figure 5(b) so as to both reduce its contribution and raise A_v. However, an excessively low R_1 loads the TIA in Figure 2. If, for example, $R_1 = 1\,k\Omega$, then the two R_1s produce $2 \times 4kTR_1 \equiv 5.75\,nV/\sqrt{Hz}$, leaving little margin for other devices' contributions before we reach our target of $10\,nV/\sqrt{Hz}$. We then decrease R_1 to $500\,\Omega$ and surmise that the lesser noise voltage of $5.75/\sqrt{2}\,nV/\sqrt{Hz} = 4.1/\sqrt{Hz}$ can be accommodated in the overall filter design.

To minimize the noise arising from the second integrator in Figure 5(b), we wish to maximize the in-band (dc) gain of the first, i.e., select a high R_2/R_1 ratio. However, (7) suggests that raising R_2 may lead to an excessively large Q and hence unacceptable peaking in the filter's frequency response.

Programmable BW

Wi-Fi requires that the baseband filters' BW, f_{3dB}, be programmable from 10 MHz to 80 MHz. As mentioned above, $f_{3dB} \approx 1.27\omega_n/(2\pi)$, necessitating programmable values in (6). But we wish to maintain a constant Q. We must therefore adjust C_1 and C_2 without changing their ratio. For example, we can double both so as to halve f_{3dB}.

Effect of Op-Amp Poles

The biquad transfer function expressed by (4) assumes ideal op amps. If the op amps exhibit their own poles, the loop phase margin degrades and the frequency response incurs greater peaking. It is shown in [1] that, for these poles to raise the peaking by no more than 1 dB, we must have:

$$A_0\omega_0 \geq 14\omega_n \tag{9}$$

where A_0 and ω_0 denote the open-loop gain and 3-dB BW of each op amp, respectively. Since the overall biquad BW is equal to $1.27\,\omega_n$, the unity-gain BW, $A_0\omega_0$, must be about 11 times the desired filter BW. This rule of thumb proves useful in the design of the op amps. In our Wi-Fi environment, f_{3dB} ranges from 10 MHz to 80 MHz, demanding a unity-gain BW as high as 880 MHz.

It is possible that the required wide BW translates to high power consumption for the op amps. We can instead design the biquad for a lower Q and allow the op amps' poles to raise it to about 1. As explained below, this remedy is not necessary in our design.

Effect of Finite Op-Amp Gain

We expect that the biquad characteristics depart from the design targets if the op amps do not offer sufficient gain. From a small-signal perspective, the Q and the BW may be affected. Denoting the

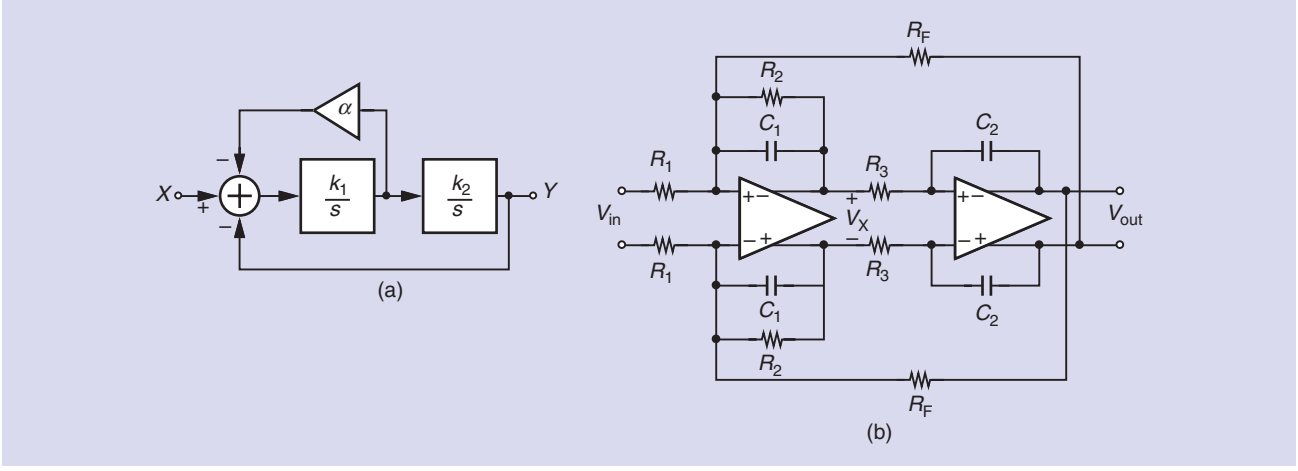

FIGURE 5: (a) The block diagram of TT filter and (b) its implementation.

open-loop gain of the op amps in Figure 5(b) by A_0 and assuming $A_0 \gg 1$, we have

$$\frac{V_{out}}{V_{in}} = \frac{R_2 R_F A_0^2}{as^2 + bs + c} \tag{10}$$

where

$$a = (A_0+1)^2 R_1 R_2 R_3 R_F C_1 C_2 \tag{11}$$

$$b = [R_2 R_F + R_1 R_2 + (A_0+1) R_1 R_F](A_0+1) \times R_3 C_2 + (A_0+1) R_1 R_2 R_F C_1 \tag{12}$$

$$c = R_2 R_F + R_1 R_2 + (A_0+1) R_1 R_F + (A_0+1)^2 R_1 R_2. \tag{13}$$

It follows that

$$\omega_n = \sqrt{\frac{c}{a}} \tag{14}$$

$$Q = \frac{\sqrt{ac}}{b} \tag{15}$$

As an example, suppose we target a BW of $f_{3dB} = 12.5$ MHz with $Q = 1$ and select $R_1 = 500\,\Omega$, $R_2 = R_3 = R_F = 2$ kΩ, and $C_1 = C_2 = 8$ pF. If $A_0 = 10$, then (14) and (15), respectively, yield $\omega_n = 2\pi(10.6\,\text{MHz})$ and $Q = 0.69$ and, hence from (8), $f_{3dB} = 10.3$ MHz. Thus, a low op-amp gain leads to a narrower BW and a smaller Q.

We can restore f_{3dB} by simply reducing C_1 and C_2. However, a low op-amp gain may not yield the desired filter linearity. For this reason, we aim for a gain of several hundred.

Effect of Op-Amp Noise

Our stipulated noise-figure penalty of 0.2 dB requires close attention to the noise contributed by the two op amps in Figure 5(b). With the aid of the low-frequency model illustrated in Figure 6, we have

$$\overline{V_{n,out}^2} = \left(\frac{R_F}{R_F \| R_1 \| R_2}\right)^2 \overline{V_{n1}^2} + \left(\frac{R_F}{R_2}\right)^2 \overline{V_{n2}^2}. \tag{16}$$

Interestingly, and unfortunately, V_{n1} experiences a gain *greater* than that seen by the main input voltage, R_F/R_1. The input-referred noise is thus given by

$$\overline{V_{n,in}^2} = \left(\frac{R_1}{R_F \| R_1 \| R_2}\right)^2 \overline{V_{n1}^2} + \left(\frac{R_1}{R_2}\right)^2 \overline{V_{n2}^2}. \tag{17}$$

For our previous example, wherein $R_1 = 500\,\Omega$ and $R_2 = R_3 = R_F = 2\,\text{k}\Omega$, we have

$$\overline{V_{n,in}^2} = 2.25\,\overline{V_{n1}^2} + 0.25\,\overline{V_{n2}^2}. \tag{18}$$

Effect of Finite Op-Amp Output Resistance

Typical CMOS op amps exhibit a fairly high output resistance, R_{out}. We must then determine how R_{out} affects the filter performance. To gain insight, let us consider a single integrator, shown in Figure 7(a), where the op amp is modeled by a finite gain and a finite R_{out}. We have

$$\frac{V_{out}}{V_{in}} = -\frac{-R_{out} C_1 s + A_0}{[(A_0+1)R_1 + R_{out}]C_1 s + 1} \tag{19}$$

obtaining a zero, $\omega_z = A_0/(R_{out} C_1)$, and a pole,

$$\omega_p = \frac{-1}{[(A_0+1)R_1 + R_{out}]C_1}. \tag{20}$$

The pole frequency can also be derived by noting that C_1 and R_{out} in Figure 7(a) experience the Miller effect, yielding the equivalent circuit depicted

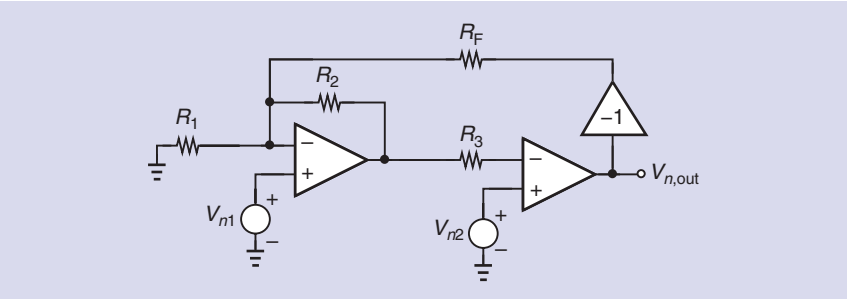

FIGURE 6: The biquad low-frequency model for noise calculation.

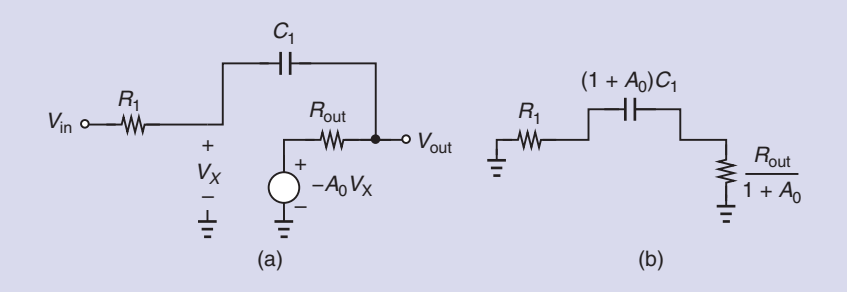

FIGURE 7: (a) The lossy integrator model and (b) an alternative view.

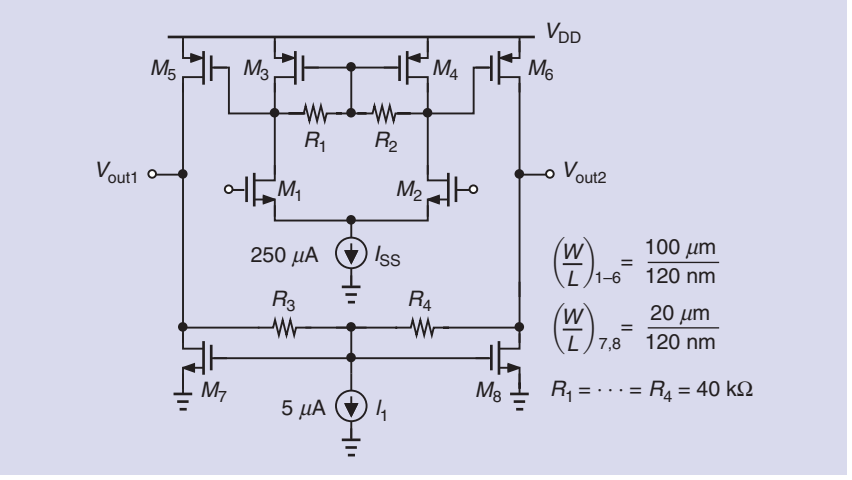

FIGURE 8: The op-amp design.

in Figure 7(b) and, hence, a time constant of $[R_1 + R_{out}/(1+A_0)](A_0+1)C_1$.

Since $|\omega_z| \gg |\omega_p|$, we say R_{out} simply lowers the pole frequency by a small amount, a benign effect.

A more critical issue is that the op-amp output resistance leads to a lower equivalent open-loop gain in the presence of resistive loads. In the TT topology of Figure 5(b), R_2 and R_3 load the first integrator, and R_F loads the second.

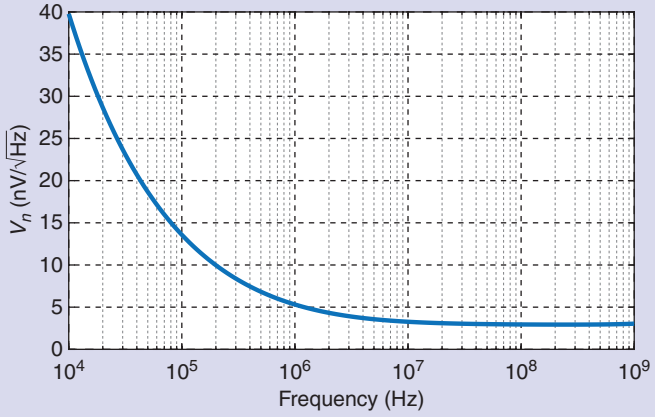

FIGURE 9: Simulated input-referred noise of the op amp.

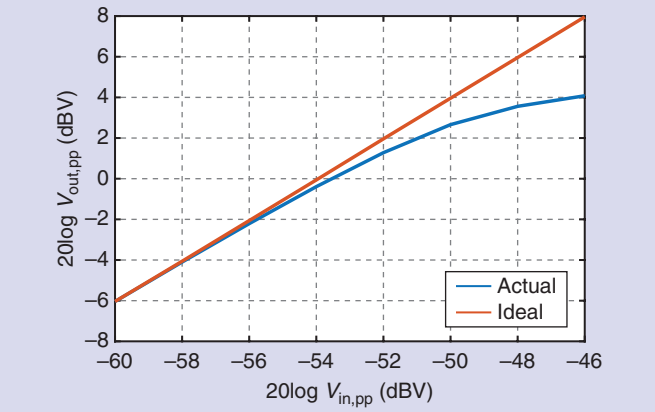

FIGURE 10: The op-amp input–output characteristic.

Op-Amp Design

The four op amps used in the biquads of Figure 2 need not adopt the same topology or the same design values. In fact, the first op amp in Biquad_1 must achieve a low input-referred noise voltage, about $5\text{nV}/\sqrt{\text{Hz}}$, but it need not accommodate large output swings because we intend to have voltage gains through the stages. The second op amp in Biquad_2, on the other hand, can benefit from a relaxed noise requirement but it must offer an output 1-dB compression point of 1.2 V_{pp}.

Nevertheless, we recognize that the op amps must incorporate a two-stage topology so as to provide sufficient gain while driving resistive loads. We hope that the same op amp design can serve the four instances in our LPF. Another benefit of such an approach is that the input and output common-mode (CM) levels of the four op amps are readily compatible.

Let us design an op amp having a gain of several hundred and low noise. Shown in Figure 8 is a differential arrangement where each stage realizes CM feedback by means of resistors. Current source I_1 shifts the output CM level up from 300 mV to about $V_{DD}/2$ so as to maximize the output voltage swing and hence

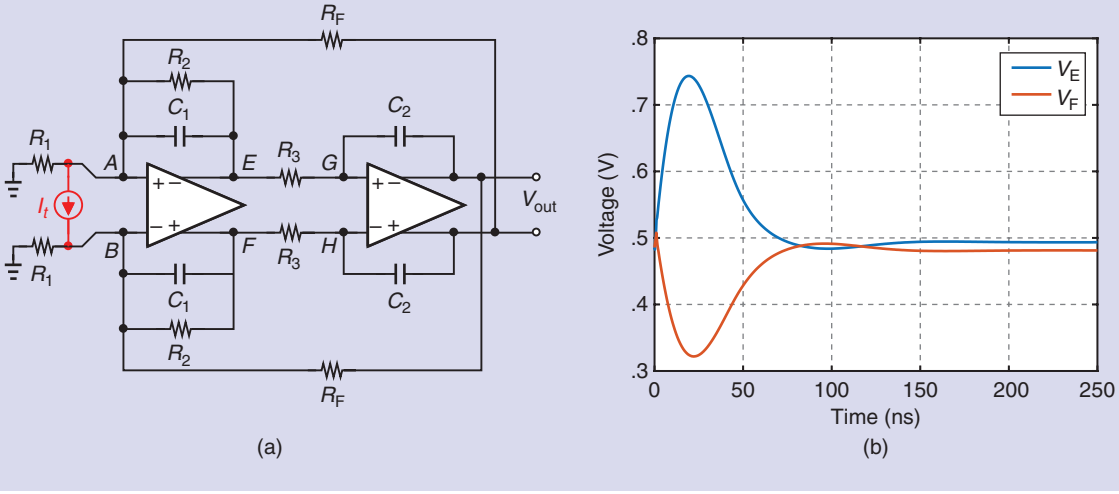

FIGURE 11: (a) Use of a current step to find the in-situ gains of the op amps and (b) resulting waveforms at nodes E and F.

P_{1dB}. The small-signal (unloaded) gain is about 500.

The bias current of the first stage is dictated by our noise target. We choose $I_{SS} = 250\,\mu$A, obtaining the input-referred noise, $\sqrt{\overline{V_n^2}}$, plotted in Figure 9. We observe a value of $5.3\,\text{nV}/\sqrt{\text{Hz}}$ at 1 MHz and $3.3\,\text{nV}/\sqrt{\text{Hz}}$ at 10 MHz, mostly arising from the first stage. But the high flicker noise must also be taken into account. For a downconverted Wi-Fi channel extending to 10 MHz, the signal spectrum contains negligible energy below 10 kHz. We then integrate $\overline{V_n^2}$ from 10 kHz to 10 MHz and divide the result by 10 MHz, arriving at an "average" noise voltage of $4.63\,\text{nV}/\sqrt{\text{Hz}}$. The circuit draws a supply current of 0.5 mA.

The op amp's small-signal single-ended output resistance is 8.5 kΩ. This fairly high value and the two-stage nature of the circuit pose a quandary with respect to the definition of the op amp's BW and our prescription that the BW be about 11 times the desired BW. This issue arises because the derivation in [1] assumes a zero output resistance for the op amp and simply one internal pole. Fortunately, the unity-gain BW of this op amp is high enough that it does not affect the loop phase margin. Interestingly, the op amp does not require frequency compensation.

To quantify the op amp's linearity, we apply a 5-MHz sinusoidal input with a variable amplitude and examine the output swing. Plotted in Figure 10, the results suggest an output 1-dB compression point of about $3\,\text{dBV} \equiv 1.4\,V_{pp}$.

First Biquad Design

We begin the design by assuming that the two biquads in Figure 2 provide similar frequency responses. The BW of two cascaded second-order stages is given by [6]:

$$BW_{tot} = \sqrt[4]{\sqrt{2}-1}\, f_{3dB} \tag{21}$$

$$\approx 0.8\, f_{3dB}. \tag{22}$$

Thus, to obtain a BW_{tot} of, say, 10 MHz, we must ensure $f_{3dB} \approx 12.5$ MHz for each biquad. Opting for $Q = 1$, we select the following values: $R_1 = 500\,\Omega$, $R_2 = R_3 = R_F = 2\,\text{k}\Omega$, and $C_1 = C_2 = 8$ pF. The op-amp design of Figure 8 is used for both instances here. This biquad's voltage gain, R_F/R_1 is nominally equal to 4, suppressing the noise of Biquad$_2$.

The resistors tied to the op amps' outputs lower their equivalent voltage gain. To measure the actual "in-situ" gains, we apply a small current step, I_t, between A and B in Figure 11(a), run a transient simulation, allow the circuit to settle,

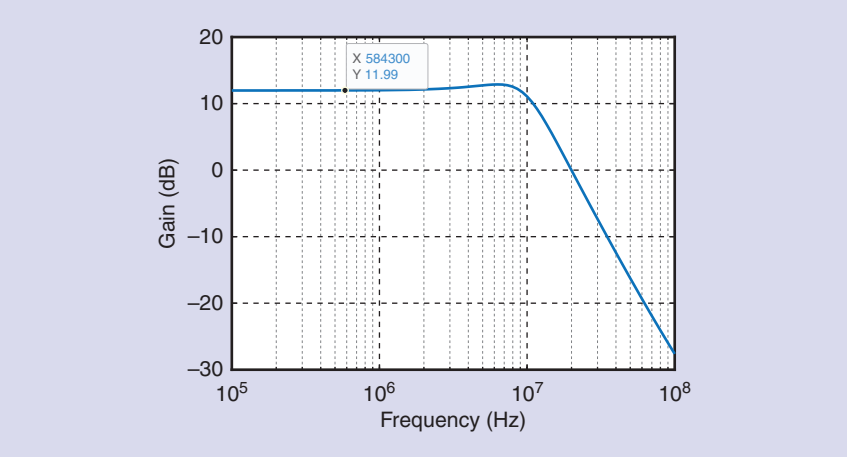

FIGURE 12: Frequency response of the first biquad.

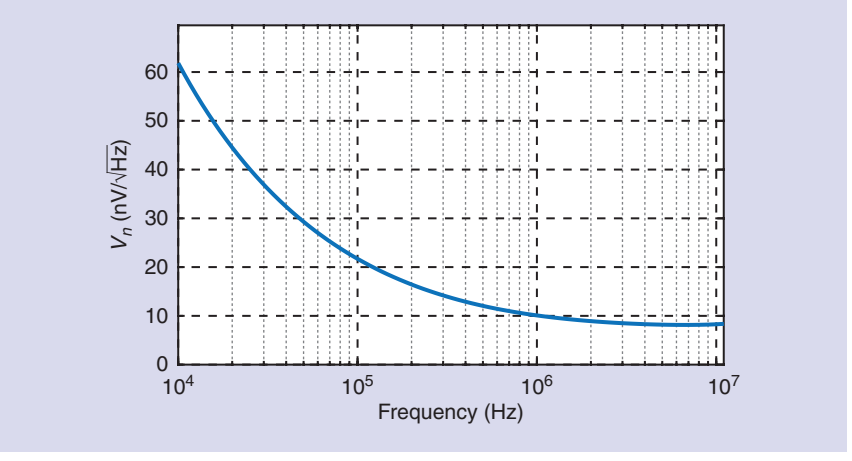

FIGURE 13: The first biquad input-referred noise.

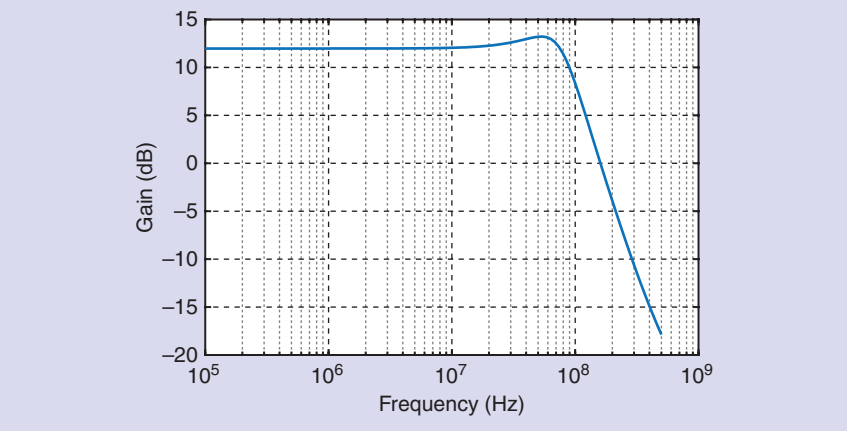

FIGURE 14: The first biquad frequency response for a nominal BW of 80 MHz.

and find $|V_E - V_F|/|V_A - V_B|$ and $|V_{out}|/|V_G - V_H|$. Each amounts to about 100, revealing that the open-loop gains have dropped by a factor of 5 but still suffice for our design.

As an example, Figure 11(b) presents V_E and V_F, also verifying that the circuit is stable.

Plotted in Figure 12 is the ac response of the first biquad, exhibiting a peaking of .87 dB and $f_{3dB} = 11.9$ MHz. As expected, the in-band gain is equal to $R_F/R_1 = 4 \equiv 12$ dB.

The biquad's input-referred noise is presented in Figure 13. It begins at 60 nV/$\sqrt{\text{Hz}}$ at 10 kHz and falls to 8.2 nV/$\sqrt{\text{Hz}}$ at 10 MHz. Integrating $\overline{V_n^2}$ across this range and normalizing to 10 MHz, we obtain an average value of 9.4 nV/$\sqrt{\text{Hz}}$.

In the last step of this design, we reduce the capacitors in Figure 5(b) by a factor of 8 so as to increase f_{3dB} to 100 MHz. Shown in Figure 14, the response displays 1.2 dB of peaking but $f_{3dB} = 96$ MHz. This error results from the finite gain of the op amps and can be removed by simply increasing the capacitor values.

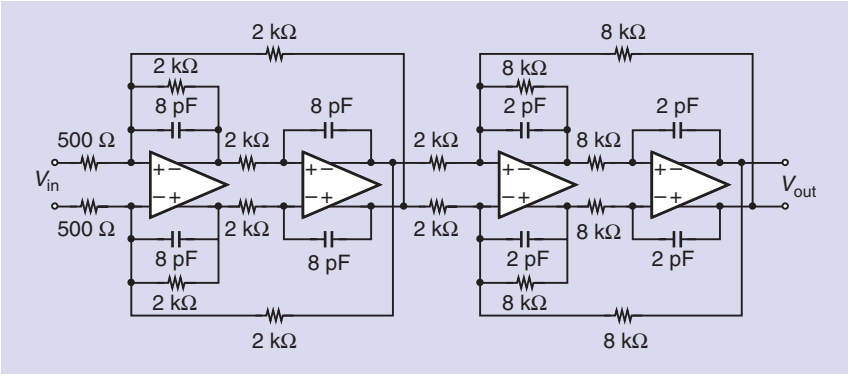

FIGURE 15: The complete filter design.

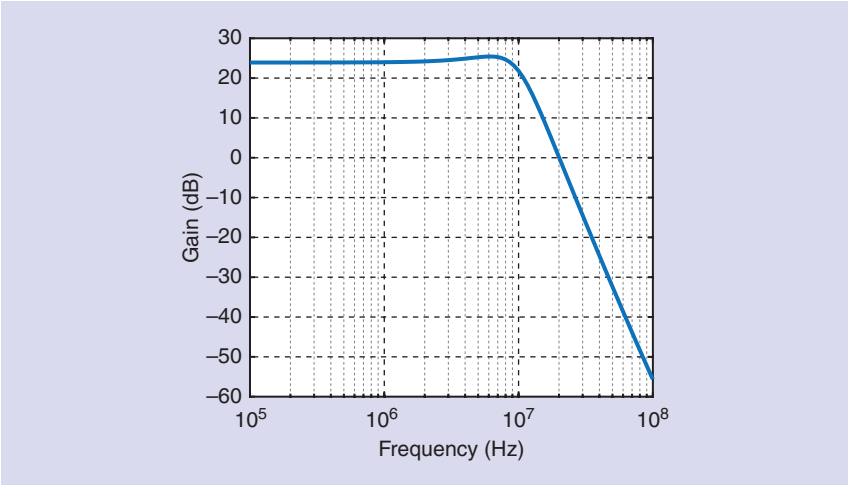

FIGURE 16: The complete filter frequency response.

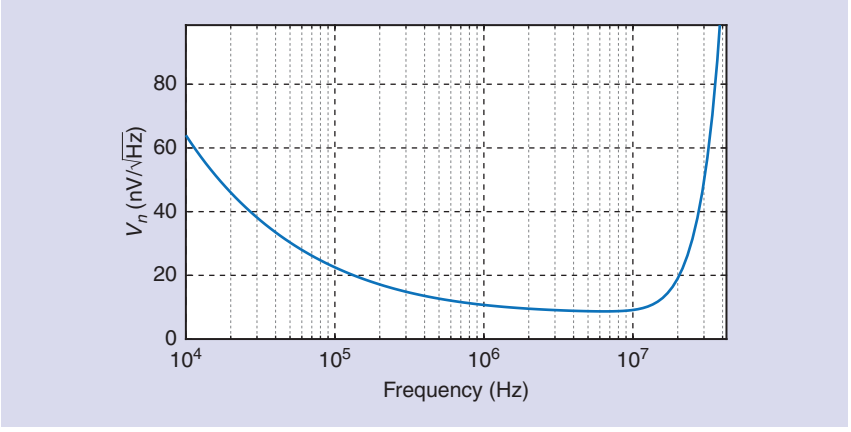

FIGURE 17: The complete filter noise behavior.

Complete Filter Design

According to Figure 2, we must now attach a second biquad to the first. Since the noise of Biquad_2 is less critical, we scale its resistors up by a factor of 4 so as to lighten the load that it presents to Biquad_1. We also scale down its capacitors by the same factor. The design is shown in Figure 15 for $f_{3dB} = 10$ MHz. We use the op amp of Figure 8 for all four instances.

Illustrated in Figure 16 is the circuit's ac response. We observe a peaking of 1.4 dB and $f_{3dB} = 10.4$ MHz. The rejections in the middle of the adjacent and alternate channels are equal to 24 dB and 48 dB, respectively, close to our target values. The TIA in Figure 2 would also provide some rejection.

The input noise is shown in Figure 17, yielding an average value of 10 nV/$\sqrt{\text{Hz}}$. While not relevant to our case, the steep climb beyond 20 MHz is due to the sharp drop of the first biquad's gain.

We now perform the linearity test depicted in Figure 10 for the overall LPF. Figure 18 presents the results and reveals an output P_{1dB} of 5 dBV $5\,\text{dBV} \equiv 1.8\,V_{pp}$.

To accommodate a 160-MHz RF channel, we require $f_{3dB} = 80$ MHz, and hence an eightfold decrease in the capacitor values. As shown in Figure 19, the response yields 2.4 dB of peaking, $f_{3dB} = 88$ MHz, and adjacent- and alternate-channel rejections of 24 dB and 48 dB, respectively. The total power consumption is 2 mW.

The peaking in Figure 19 is somewhat objectionable. We can readily alleviate the issue by introducing

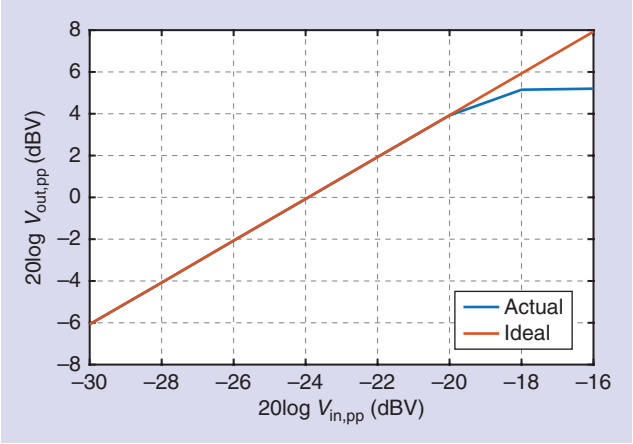

FIGURE 18: The input–output characteristic of the overall filter.

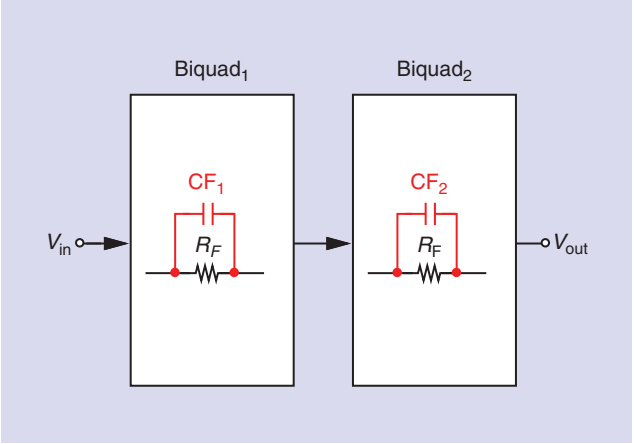

FIGURE 20: Addition of feedforward capacitors to reduce peaking.

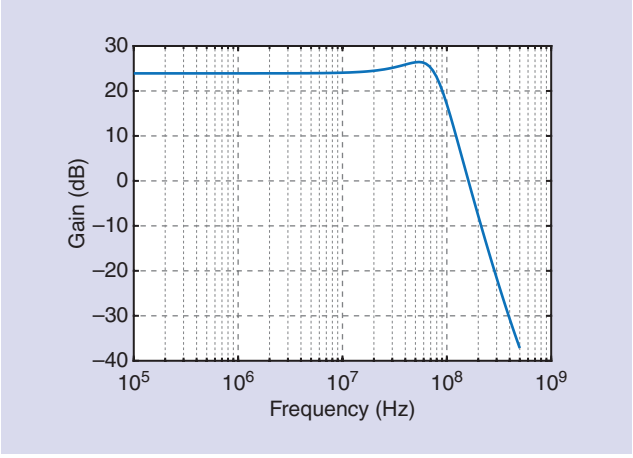

FIGURE 19: The complete filter frequency response for a BW of 80 MHz.

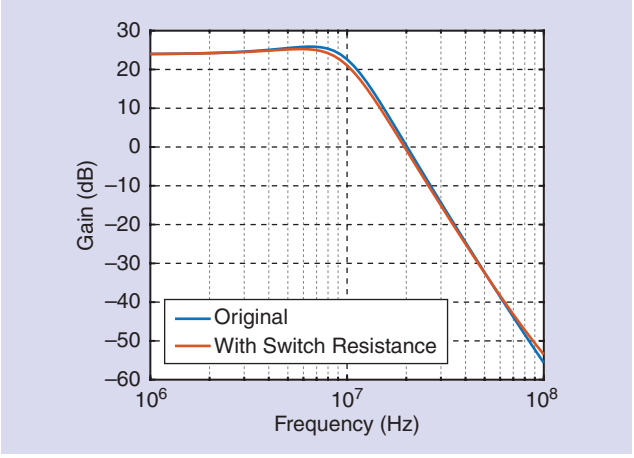

FIGURE 21: Overall response with and without switch resistance.

feedforward capacitors around the biquads (Figure 20). With $C_{F1} = C_{F2} =$ 50 fF, the peaking falls below 1 dB while other performance parameters remain intact.

Capacitor Programmability

To change the capacitor values in Figure 15 for different BWs, we must insert switches in series with both of their terminals. With a CM level around $V_{DD}/2$, the switches must incorporate both NMOS and PMOS devices. But we must ponder the maximum tolerable switch resistance so as to avoid excessively large transistors.

We predict that resistances in series with the capacitors begin to manifest themselves as the capacitor impedances fall at high frequencies. Specifically, in the middle of the alternate-adjacent channel, the filter's rejection suffers if the series resistances become comparable to the capacitor impedances. In Figure 15, the 8-pF capacitors display an impedance of about $-j500\,\Omega$ at 40 MHz, requiring that the total series resistance be much less than $500\,\Omega$. For the second biquad, a fourfold higher resistance is tolerable. Plotted in Figure 21 are the original response and that after we have inserted a resistance of $100\,\Omega$ in series with the 8-pF capacitors and $400\,\Omega$ in series with the 2-pF capacitors. We observe a slight change in the 3-dB BW and negligible degradation of rejection at 40 MHz. The switch widths must therefore be chosen according to these criteria.

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