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The Active Inductor

The active inductor is an inductorless circuit whose impedance rises with frequency across some frequency range. Occupying much less area than a passive inductor and offering tunability, such a circuit proves useful in broadening the bandwidth or realizing other functions that require an inductive element.

As an example of early active inductors, we refer to a 1964 patent by Christensen [1], in which he proposes the circuit shown in Figure 1, where the capacitor at the collector of the transistor drops the gain at high frequencies, weakening the Miller effect of the feedback resistor and hence raising the input impedance. In this article, we study various implementations of active inductors.

Basic Active Inductors

Consider the negative-feedback system shown in Figure 2(a), where the feedback network, K, returns a current to the input. We recognize that feedback lowers the input impedance from Z_1 to

$$Z_{in} = \frac{Z_1}{1 + KH(s)}. \quad (1)$$

Thus, if $H(s)$ falls as the frequency increases, we expect Z_{in} to rise. While appealing, this intuition is not accurate because $H(s)$ takes on a complex value and does not simply fall. Nevertheless, we proceed with this view for now and conclude that a low-pass $H(s)$ or, more generally, a low-pass $KH(s)$ yields an inductive input impedance. Note that the output of $H(s)$ can be a voltage quantity or a current quantity.

Let us implement the topology of Figure 2(a) at the circuit level. As depicted in Figure 2(b), we can realize $H(s)$ simply by a first-order low-pass filter and K by a single MOS device. As explained in the following, proper choice of the element values leads to an inductive Z_{in}.

We should note that the impedance of interest need not appear at the input port of a negative feedback system; the output port is equally qualified. As illustrated in Figure 2(c), if the feedback network senses the output voltage, then the output impedance drops from Z_2 to

$$Z_{out} = \frac{Z_2}{1 + KH(s)} \quad (2)$$

and behaves inductively for a low-pass KH. The signal returned by K to the input can be a voltage or current quantity.

The forward transfer function, $H(s)$, in Figure 2(a) can itself be an active circuit. For example, a low-pass function can be formed by means of a transconductance (G_m) stage and a capacitor. Depicted in Figure 3, the resulting active inductor exhibits certain superior properties compared

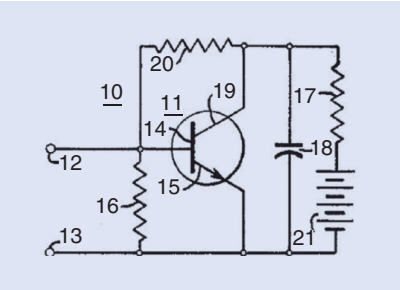

FIGURE 1: The active inductor described by Christensen.

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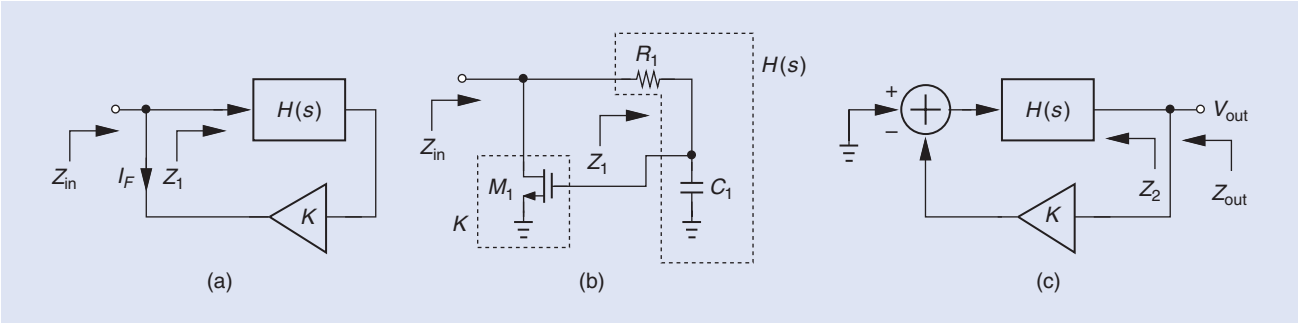

FIGURE 2: A negative-feedback system: its (a) input impedance, (b) circuit implementation, and (c) output impedance.

to that in Figure 2(b). We analyze this topology subsequently, but should remark that $G_{m1}G_{m2}$ must be negative. Also, the loop consisting of G_{m1} and G_{m2} is called a *gyrator*, as it rotates the impedance of C_1 (by 90°), transforming it to inductance.

In the spirit of Christensen's topology, we can construct the circuit shown in Figure 4, where C_1 creates low-pass action at the drain of M_1. We can also view M_1 as a transconductance stage, G_{m1}, and R_1 as a "poor man's" approximation of a feedback transconductance stage, G_{m2}, concluding that the circuit gyrates C_1 to an inductor.

There is yet another perspective for creating active inductance. Let us suppose the feedback in Figure 2(c) is positive and write

$$Z_{out} = \frac{Z_2}{1 - KH(s)}. \tag{3}$$

We surmise that, in this case, a high-pass $KH(s)$ causes Z_{out} to rise with frequency. The high-pass $KH(s)$ also avoids latch-up (which can occur in the presence of positive feedback) by suppressing the loop gain at low frequencies. As illustrated in Figure 5, this topology can be realized by a source follower. Interestingly, here $H(s)$ is not a high-pass function, but K is. Of course, if M_1, R_1, and C_1 are viewed as forming a two-terminal impedance, the two circuits in Figures 2(b) and 5 are equivalent. We reexamine both later in this article.

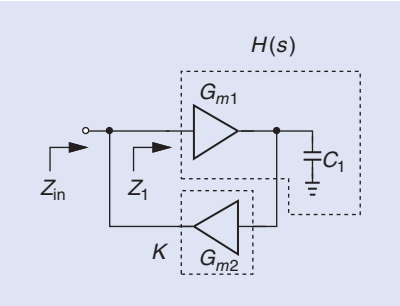

FIGURE 3: An active inductor incorporating a gyrator.

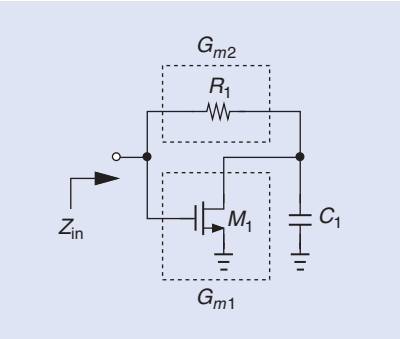

FIGURE 4: An MOS implementation of Christensen's circuit.

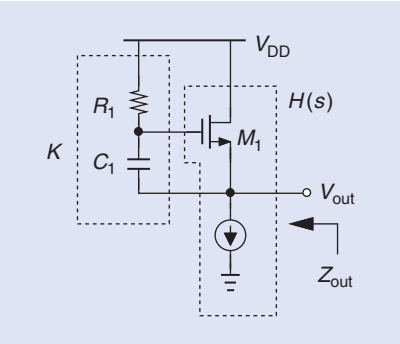

FIGURE 5: A source follower providing an inductive output impedance.

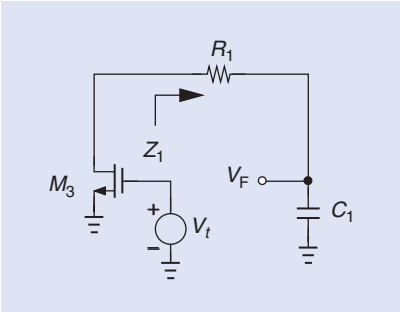

FIGURE 6: The open-loop circuit of an active inductor.

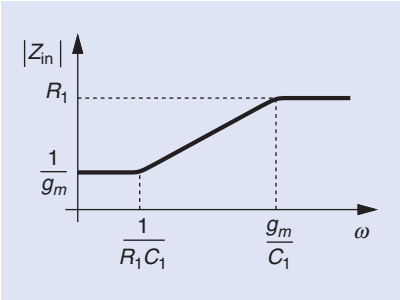

FIGURE 7: The frequency response of an active inductor.

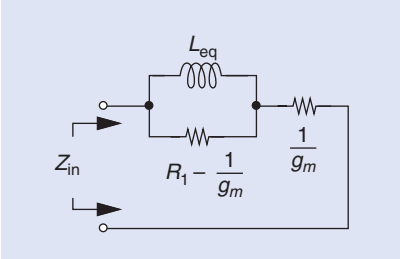

FIGURE 8: The equivalent circuit of an active inductor.

Properties of Active Inductors

As our first step toward quantifying the impedance of active inductors, we return to Figure 2(b) and, from the open-loop circuit shown in Figure 6, write

$$Z_1 = R_1 + \frac{1}{C_1 s}, \tag{4}$$

where channel-length modulation is neglected. Also, since the small-signal drain current of M_1 entirely flows through C_1, the loop gain (loop transmission) is given by

$$KH(s) = -\frac{V_F}{V_t} \tag{5}$$

$$= \frac{g_m}{C_1 s}. \tag{6}$$

It follows from (1) that the closed-loop input impedance is equal to

$$Z_{in} = \frac{\frac{R_1 C_1 s + 1}{C_1 s}}{1 + \frac{g_m}{C_1 s}} \tag{7}$$

$$= \frac{R_1 C_1 s + 1}{C_1 s + g_m}. \tag{8}$$

This result agrees with our intuition in Figure 2(b). At low frequencies, C_1 acts as an open circuit and M_1 as a diode-connected device, yielding $Z_{in} \approx 1/g_m$. At high frequencies, the gate of M_1 is at ac ground, and $Z_{in} \approx R_1$. Sketched in Figure 7, $|Z_{in}|$ rises with frequency if $1/g_m < R_1$, i.e., if the zero of Z_{in}, ω_z, has a lower magnitude than its pole, ω_p. The circuit thus behaves inductively between ω_z and ω_p.

We wish to formulate the equivalent inductance of this topology. As an approximation, we can find the slope of $|Z_{in}|$ in Figure 7 between ω_z and ω_p. But an exact expression is also possible. Since Z_{in} reduces to $1/g_m$ at low frequencies and to R_1 at high frequencies, we envision the arrangement shown in Figure 8. Let us first subtract the series element, $1/g_m$, from Z_{in}:

$$Z_{in} - \frac{1}{g_m} = \frac{\left(R_1 - \frac{1}{g_m}\right) C_1 s}{C_1 s + g_m}. \quad (9)$$

Inverting this impedance and decomposing the result into a sum,

$$\left(Z_{in} - \frac{1}{g_m}\right)^{-1} = \frac{1}{\left(R_1 - \frac{1}{g_m}\right)\frac{C_1}{g_m} s} + \frac{1}{R_1 - \frac{1}{g_m}}, \quad (10)$$

we identify two elements in parallel. The first term on the right represents the admittance of an inductor having a value of

$$L_{eq} = \left(R_1 - \frac{1}{g_m}\right)\frac{C_1}{g_m}, \quad (11)$$

and the second term corresponds to the inverse of a resistance equal to $R_1 - 1/g_m$, both of which confirm the topology predicted in Figure 8. As expected, we must have $R_1 > 1/g_m$ to obtain an inductance. In practice, we choose $R_1 \gg 1/g_m$, obtaining

$$L_{eq} = \frac{R_1 C_1}{g_m}. \quad (12)$$

The circuits of Figures 4 and 5 follow these results as well. We can thus select R_1, C_1, and g_m to obtain a desired inductance, and we can make them programmable so as to tune L_{eq}.

The two resistive components in Figure 8 imply a finite quality factor (Q) for the active inductor. Returning to Z_{in} in (8), we can define the Q as the desirable (imaginary) part of Z_{in} divided by the undesirable (real) part. It follows that

$$Q = \frac{\mathrm{Im}\{Z_{in}\}}{\mathrm{Re}\{Z_{in}\}} \quad (13)$$

$$= \frac{(g_m R_1 - 1) C_1 \omega}{g_m + R_1 C_1^2 \omega^2}. \quad (14)$$

If $R_1 \gg 1/g_m$,

$$Q = \frac{\frac{g_m}{C_1 \omega} R_1 C_1 \omega}{\frac{g_m}{C_1 \omega} + R_1 C_1 \omega} \quad (15)$$

$$= \left(\frac{g_m}{C_1 \omega}\right) \| (R_1 C_1 \omega). \quad (16)$$

We note that the first term on the right corresponds to the Q of L_{eq} if only the parallel resistance, $R_1 - 1/g_m \approx R_1$, is considered, and the second term represents the Q only if the series resistance, $1/g_m$, is taken into account. The maximum Q occurs if $g_m/(C_1\omega) = R_1 C_1 \omega$ and is equal to $g_m/(2C_1\omega)$. However, the Q is also limited by the output resistance of M_1.

For the gyrator-based circuit of Figure 3, one can readily show that

$$Z_{in} = -\frac{C_1}{G_{m1} G_{m2}} s. \quad (17)$$

(Recall that $G_{m1} G_{m2}$ must be negative.) The equivalent inductance is therefore equal to $-C_1/(G_{m1} G_{m2})$ and can be set to relatively large values (e.g., in the microhenry range) by selecting a small $G_{m1} G_{m2}$ product. Since the G_m blocks can incorporate multiple stages, this structure can achieve higher inductance values than that in Figure 2(b).

In contrast to the topology of Figure 2(b), the gyrator-based inductor appears to exhibit an infinite Q as (17) does not contain a real part. But the output resistances of G_{m1} and G_{m2} must be considered. Referring to Figure 9, we write I_F as

$$I_F = -G_{m1} \frac{r_{O1}}{r_{O1} C_1 s + 1} G_{m2} V_X, \quad (18)$$

and hence

$$\frac{V_X}{I_F} = \frac{-C_1}{G_{m1} G_{m2}} s - \frac{1}{G_{m1} G_{m2} r_{O1}}. \quad (19)$$

The equivalent inductor thus suffers from both a series resistance equal to $-1/(G_{m1} G_{m2} r_{O1})$ and a parallel resistance equal to r_{O2}.

Applications and Design Issues

Active inductors have found a multitude of applications in circuit design. In this section, we study a few and describe their tradeoffs.

In a manner similar to their passive counterparts, active inductors can create shunt peaking, thus widening the bandwidth of amplifiers. Illustrated in Figure 10(a) is an example [2] where M_1 along with R_1 and the gate-source capacitance, $C_{GS} = C_1$, acts as an inductance in series with R_D. This branch exhibits a higher impedance as the frequency increases, partially counteracting the effect of C_L.

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The speed improvement afforded by M_1 is limited by its gate-drain and source-bulk capacitances. We can quantify the effect of the former by redrawing the active inductor as in Figure 10(b), where C_2 denotes the gate-drain capacitance. Opening the feedback loop, noting that the loop gain is still equal to $g_m/(C_1 s)$, and finding the overall impedance, we have

$$Z_{in} = \frac{R_1 (C_1 + C_2) s + 1}{C_1 s + g_m} \cdot \frac{1}{R_1 C_2 s + 1}. \quad (20)$$

Compared to (8), this impedance exhibits a lower zero frequency and

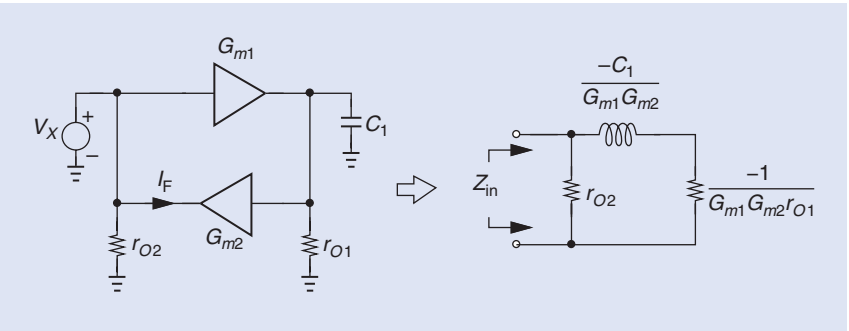

FIGURE 9: A gyrator circuit with finite output impedances.

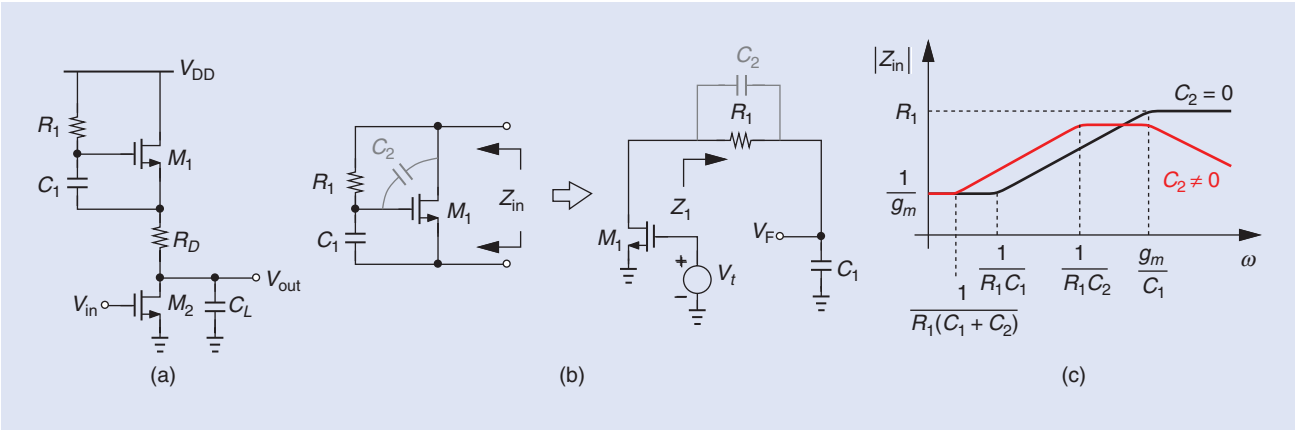

FIGURE 10: Shunt peaking by means of active inductors: (a) a common-source amplifier employing an active inductor, (b) the effect of $C_{GD} = C_2$, and (c) the resulting frequency response.

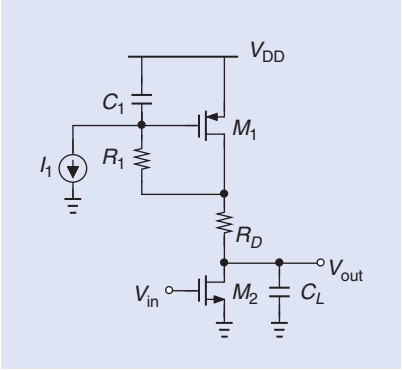

FIGURE 11: A peaking stage using a PMOS device as an active inductor.

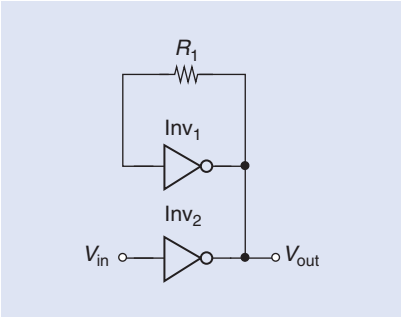

FIGURE 12: Inverter-based amplification employing an active inductor.

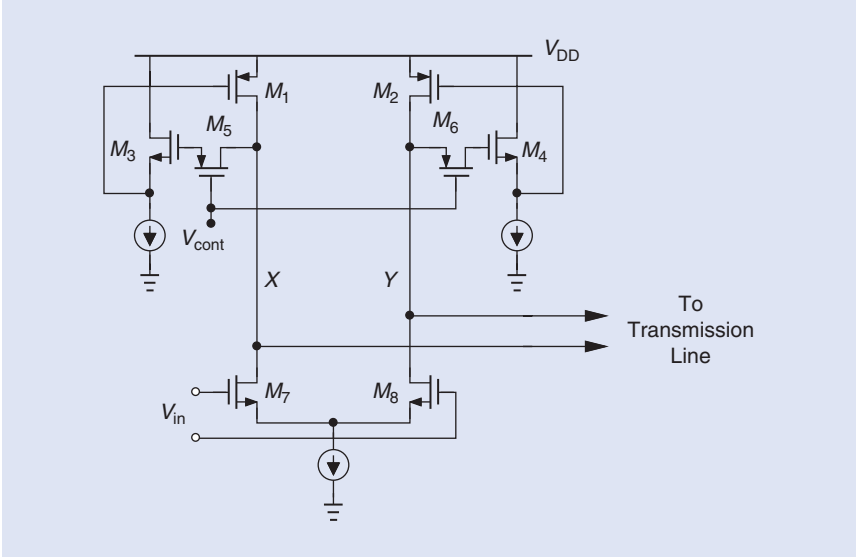

FIGURE 13: An output current-mode driver using active inductors.

an additional pole arising from C_2. Figure 10(c) sketches $|Z_{in}|$, revealing that C_2 reduces the inductive frequency range and also yields a capacitive behavior beyond $\omega = g_m/C_1$.

Another drawback of the active inductor shown in Figure 10(a) relates to its voltage headroom consumption, in the amount of V_{GS1}. This issue limits the utility of the circuit in low-voltage design. It is possible to alleviate the problem by changing M_1 to a PMOS transistor, as depicted in Figure 11, and drawing a constant current from R_1. Selecting $I_1 R_1 \approx |V_{TH1}|$, we can place M_1 at the edge of the triode region, thereby reducing its headroom consumption from $|V_{GS1}|$ to $|V_{DS1}|$. Alternatively, a source follower can be inserted in the loop around M_1, as described subsequently.

The diode-connected nature of M_1 in Figure 10(a) produces inverse nonlinearity and partially cancels the nonlinearity of M_2 while creating inductive peaking as well. This idea can also be applied to CMOS inverters targeting moderate amounts of linearity. Depicted in Figure 12 [3], such a structure employs Inv_1 and R_1 to provide an active inductor and an inverse load for the main inverter, Inv_2. Thus, the bandwidth at the output node is broadened, and V_{out} is a more linear function of V_{in} than in a simple inverter. Of course, the poor supply rejection of the inverters dictates careful supply regulation.

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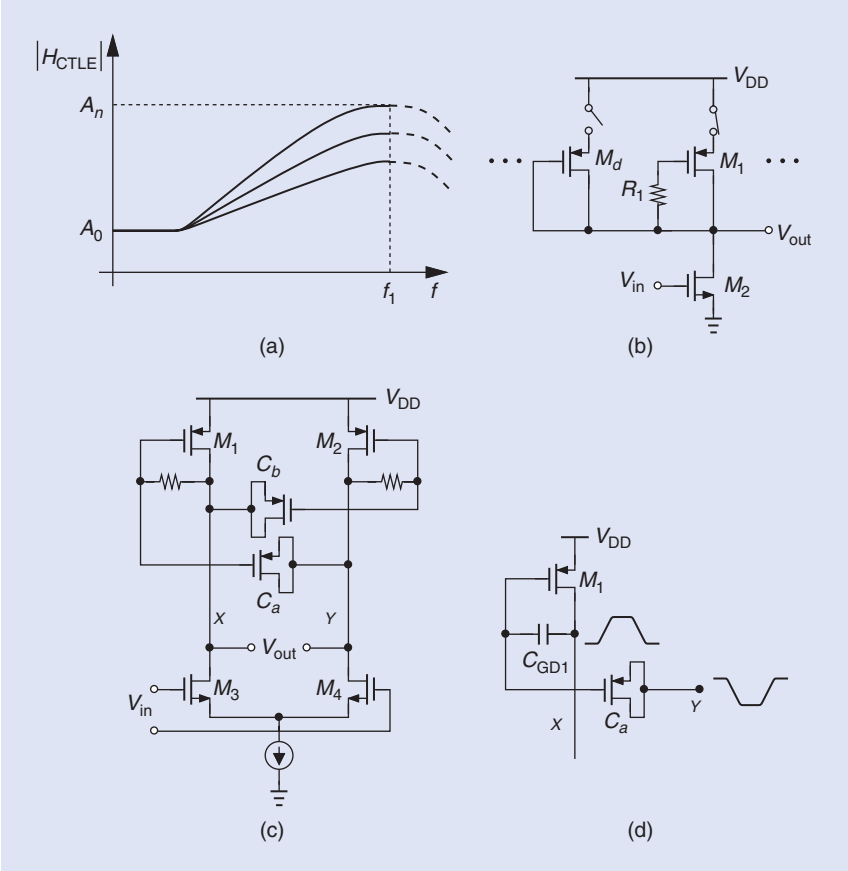

FIGURE 14: CTLE application of active inductors: (a) the typical CTLE frequency response, (b) the CTLE implementation using active inductors, (c) cancellation of gate-drain capacitance in a differential topology, and (d) an illustration of the capacitors' role.

example [4] where a differential pair delivers a large voltage swing to a transmission line and the network comprising M_1-M_6 serves as a tunable inductive load. We recognize that M_1 and M_2 play the same role as M_1 in Figure 11 and M_5 and M_6 the same role as R_1. Moreover, source followers M_3 and M_4 act as level shifters, allowing the gate voltages of M_1 and M_2 to be lower than their respective drain voltages by $V_{GS3,4}$. This structure therefore lends itself to low supply voltages. The on-resistance of M_5 and M_6 can be adjusted by means of their gate voltage, thus providing a variable boost factor [4].

Another interesting application of active inductors is in continuous-time linear equalizers (CTLEs) used in wireline receivers. A CTLE must provide a high-pass response to partially compensate for the high-frequency loss of the channel through which the data travels [Figure 14(a)]. We say the CTLE provides a "boost factor," A_n/A_0, and we make it programmable so as to accommodate different channel losses.

We can envision the CTLE as a simple common-source stage and implement the responses in Figure 14(a) by means of a variable load impedance; specifically, since the slope of the load must be programmable, we surmise that a variable inductance can serve this purpose. The tunability afforded by (12) thus proves useful here, leading to the CTLE topology shown in Figure 14(b) [5]. The inductance is tuned by varying the PMOS load's transconductance. This device is decomposed into a number of units, each of which can participate in the active inductor environment. But, to ensure a constant low-frequency gain, A_0, when some of these units turn off, additional diode-connected transistors are turned on [5]. This approach must still deal with the voltage headroom consumed by the PMOS transistors.

Recall from Figure 10(c) that the gate-drain capacitance of the core transistor in an active inductor degrades the performance. This issue can be resolved in a differential topology by adding compensating capacitors [Figure 14(c)] [5]. Here, C_a and C_b are chosen equal to the PMOS gate-drain capacitances. As illustrated in Figure 14(d), the gate voltage of M_1 is now unaffected by C_{GD1} because this capacitance and C_a inject equal and opposite amounts of charge.

Active inductors can also serve in analog filter design. In fact, some classic filters were based on "simulated inductors" [6], circuits that used op-amps and capacitors to emulate an inductive behavior.

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