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The Design of a Millimeter-Wave VCO

Millimeter-wave transceivers have found their place in 5G radios operating around 30 GHz. In this article, we design a voltage-controlled oscillator (VCO) in 28-nm CMOS technology for such an environment. We target the following performance

- tuning range: 28–32 GHz
- phase noise (PN): –100 dBc/Hz at 1-MHz offset
- power consumption: less than 2 mW.

The circuit is simulated in the slow–slow corner of the process with V_{DD} = 0.95 V and at $T = 75°C$. Given the high oscillation frequency and the low PN, we opt for an inductance–capacitance (*LC*) topology. The reader is referred to numerous articles on *LC* oscillator design for background information, e.g., [1]–[5].

The design of the VCO depends to some extent on the phase-locked loop (PLL) in which it is embedded. We assume that the PLL receives a reference frequency of 200 MHz with a PN of –170 dBc/Hz. The PLL therefore employs a feedback divide ratio equal to 300.

General Considerations

We begin with the simple *LC* oscillator shown in Figure 1, where R_p models the loss of each tank. It can be shown that the peak-to-peak voltage swing at X (or Y) is given by $(4/\pi)R_pI_{SS}$ [5]. The outputs bear a common-mode (CM) level close to V_{DD}, possibly requiring capacitive coupling for driving stages such as mixers and frequency dividers. The tail current source is necessary to maintain the proper bias conditions and voltage swings in the presence of process, supply voltage, and temperature (PVT) variations.

The output PN of this structure due to the thermal noise of M_1, M_2, and the tanks is expressed as

$$S_{\phi n}(\Delta f) = \frac{\pi^2 kT(\gamma+1)}{2R_pI_{SS}^2}\left(\frac{f_0}{2Q\Delta f}\right)^2, \quad (1)$$

where $k = 1.38\times10^{-23}$ J·K, γ is the MOS excess noise coefficient (and approximately equal to one), f_0 is the oscillation frequency, Q is the tank quality factor, and Δf is the offset frequency [5]. Since $V_0 = (4/\pi)I_{SS}R_p$, we rewrite (1) as

$$S_{\phi n}(\Delta f) = \frac{2\pi kT(\gamma+1)}{I_{SS}V_0}\left(\frac{f_0}{2Q\Delta f}\right)^2. \quad (2)$$

If we select $V_0 \approx 0.8V_{pp}$, we have only I_{SS} and Q under our control. What combination of these two parameters yields $S_{\phi n}(\Delta f = 1\text{MHz}) = -100\,\text{dBc/Hz}$ at T = 350 K? For example, a power budget of 2 mW and $I_{SS} \approx 2$ mA requires $Q \approx 9$, a reasonable value. We bear in mind these theoretical predictions and proceed.

Inductor Design

The tank quality factor, the output swing, and the PN of the foregoing oscillator strongly depend on the inductor's design. We then ponder how this device must be realized. Numerous geometries can be envisioned, but we focus on a single-turn octagonal structure. Shown in Figure 2(a), this shape provides two degrees of freedom, namely, the diameter, d, and the linewidth, W. The former defines the inductance, and the latter affects the loss. At millimeter-wave frequencies, the current tends to flow near the edges of the octagon, but W still plays some role in the Q. In this spirit, we also consider a parallel stack of metal-9 (M9) and metal-8 (M8) lines [Figure 2(b)] and ask whether it can offer a greater Q.

The two geometries in Figure 2 have been simulated in Cadence's EMX tool for various inductance values and with different dimensions. Table 1 summarizes the results, suggesting that the Q reaches a maximum of 32 for a 106-pH M9/M8 stack having a diameter of 110 μm and a linewidth of 20 μm. The Q does rise by 10% as a result of stacking. We should remark that these values correspond to the differential excitation of the inductors.

Whether or not the 106-pH device satisfies our needs is also determined

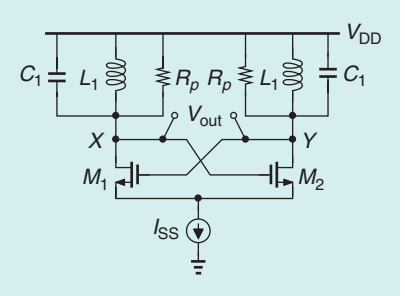

FIGURE 1: A basic *LC* oscillator.

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by the equivalent parallel resistance, R_p, that it provides. Specifically, with an I_{SS} bound of about 2 mA in Figure 1, the output swing, $(4/\pi)R_pI_{SS}$, must be reasonable. Fortunately, a differential inductance of L = 106 pH yields $R_p = (L/2)\omega Q = 320\,\Omega$ at 30 GHz, and hence, a single-ended swing of about 815 mV_{pp}. We then proceed with this geometry.

Using (1) and this inductor design, we can predict the PN. If $I_{SS} = 2$ mA and $R_p = 320\,\Omega$, we have $S_{\phi n}(\Delta f) = -112$ dBc/Hz at 1-MHz offset. We are eager to see whether simulations agree with this result.

Basic Oscillator Design

With the optimal inductor found, we construct the basic oscillator shown in Figure 3(a). Here, we select $(W/L)_{1,2}$ such that M_1 and M_2 steer their tail current completely and rapidly while sensing sinusoids at X and Y having a peak-to-peak swing of about 800 mV. For now, each tank includes a constant capacitance of 500 fF so as to provide $f_0 \approx 30$ GHz.

Plotted in Figure 3(b) are the output waveforms. The swing is about 10% less than the target because

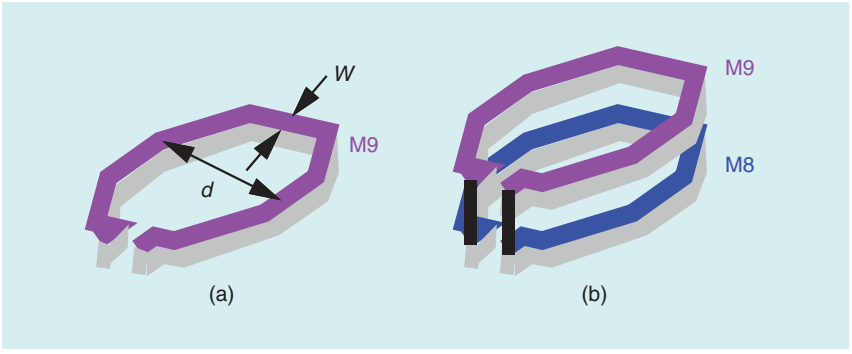

FIGURE 2: Octagonal inductors realized as (a) a single metal-9 layer and (b) parallel stack of metal-9 and metal-8 (M8) layers.

TABLE 1. A COMPARISON OF DIFFERENT INDUCTOR DESIGNS.

***d* (μm)**	82	110	118	136
***W* (μm)**	20	20	15	13
***L* (pH)**	57	106	158	203
***Q* at 30 GHz**				
M9 Only	22	29	28	28
M9/M8	25	32	30	30

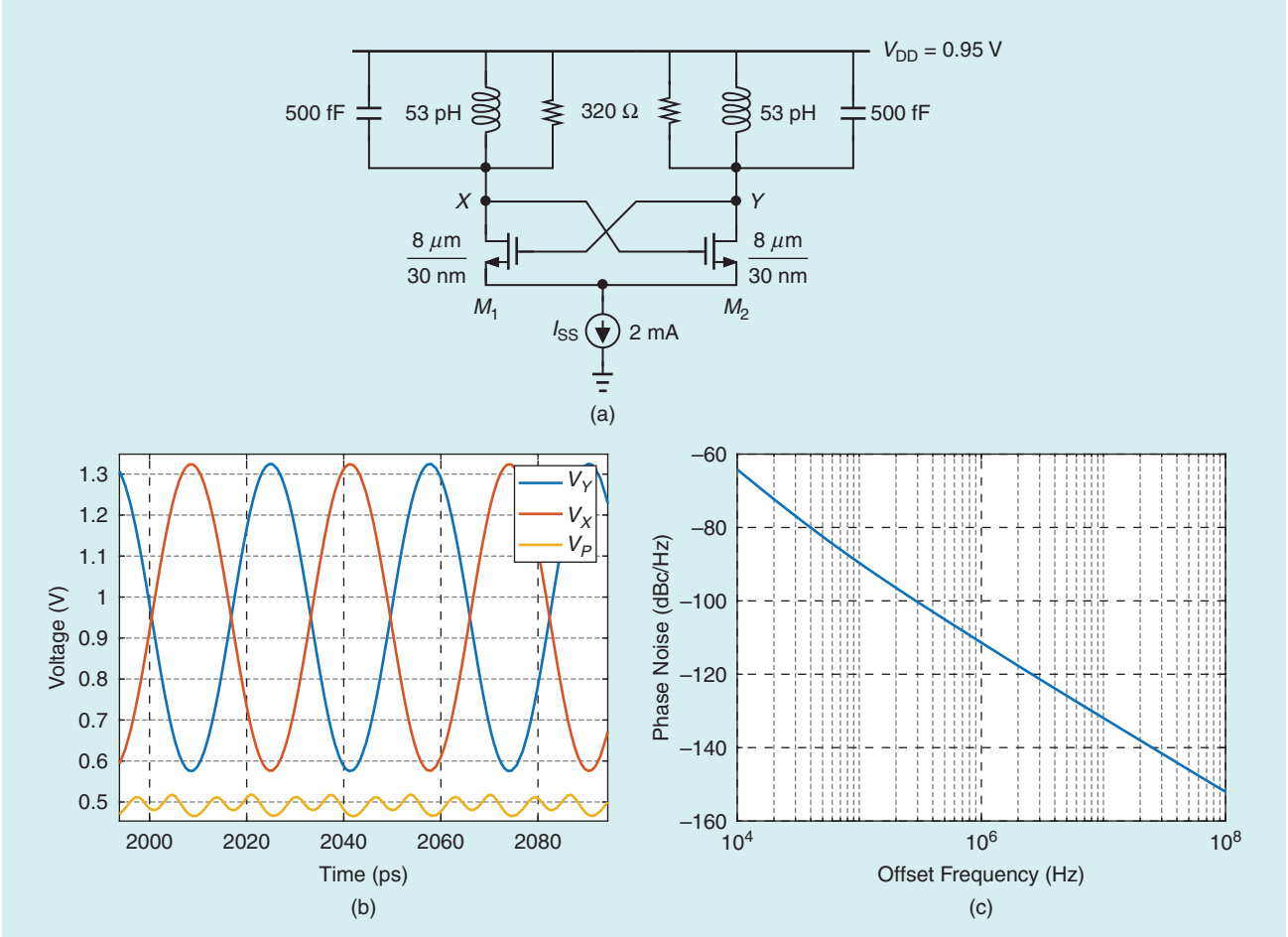

FIGURE 3: (a) The preliminary oscillator design, (b) its waveforms, and (c) its PN profile.

the expression $(4/\pi)R_p I_{SS}$ assumes that the drain currents are perfect square waves, but in reality, they suffer from gradual transitions.

The oscillator's PN is shown in Figure 3(c), offering two interesting insights. First, the profile displays a slope of about –30 dBc/decade from $\Delta f = 10\,\text{kHz}$ to $\Delta f = 100\,\text{kHz}$, suggesting flicker noise upconversion. Second, the PN at $\Delta f = 1$ MHz is about –111 dBc/Hz, while (1) implies a value of –114 dBc/Hz at $T = 350$ K and with $Q = 32$. This discrepancy arises primarily because M_1 and M_2 enter the triode region in this design—as evidenced by a maximum $V_X - V_Y$ of 750 mV—whereas (1) assumes they do not.

The basic oscillator must now be modified for continuous and discrete tuning. The former is created by varactors, and the latter is realized by switched capacitors.

Continuous Tuning

We wish to add MOS varactors to the output nodes so as to provide continuous tuning (Figure 4). We must select the dimensions of M_{v1} and M_{v2}. The minimum length is typically dictated by the design kit's rules at a value much greater than the process node's minimum channel length. This is possibly because the foundry has not measured and characterized short-channel varactors. Here, we choose the minimum allowable length of 200 nm, expecting that the long channel introduces a high equivalent series resistance, degrading the varactor Q. Indeed, the Q is around 20 at 30 GHz.

This limitation may suggest that the tank Q drops considerably when the varactors are attached. Fortunately, M_{v1} and M_{v2} need provide but a narrow tuning range and can therefore be small. It is shown [6] that the overall tank Q is obtained from

$$\frac{1}{Q_{\text{tot}}} = \frac{1}{Q_L} + \frac{1}{\left(1 + \frac{C_1}{C_{\text{var}}}\right) Q_{\text{var}}}, \qquad (3)$$

where Q_L and Q_{var} denote the inductor and varactor quality factors, respectively; C_1 is the constant tank capacitance; and C_{var} is the varactor capacitance. For example, if $Q_L = 32$, $Q_{\text{var}} = 20$, and $C_1/C_{\text{var}} = 20$, then the varactor lowers the tank Q by about 9%. This point calls for a small C_{var} and, thus, a low VCO gain, K_{VCO}. Nonetheless, an excessively narrow continuous tuning range means that the circuit cannot accommodate large temperature drifts unless the discrete-tuning network switches capacitors into or out of the tanks. Such an action disrupts the operation of the phase-locked loop and should be preferably avoided.

As a compromise, we choose a width of 16 μm for M_{v1} and M_{v2} in Figure 4, obtaining $f_0 = 28.8$ GHz for $V_{\text{cont}} = 100$ mV and $f_0 = 29.7$ GHz for $V_{\text{cont}} = 850$ mV. (The control voltage is allowed to reach within 100 mV of the supply rails in view of the preceding circuit's output voltage compliance.) The 900-MHz range accrues at the cost of a high K_{VCO}, nearly 1.9 GHz/V in the vicinity of $V_{\text{cont}} = 850$ mV. This effect makes the circuit sensitive to noise on V_{cont} and on V_{DD}. For example, suppose a sinusoidal ripple appears on V_{cont} at the PLL reference frequency of 200 MHz. For such a ripple to yield an output spur at –60 dBc, we have $K_{\text{VCO}} V_m/(2\omega_m) = 10^{-3}$, where V_m and ω_m denote the ripple amplitude and frequency, respectively. It follows that $V_m < 0.21$ mV, a difficult condition to guarantee.

We can also estimate the maximum tolerable supply noise for $K_{\text{VCO}} = 1.9$ GHz/V. As explained in [7], a noise spectral density of $\overline{V_n^2}$ at a frequency f_1 yields $S_\phi(f_1) = K_{\text{VCO}}^2 \overline{V_n^2}/(4\pi^2 f_1^2)$. For this value to remain negligible with respect to our target of –100 dBc/Hz at 1-MHz offset, we select $S_\phi(f_1) = -110\,\text{dBc/Hz}$, obtaining $\sqrt{\overline{V_n^2}} = 4.4\ \text{nV}/\sqrt{\text{Hz}}$, also a daunting challenge in supply voltage regulator design.

Another issue arising from a high K_{VCO} relates to the conversion of amplitude modulation (AM) to phase modulation (PM). As explained later, this occurs when the tail current source's noise modulates the output amplitude, and the varactor nonlinearity converts this AM to PM.

For these reasons, we halve the varactor width and observe a tuning range of 500 MHz and a maximum K_{VCO} of 980 MHz/V. In practice, these choices are refined in conjunction with the PLL design.

According to simulations, the 8-μm -wide varactors negligibly affect the PN. Unfortunately, this will not be true when the ideal tail current source is replaced with an actual implementation, as seen later.

Discrete Tuning

In addition to the 500-MHz continuous tuning range produced previously, we wish to cover a total of about 4 GHz by means of switched capacitors. We envision the characteristics shown in Figure 5(a), where adjacent curves must have some overlap, f_{ov}, so as to avoid "dead zones." This family of curves presents its own challenges.

Suppose we allow $f_{\text{ov}} = 100$ MHz. Then, the VCO demands about 10 tuning curves, i.e., 20 switched capacitors must be tied to nodes X and Y in Figures 4(a) and Figure 5(b). The inductor's legs are extended to accommodate the switching units, thereby introducing additional resistance, while their inductances approximately cancel. The Q thus drops. Given that the total length of the original 106-pH inductor is about 350 μm, we must maintain l_1 below about 10 μm. The 10 units on each side must therefore be designed with a pitch of no more than 1 μm, an impossible task in 28-nm technology.

The next challenge stems from the finite Q of the switched capacitors. Consider the simple branch shown in Figure 6(a), where the digital input, D_j, switches the unit

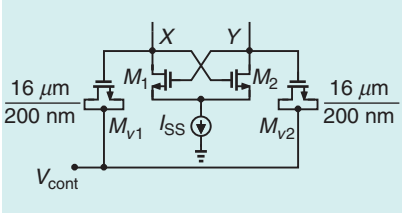

FIGURE 4: The addition of varactors to oscillator core.

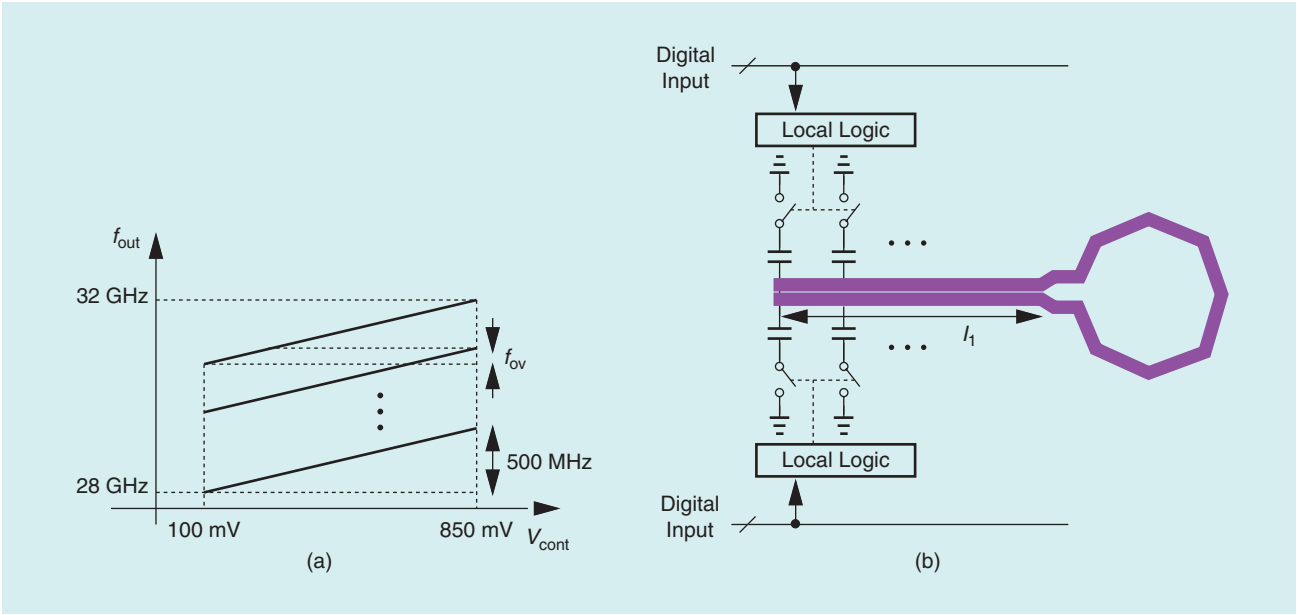

FIGURE 5: (a) The desired continuous and discrete tuning characteristics and (b) the resulting layout complexity.

capacitor, C_u, into or out of the tank at node X. If conducting, S_1 displays an on-resistance, R_u, limiting the Q of this branch to $1/(R_u C_u \omega_0)$. If off, S_1 still presents $C_p = C_{GD} + C_{DB}$ in series with C_u. That is, the "on/off capacitance ratio" is given by $1 + C_u/(C_{GD} + C_{DB})$. As the width of S_1 increases, so does the Q, but this ratio drops. The reader can see that this less-than-infinity ratio reduces the vertical spacing between the successive curves in Figure 5(a) or, equivalently, raises the overlap, f_{ov}. In other words, 10 curves may not suffice to cover a range of 4 GHz.

With the foregoing thoughts, we ask whether it is possible for the switched-capacitor branches to achieve a Q comparable to that of the inductor. This is an important issue because, unlike the varactors, these capacitors must constitute about 25% of the tank capacitance, potentially degrading the overall Q considerably.

With L = 53 pH, the tank capacitance should vary from 610 fF to 470 fF to yield the desired frequency range. The total switched capacitance then amounts to 140 fF. We begin with the arrangement shown in Figure 7(a), where all of the switched branches are lumped into one. We select, as an example, a W/L ratio of 10 μm/30 μm for S_1 and use ac simulations to find the Q of the structure. Defining Q as $1/(R_{on} C_a \omega) = \mathrm{Im}\{Z_a\}/\mathrm{Re}\{Z_a\}$, we obtain $Q \approx 1$ at 30 GHz! This means that $R_{on} \approx 1/(C\omega) \approx 44\,\Omega$. Thus, to approach the inductor Q of 32, the width of the switch must increase to $10\,\mu\mathrm{m} \times 32 = 320\,\mu\mathrm{m}$. Note that with such a high Q, we have from Figure 7(b)

$$\left|\frac{V_N}{V_X}\right| = \left|\frac{R_{on} C_a s}{R_{on}(C_a + C_p)s + 1}\right| \quad (4)$$

$$\approx \frac{1}{Q}. \quad (5)$$

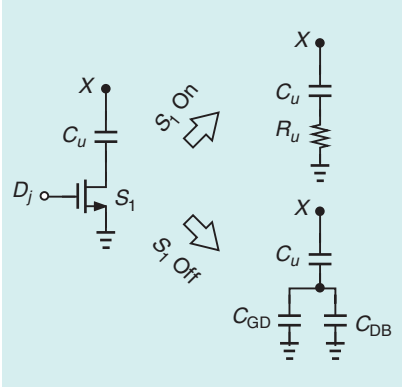

FIGURE 6: A switched-capacitor branch in on and off conditions.

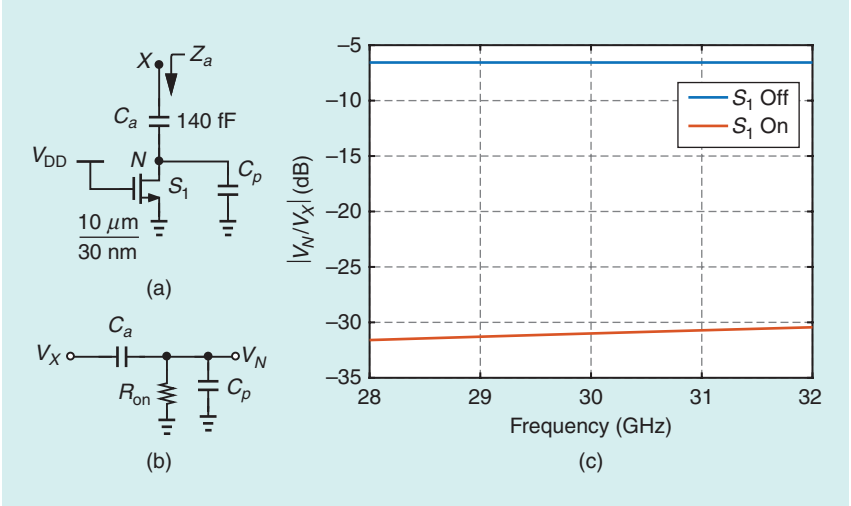

FIGURE 7: (a) A lumped representation of the entire discrete tuning network, (b) the simplified model, and (c) the magnitude response for the on and off states.

We can then simply measure the Q from the plot of $|V_N/V_X|$ [Figure 7(c)]. When the switch is off,

$$\left|\frac{V_N}{V_X}\right| = \frac{C_a}{C_a + C_p}, \tag{6}$$

which is also plotted in Figure 7(c). The 6-dB attenuation reveals that $C_p \approx C_a$, and hence, the on/off ratio is $C_a/(0.5C_a) = 2$.

In summary, it is possible to raise the Q of the tank's switched capacitance to that of the inductor. Applying (3) to this case, we write the second denominator on the right as $(1 + 610\,\text{fF}/140\,\text{fF}) \times 32 \approx 170$, obtaining $Q_{tot} = 27$. The PN then degrades by $20 \log 32/27 = 1.5$ dB. More importantly, the low on/off ratio limits the tuning range; with the 140-fF capacitor switched out, the tank still contains $470\,\text{fF} + 140\,\text{fF}/2 = 540\,\text{fF}$. That is, the frequency rises by only $\sqrt{610\,\text{fF}/540\,\text{fF}} = 6.3\% \approx 1.89$ GHz rather than by 4 GHz. It is important to note that these issues are far less severe in designs operating at, e.g., 5 GHz, because the width of the bottom-plate switches can be proportionally smaller at these frequencies for the same Q.

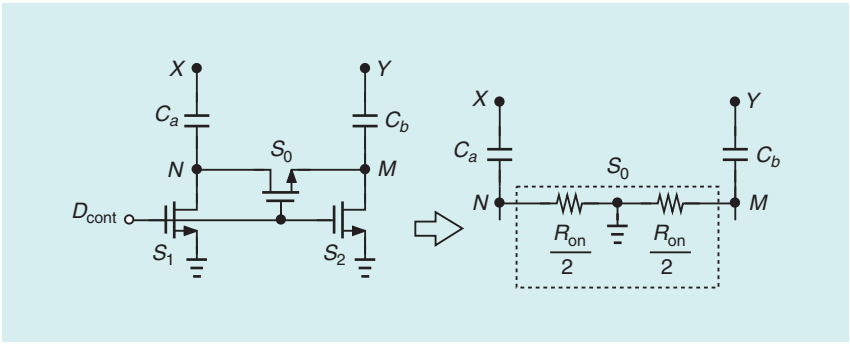

FIGURE 8: The use of a differential switch to alleviate the Q-capacitance tradeoff.

It is possible to improve the situation through the use of a "differential" switch. Illustrated in Figure 8, the idea is to recognize that the differential swings at X and Y also cause V_N and V_M to vary in opposite directions. Consequently, the "midpoint" of the channel of S_0 is at ac ground, introducing only half of the device's on-resistance in series with C_a and C_b.

We conclude that S_0 can be only 160 μm wide and yet afford a Q of 32 for these capacitors. The parasitic capacitance is then halved. When C_a and C_b are switched out, they appear in series with 140 fF/2, yielding a net value of $140\,\text{fF}/3 \approx 47$ fF. Repeating the foregoing calculations, we learn that the frequency rises by $\sqrt{610\,\text{fF}/517\,\text{fF}} = 8.6\% \approx 2.6$ GHz. Switches S_1 and S_2 can have minimum dimensions as they simply define a zero dc level for V_N and V_M.

Since we still do not meet our 4-GHz tuning target, we select $C_a = C_b = 175$ fF in Figure 8, at the cost of reducing the Q. Figure 9(a) shows our present design, and Figure 9(b) plots the PN at $f_0 = 28$ GHz and $f_0 = 32$ GHz (with the 175-fF capacitors switched in and out and with Vcont set to 100 and 850 mV, respectively.) The latter PN is higher than expected by a large amount, an effect studied in the next section.

We now decompose the 175-fF capacitors and the 160-μm switch into 10 units. The units need not be

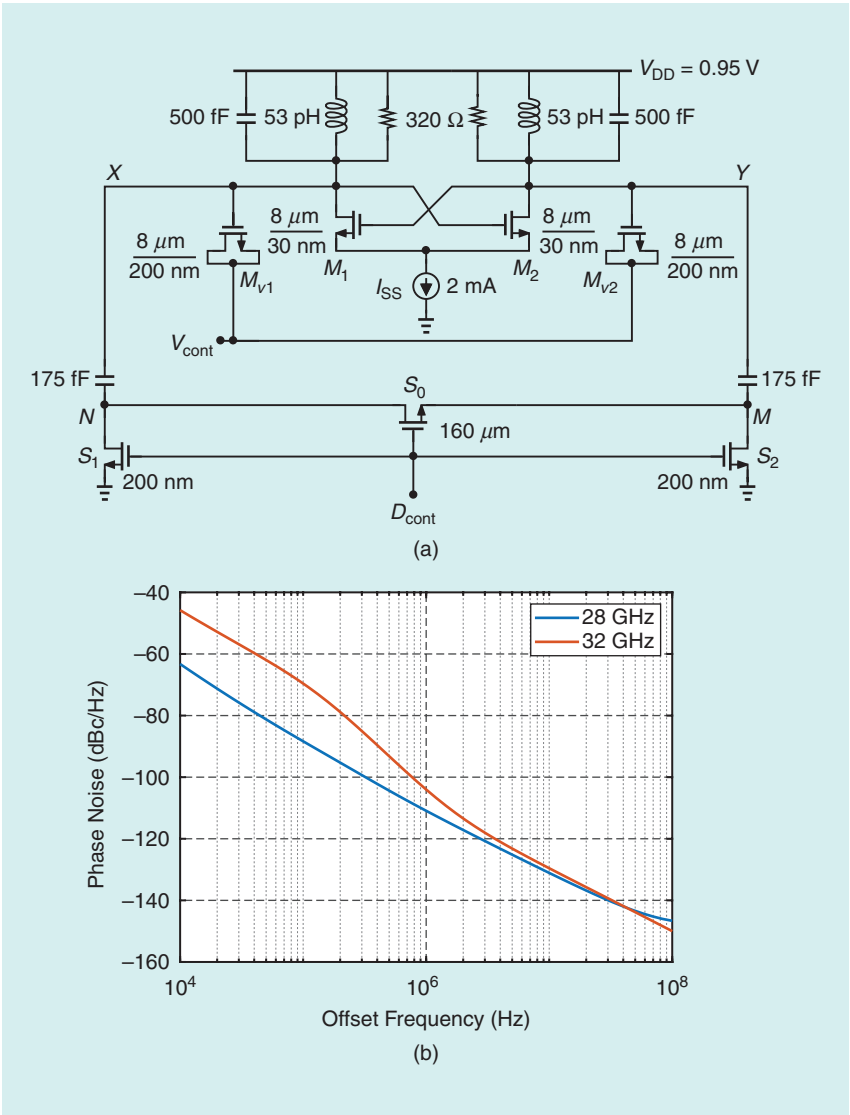

FIGURE 9: (a) The preliminary VCO design and (a) its PN profile at 28-GHz and 32-GHz oscillation frequencies.

identical. In fact, those that switch out at higher frequencies should be smaller so as to yield relatively uniform steps in the tuning range.

The Problem of Switch Flicker Noise

The discrete tuning circuit of Figure 8 presents an interesting issue when the switches are nominally off. Since V_N and V_M swing by several hundred millivolts, the switches turn on partially and inject flicker noise. Fortunately, the situation can be remedied by raising the CM level of N and M in the off mode. Illustrated in Figure 10(a), this is accomplished by tying these nodes to a dc level of about $V_{DD}/2$ through two large resistors. Figure 10(b) plots the PN before and after the resistors are added, suggesting that the degradation is almost completely avoided.

The method shown in Figure 10(a) does pose another difficulty; upon decomposing the network into, for example, 10 cells, we must scale the resistors up by the same factor. The large footprint of such devices makes the layout depicted in Figure 5(b) even more complex.

The Problem of the Tail Current Source

The ideal tail current source in the VCO of Figure 9(a) must now be realized by a current mirror arrangement [Figure 11(a)]. To conserve power, we are tempted to select a value of 5–10 for the mirror current multiplication factor, e.g., we have $I_{REF} = 400\,\mu$A. But the flicker and thermal noise of M_{REF} are amplified proportionally. The tail flicker noise current, I_n, simply adds to I_{SS} and introduces AM according to $(4/\pi)R_p(I_{SS} + I_n)$, evidently a benign effect as far as the output *phase* is concerned. However, the nonlinear capacitance at X and Y converts AM to PM [8]. The tail thermal noise at twice the oscillation frequency also manifests itself as PN around the carrier.

We should note that the worst case for AM/PM conversion in this design occurs when K_{VCO} is maximum. This is because the varactors

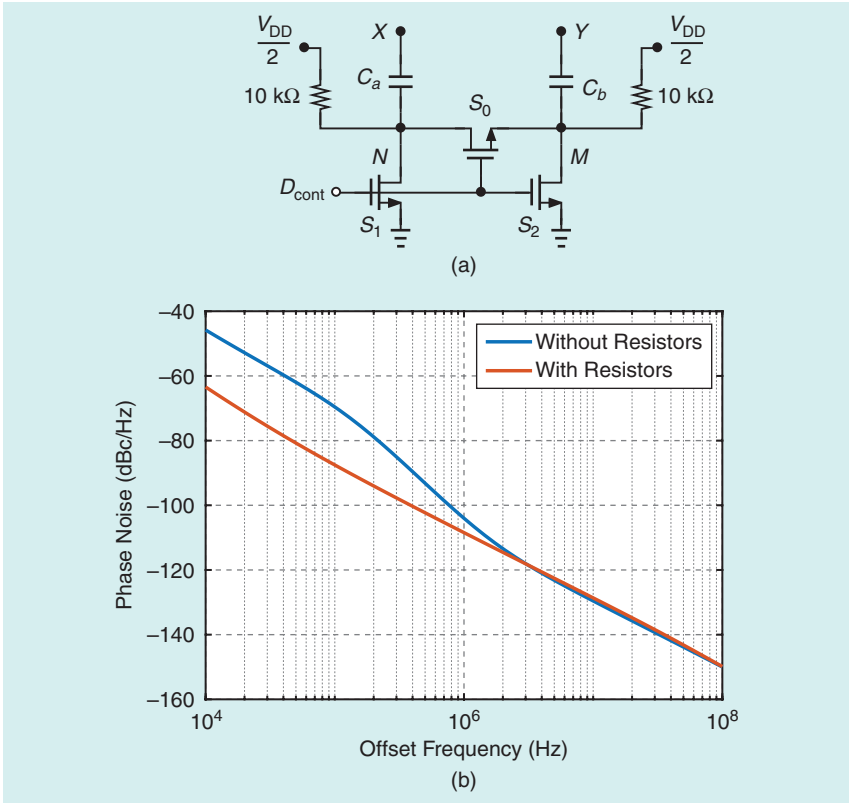

FIGURE 10: The use of pull-up resistors to avoid turning on the bottom-plate switches and (b) the effect of pull-up on the PN.

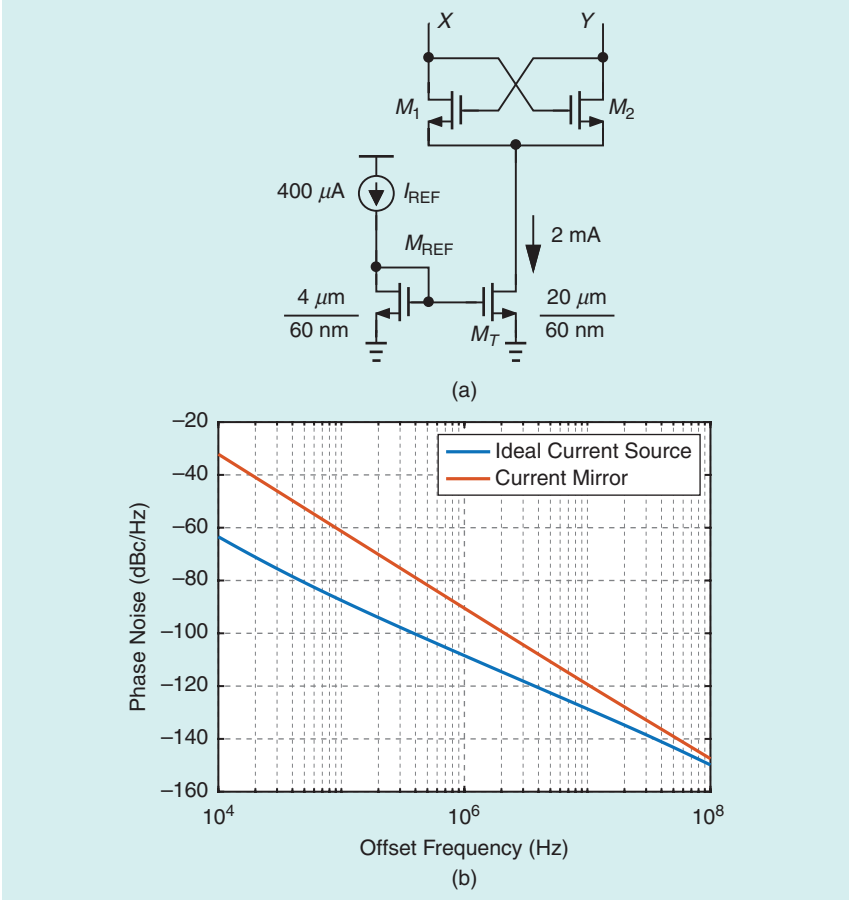

FIGURE 11: (a) Tail current source realization by a mirror arrangement and (b) its effect on PN.

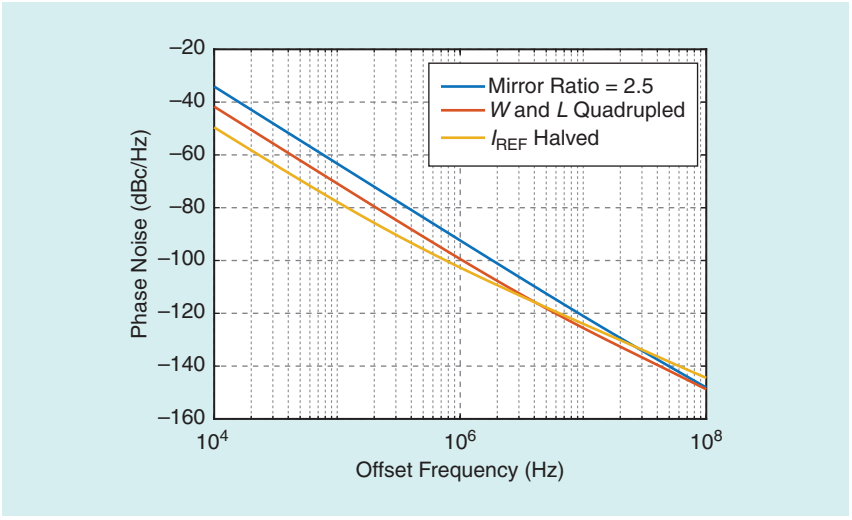

FIGURE 12: The VCO PN with a reduced mirror ratio, larger mirror transistors, and a lower tail current.

exhibit the greatest voltage dependence at this extreme. We then turn off the switched capacitors and set V_{cont} to 850 mV.

If we choose $(W/L)_{REF} = 4\,\mu m/60$ nm and $(W/L)_T = 20\,\mu m/60$ nm, we obtain the PN plotted in Figure 11(b), which also includes the profile corresponding to an ideal tail current source. The degradation is more than 20 dB at low offset frequencies.

To alleviate this issue, we decrease the mirror ratio to 2.5, allowing I_{REF} = 0.8 mA and $(W/L)_{REF} = 8\,\mu m/60$ nm, at the cost of not meeting our power budget. The new VCO PN is plotted in Figure 12, still higher than our specification of –100 dBc/Hz at 1-MHz offset. In the next step, we reduce the flicker noise of the two transistors by quadrupling their (drawn) widths and lengths. As shown in Figure 12, the PN at 1-MHz offset falls to –100 dBc/Hz.

Recognizing that flicker noise modulates the varactor capacitances (if they exhibit odd-order symmetry), we surmise that the effect can be alleviated if the voltage swings at X and Y are reduced. We therefore halve I_{REF} and observe a 3-dB drop in PN (Figure 12). This leads to a single-ended output swing of about 400 mV_{pp}, requiring that the VCO be followed by self-biased inverters if rail-to-rail swings are required.

References

[1] J.-C. Chen and L.-H. Lu, "Design of wide-tuning-range millimeter-wave CMOS VCO with a standing-wave architecture," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1942–1952, Sep. 2007, doi: 10.1109/JSSC.2007.903050.

[2] X. Liu, Z. Huang, J. Yin, and H. C. Luong, "Magnetic-tuning millimeter-wave CMOS oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2019, pp. 1–8, doi: 10.1109/CICC.2019.8780120.

[3] P. Andreani and H. Sjoland, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 342–348, Mar. 2002, doi: 10.1109/4.987086.

[4] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008, doi: 10.1109/JSSC.2008.2004867.

[5] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005, doi: 10.1109/JSSC.2005.845991.

[6] B. Razavi, *RF Microelectronics*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2012.

[7] B. Razavi, "The design of an LDO regulator," *IEEE Solid-State Circuits Mag.*, vol. 14, no. 2, pp. 7–17, Spring 2022, doi: 10.1109/MSSC.2022.3167308.

[8] S. Levantino, C. Samori, A. Zanchi, and A. Lacaita, "AM-to-PM conversion in varactor-tuned oscillators," *IEEE Trans. Circuits Syst. II. Analog Digit. Signal Process. (1993–2003)*, vol. 49, no. 7, pp. 509–513, Jul. 2002, doi: 10.1109/TCSII.2002.804051.

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