Behzad Razavi

The *R*-2*R* and *C*-2*C* Ladders

The *R*-2*R* and *C*-2*C* ladders are compact structures that can provide a variable impedance and/or a variable gain. As such, they have found use in analog, wireless, and wireline circuits. In this article, we study their properties and applications.

The *R*-2*R* Ladder

The *R*-2*R* ladder dates to the 1960s, as exemplified by the circuit shown in Figure 1 [1]. Here, resistors 78–81 are equal to R, and 71–77 are equal to $2R$, with units 60–64 acting as switches. The circuit can be viewed as a voltage-mode digital-to-analog converter (DAC) or a programmable attenuator operating on the signal produced by the transformer.

To understand the *R*-2*R* ladder's properties, we begin with the simple arrangement depicted in Figure 2(a), where the horizontal (bridge) and vertical (branch) resistors are equal to R and $2R$, respectively, except for the termination device, R_T, which is equal to R. We compute the impedance seen from the left by noting that the section in the dashed box is equivalent to R and, hence, the overall circuit recursively reduces to $2R$. We also see that the choice $R_T = R$ is necessary for the recursion to proceed consistently.

In the next step, let us tie equal current sources from each node to the ground [Figure 2(b)]. We wish to determine the Norton equivalent of the circuit as seen from the left. Again, we begin from the right and

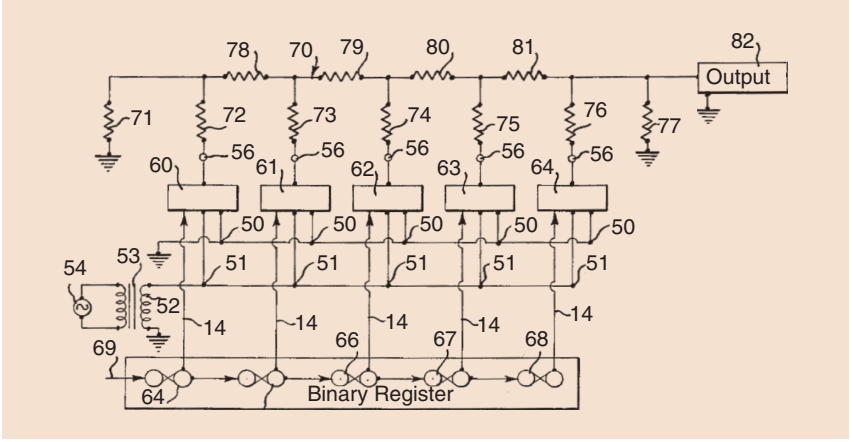

FIGURE 1: The *R*-2*R* ladder originally disclosed in [1].

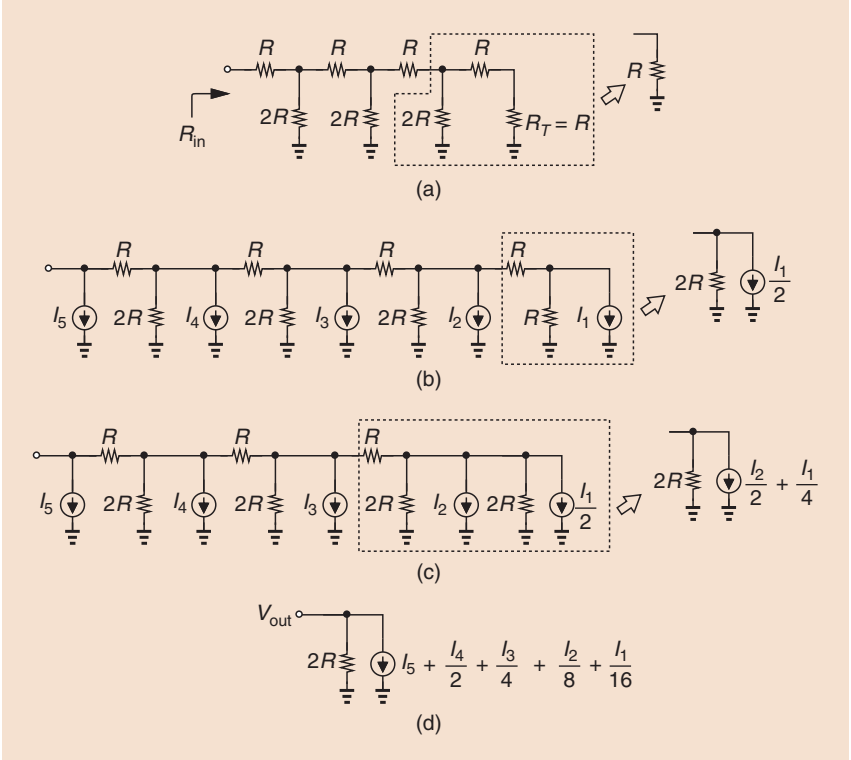

FIGURE 2: (a) The basic *R*-2*R* ladder, (b) the *R*-2*R* ladder DAC, (c) the Norton equivalent of two sections, and (d) the overall Norton equivalent.

Digital Object Identifier 10.1109/MSSC.2019.2922886
Date of publication: 27 August 2019

find the Norton equivalent of I_1 and the two resistors connected to it, recognizing that I_1 is halved. Reducing the circuit to that in Figure 2(c), we continue to merge current sources and resistors and replace them with their Norton equivalents. Illustrated in Figure 2(d), the final result reveals that the circuit provides a current equal to a binary-weighted sum of the unit current sources and exhibits an output resistance equal to $2R$. As such, the network can operate as a DAC. In that environment, I_1–I_5 are controlled by a digital binary input, with I_1 acting as the least-significant bit (LSB) and I_5 as the most-significant bit (MSB) [Figure 3(a)].

The principal advantage of the R-$2R$ DAC is its compact design; in the 5-b example, it requires only five unit current sources and 11 unit resistors (each equal to R). By comparison, a 5-b segmented (also called *thermometric*) DAC would employ 31 unit current sources.

The R-$2R$ DAC, however, suffers from two drawbacks. First, it necessitates stringent matching among the current sources for high-resolution applications. This can be seen by assuming that, in Figure 3(a), the digital input, $D_5 \ldots D_1$, goes from 01111 to 10000. We call this change the *MSB transition*. Consequently, I_1–I_4 turn off, while I_5 turns on, and the output current, I_{out}, increases by 1 LSB only if

$$I_5 = \frac{I_4}{2} + \frac{I_3}{4} + \frac{I_2}{8} + \frac{I_1}{16} + 1\,\text{LSB}. \quad (1)$$

While fairly relaxed in this 5-b example, such a matching condition becomes difficult to meet for resolutions greater than 7 or 8 b. If, due to mismatches, the MSB current source happens to be slightly *less* than the weighted sum of the remaining current sources, I_{out} *falls* as D_{in} goes from 011…1 to 10…0, creating a nonmonotonic characteristic [Figure 3(b)]. By contrast, a segmented architecture is free from nonmonotonicity.

The second drawback of the R-$2R$ DAC relates to the voltage drop incurred by the resistor ladder. As shown by Figure 3(a), with $D_5 D_4 \ldots D_1 = 11\ldots1$, we have

$$V_{out} - V_1 = \frac{R}{2}\left(I_4 + \frac{3I_3}{2} + \frac{7I_2}{4} + \frac{15I_1}{8}\right) \quad (2)$$

$$= \frac{49}{16} R I_u, \quad (3)$$

where I_u denotes the nominal value of each current source. This drop reduces the voltage headroom for I_1 and creates a mismatch between I_5 and I_1 due to channel-length modulation. The other current sources experience similar effects.

The simplified topology in Figure 2(d) points to another possible application of R-$2R$ ladders. Writing

$$V_{out} = -2R\left(I_5 + \frac{I_4}{2} + \frac{I_3}{4} + \frac{I_2}{8} + \frac{I_1}{16}\right), \quad (4)$$

we note that a current entering different nodes experiences different weighting factors as it translates to V_{out}. Bearing this property in mind, we consider a radio-frequency (RF) mixer that generates an output current and follow it by such a ladder so as to realize a programmable gain. Illustrated in Figure 4 [2], the circuit senses an RF input, V_{RF}, converts it to current, and mixes the result with the local oscillator (LO) signal. The downconverted current, I_{out}, is then injected into only one of the nodes of an R-$2R$ ladder. From (4), we have

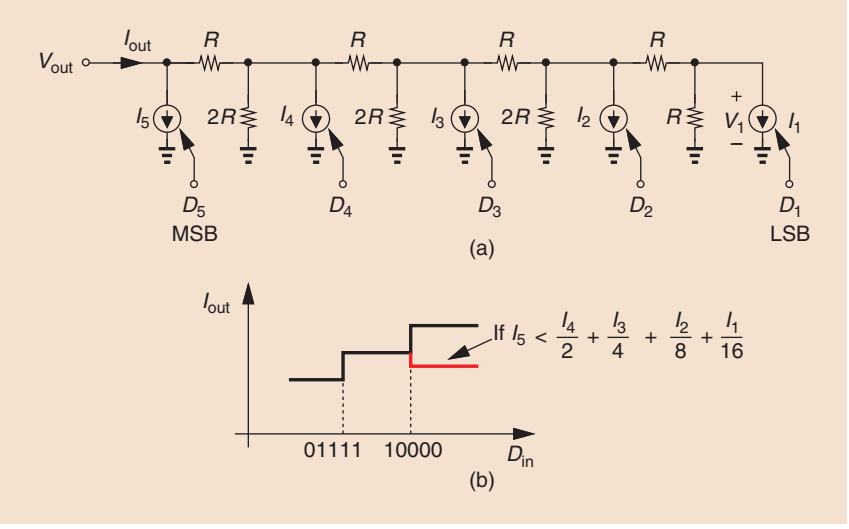

FIGURE 3: (a) The problem of voltage drop along the ladder and (b) the effect of mismatch between the MSB current source and LSB current source.

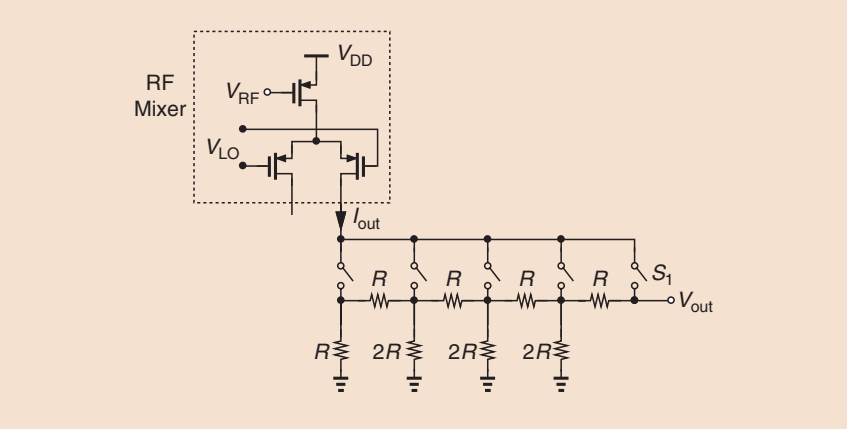

FIGURE 4: The use of an *R*-2*R* ladder in an RF mixer.

$$V_{out} = 2R\frac{I_{out}}{2^N}, \tag{5}$$

where $N = 0$ when S_1 is on. The ladder can be viewed as a variable "transresistor" having a transresistance equal to $2R/2^N$. A key property of this mixer topology is that its gain steps are linear in decibels; for instance, as N increases by 1, the gain drops by 6 dB.

The R-$2R$ ladder can also act as a variable resistor [3]. Depicted in Figure 5(a), the structure is driven by a voltage while delivering a current to an ac or virtual ground. Note that R_T in Figure 2(a) is split into two parallel resistors equal to $2R$, with one controlled by the switches. It can be shown that [3]

$$\frac{V_{in}}{I_{out}} = \frac{R}{\sum_{j=1}^{N}\frac{D_j}{2^j}}, \tag{6}$$

where D_j denotes the bit controlling the switches tied to node j. Interestingly, the input resistance is constant but not the output resistance. This programmable resistor proves useful in automatic gain control, as exemplified by the arrangement presented in Figure 5(b). Here, the input and feedback resistors are programmable, providing a wide range of gain settings.

Another interesting application of R-$2R$ ladders is described by [4] in the context of wireline transmitters. Such systems subject the data to de-emphasis to amplify their high-frequency components and partially compensate for the loss of the medium in which they travel. In the time domain, this is equivalent to deliberately creating over- and undershoots in the data waveform. The de-emphasis function is typically realized by a feedforward equalizer (FFE), conceptually illustrated in Figure 6(a). The data sequence, D_{in}, is delayed by one period, scaled by a factor of α, and subtracted from itself. The scaling factor is adjusted according to the loss of the channel.

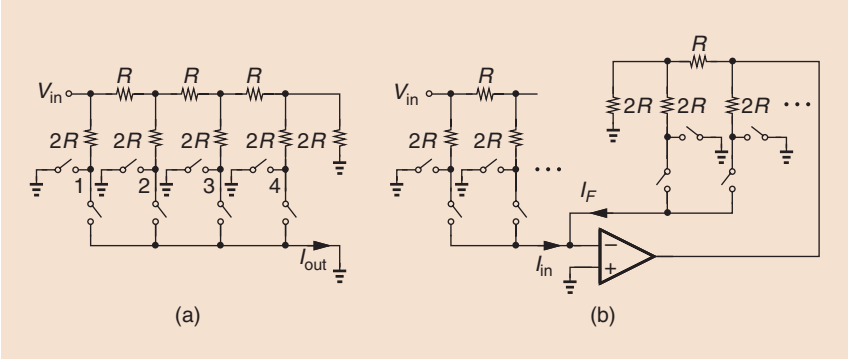

FIGURE 5: (a) The R-$2R$ ladder as a programmable resistor and (b) its use in an amplifier.

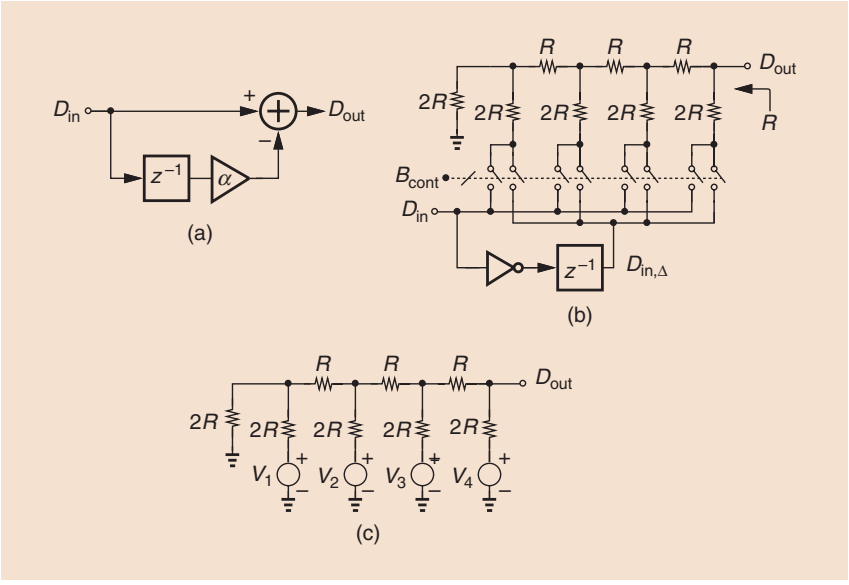

FIGURE 6: (a) A basic FFE, (b) the realization using an R-$2R$ ladder, and (c) the equivalent circuit.

Shown in Figure 6(b), the voltage-mode transmitter in [4] employs an R-$2R$ ladder to provide a programmable scaling factor and perform the summation of D_{in} and its delayed replica, $D_{in,\Delta}$. According to the digital control, B_{cont}, the bottom terminals of the $2R$ units are connected to either D_{in} or $D_{in,\Delta}$. We simplify the topology as depicted in Figure 6(c) and denote D_{in} or $D_{in,\Delta}$ by voltage sources V_1–V_4. The output contains binary-weighted copies of the two signals. Thus, the network applies scaling factors to D_{in} and $D_{in,\Delta}$. A key attribute of this architecture is that the transmitter output impedance remains constant and equal to R for different switch settings if the driving impedances at D_{in} and $D_{in,\Delta}$ are negligible.

The C-2C Ladder

With the growing popularity of CMOS technology in the 1970s, a capacitive counterpart of the R-$2R$ ladder proved necessary. Early examples of DACs employing C-$2C$ networks include [5] and [6].

Figure 7 shows a basic C-$2C$ DAC, which incorporates a value of $2C$ for the bridge capacitors, except for the rightmost one, and C for the branch units. The two switches tied to each bottom plate can provide a voltage swing equal to V_{REF}. The circuit operates as follows. First, switch S_0 turns on, resetting V_{out} to zero (or a desired common-mode level), while the bottom plates of the branch capacitors are tied to the ground. Next, S_0 turns off, and, according to the value of the digital input, $D_5 \ldots D_1$, some bottom plates swing to V_{REF}. As indicated by the dashed box, we can begin from the right and recursively construct Thevenin equivalents for the DAC. Each Thevenin equivalent exhibits an output series capacitance of $2C$,

allowing consistent recursion. It follows that

$$V_{out} = D_5 \frac{V_{REF}}{2} + \cdots + D_1 \frac{V_{REF}}{32}. \quad (7)$$

In this example, the DAC requires 14 unit capacitors, in comparison with a segmented topology using 32 units.

As with all capacitor DACs, the output voltage in Figure 7 suffers from kT/C noise when S_0 turns off. The total capacitance seen between the output node and the ground is equal to $2C$ and must be large enough to yield acceptable noise.

A difficult issue in C-$2C$ ladders, absent in the R-$2R$ counterpart, relates to the parasitic capacitances accompanying the bridge and branch capacitors. At least one plate of each capacitor exhibits a parasitic, C_p, to the ground. Let us include one C_p in the LSB section (Figure 8) and construct its Thevenin equivalent. We note two issues here.

1) The Thevenin capacitance departs from $2C$, prohibiting recursion and causing errors in the voltage divisions that occur beyond the LSB section.
2) The Thevenin voltage deviates from its ideal value as well.

Both contribute nonlinearity to the DAC's input-output characteristic. The analysis in [7] quantifies the nonlinearity in terms of C_p/C.

We can attempt to correct for C_p by adjusting the bridge or branch capacitor values. Suppose we select the bridge capacitors equal to αC, as shown in Figure 9(a), but with the rightmost C replaced by the series combination of two units equal to αC. If the two errors mentioned in the previous paragraph are to be nulled, the Thevenin capacitance of the dashed box must be equal to αC so that the recursion can continue:

$$C + C_p + \frac{\alpha C}{2} = \alpha C. \quad (8)$$

That is,

$$C = \frac{1}{\frac{\alpha}{2} - 1} C_p. \quad (9)$$

Also, the Thevenin voltage must be equal to $V_{REF}/2$:

$$\frac{C}{C + C_p + \frac{\alpha C}{2}} V_{REF} = \frac{V_{REF}}{2}, \quad (10)$$

and hence

$$C = \frac{1}{1 - \frac{\alpha}{2}} C_p. \quad (11)$$

Equations (9) and (11) imply that no solution exists.

Let us introduce one more variable and select the rightmost capacitor in Figure 9(a) equal to βC [Figure 9(b)]. Repeating the foregoing conditions for the Thevenin capacitance and voltage of the dashed box, we have

$$\beta = 2, \quad (12)$$

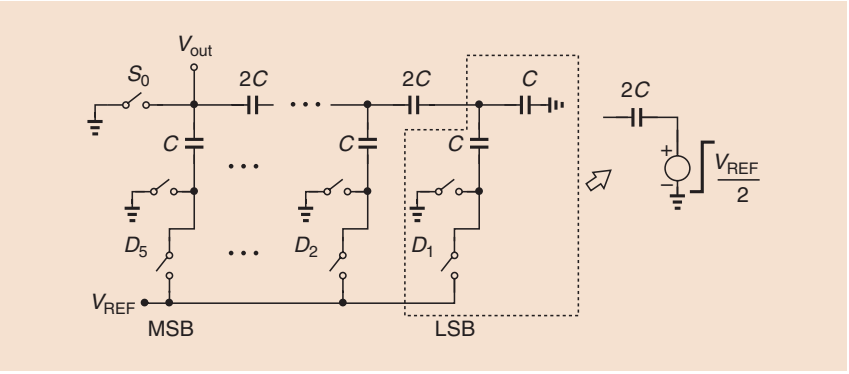

FIGURE 7: The basic C-$2C$ ladder DAC.

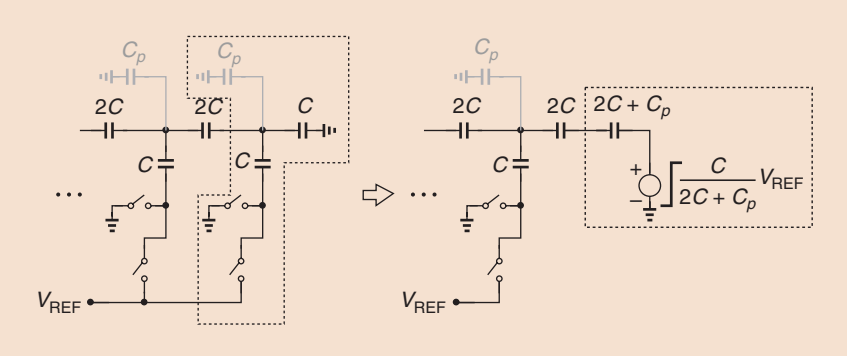

FIGURE 8: The effect of parasitic capacitances on the C-$2C$ DAC performance.

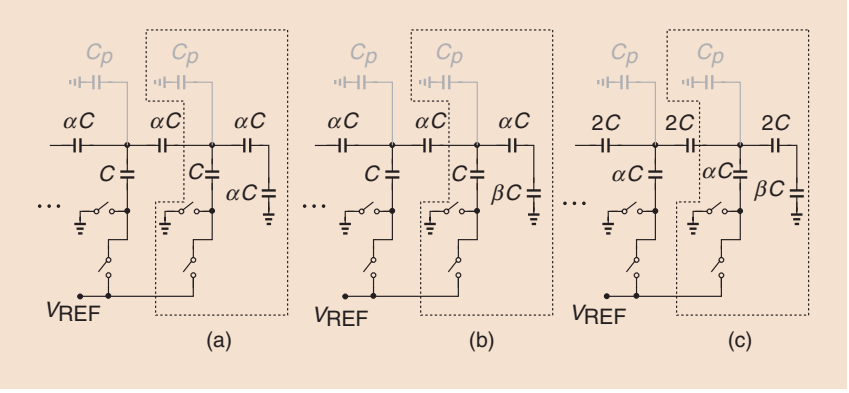

FIGURE 9: The correction for parasitic capacitances by changing (a) the bridge capacitors and the rightmost capacitor to αC, (b) the bridge capacitors to αC and the rightmost capacitor to βC, and (c) the branch capacitors to αC and the rightmost capacitor to βC.

$$\alpha = 2\frac{C - C_p}{C + C_p}, \tag{13}$$

and

$$\alpha \approx 2\left(1 - \frac{C_p}{C}\right)^2, \tag{14}$$

if $C_p \ll C$. A solution exists, but α must be slightly *less* than two, an undesirable condition because it is difficult to subtract a certain amount from a capacitor. In our final trial, we assign a capacitance of αC to the branches while keeping the rightmost capacitor equal to βC [Figure 9(c)]. Now, the conditions emerge as

$$\beta = 2 \tag{15}$$

and

$$\alpha C = C + C_p. \tag{16}$$

That is, the branch capacitors must be raised by a value equal to C_p. Although C_p is not precisely defined, an approximation thereof can be added to the unit C, thus providing partial correction and lowering the DAC nonlinearity.

Owing to its compact nature, the C-$2C$ ladder has found a wide range of applications. In [8], a 7-b successive approximation register (SAR) analog-to-digital converter (ADC) employs a variant of such a network and calibrates the effect of the parasitic capacitances. As shown in Figure 10, this is accomplished by adding

1) a programmable capacitor, C_B, to each node that absorbs C_p and reaches $C/2$ after calibration
2) a section consisting of C and C_{cal} that injects or removes charge from the array.

During calibration, a known voltage is applied to the ADC input, and V_{cal} is adjusted to obtain the correct digital output [8].

Another application of C-$2C$ ladders aims for high-frequency resolution in digitally controlled oscillators (DCOs) [9]. A critical issue affecting the output jitter of digital phase-locked loops, the DCO output frequency steps must often be less than 1 part per million with respect to the oscillation frequency itself. Such fine steps demand extremely small unit capacitors in the tuning network of IC DCOs. To avoid dealing with the parasitics and modeling issues related to very small geometries, we seek methods that attenuate the effect of a capacitor.

The DCO in [9] is realized as shown in Figure 11, where tuning elements $2\Delta C$ and ΔC are added to each section and controlled by 2 b. Let us begin with the rightmost section and denote the programmable component by $k\Delta C$, where $k = 0$, 1, 2, or 3. Thus,

$$C_{\text{eq}} = \frac{2C(2C + k\Delta C)}{2C + 2C + k\Delta C} \tag{17}$$

and

$$C_{\text{eq}} \approx C + \frac{k}{2}\Delta C, \tag{18}$$

where $k\Delta C$ in the denominator is neglected. Continuing the recursion, we observe that each section presents at its input three components: one equal to C, one equal to half its own programmable capacitance, and one equal to half the total programmable capacitance presented by the section to its right. In other words, the capacitance loading the oscillator can be expressed as

$$C_{\text{in}} = C + \frac{k_1\Delta C}{2} + \frac{k_2\Delta C}{4} + \frac{k_3\Delta C}{8} + \cdots, \tag{19}$$

where $k_j\Delta C$ denotes the value of the programmable capacitance in section j. This result suggests that the effect of ΔC can be reduced arbitrarily if the capacitor is placed deep in the cascade. Indeed, the DCO in [9] employs 14 sections to achieve a remarkable frequency resolution of 4 Hz at 60 GHz.

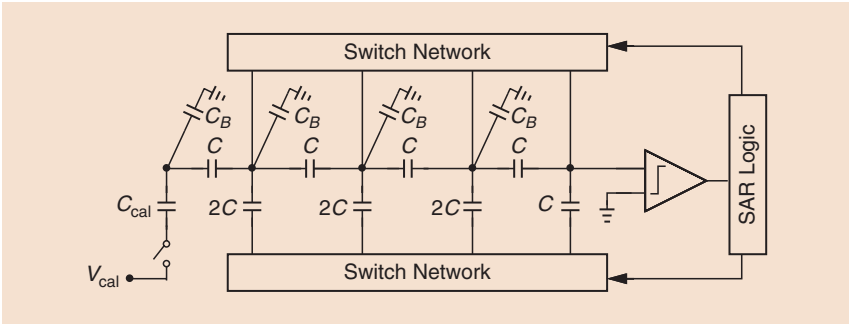

FIGURE 10: A SAR ADC using a variant of the C-$2C$ ladder.

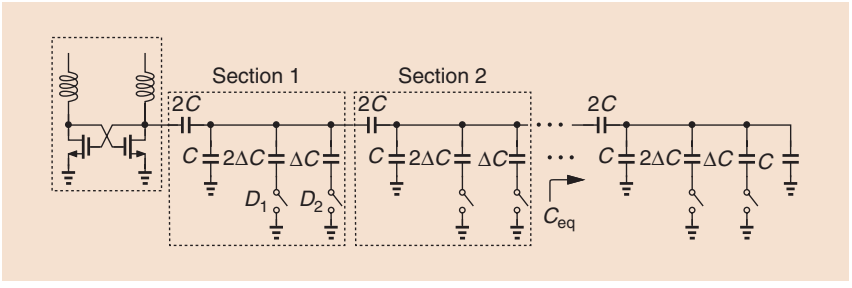

FIGURE 11: A DCO using a C-$2C$ ladder for fine frequency control.

Answers to Last Issue's Questions

1) How does C_M shape the power-supply rejection ratio (PSRR) of the circuit in Figure 12?

   Let us assume that the op amp has a one-pole response equal to $A_0/(1 + s/\omega_0)$ and the small-signal resistance, R_L, is much less than $R_1 + R_2$. We open

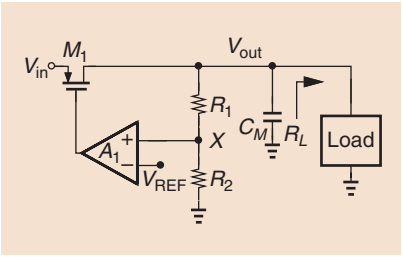

FIGURE 12: The use of a smoothing capacitor to absorb load transient currents.

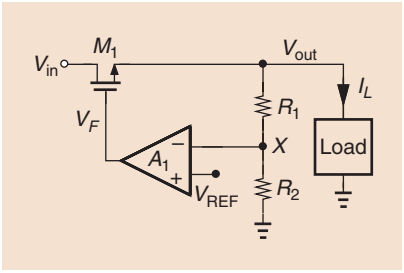

FIGURE 13: Low dropout using a source follower.

the loop at the input of A_1 and note that C_M contributes a pole given by $\omega_M \approx 1/(R_L C_M)$. This pole is typically far above ω_0. It follows that the closed-loop PSRR rises and then begins to fall as C_M manifests itself.

2) The op amp gain in Figure 13 falls at high frequencies. Can we place a capacitor in parallel with R_1 to counteract this effect and maintain a relatively constant loop gain?

Yes, a capacitor in parallel with R_1 yields a zero in the open-loop transfer function, potentially improving the phase margin and allowing a wider, stable closed-loop bandwidth.

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