Systematic Transistor and Inductor Modeling for Millimeter-Wave Design

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***Abstract*—This paper proposes a simulation-based modeling methodology that provides greater flexibility in the design and layout of millimeter-wave CMOS circuits than measurement-based models do. A physical model for the metallization capacitances of the transistors is described and new layout techniques are introduced that exploit these capacitances to improve the circuit performance. The accuracy of the models is verified by the design and measurement of five oscillators operating in the range of 40 GHz to 130 GHz in 90-nm CMOS technology.**

***Index Terms*—High-frequency MOS models, inductor models, interconnect models, millimeter-wave circuit design, millimeter-wave layout techniques, MOS device capacitances.**

I. Introduction

THE heightened interest in millimeter-wave (mm-wave) applications such as broadband wireless links, radars, and imaging systems has led to extensive research in CMOS circuit and architecture design for these frequencies [1]–[5]. A critical issue that can potentially introduce significant discrepancies between the simulated and measured performance of such circuits relates to the modeling of their constituent devices. In fact, even the effect of interconnects *within* the transistors substantially alters the behavior of mm-wave designs. Also, typical parasitic extraction tools used in post-layout simulations prove inadequate here because they do not take into account frequency dependencies or distributed effects.

This paper proposes a systematic simulation-based modeling methodology for transistor capacitances and spiral inductors that can be applied to various device geometries while providing physical representations. Applied to the complex layout of five CMOS oscillators in the range of 40 to 130 GHz, the methodology predicts their oscillation frequencies with a maximum error of 3.2% with no fabrication or modeling iterations.

Section II of the paper describes the challenges in mm-wave modeling, contending that measurement-based models severely constrain the design and layout of devices and circuits. Section III introduces the transistor capacitance modeling methodology and the resulting device models. Section IV deals with interconnect and inductor modeling, and Section V presents new layout techniques. Section VI describes the experimental results.

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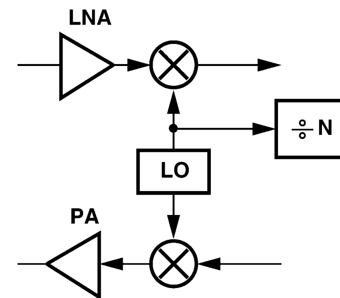

Fig. 1. Generic transceiver front end.

II. Millimeter-Wave Modeling Issues

Recent work on transistor modeling has been based on the measurement of fabricated devices, yielding models expressed as a black box (e.g., with S-parameters) or as a fitted physical representation with additional parasitics [4], [5]. As such, this type of model makes it exceedingly difficult to depart from the specific geometry of the fabricated devices, thereby constraining the design and layout of circuits considerably. Moreover, due to various folding and routing techniques needed to create a compact layout for a given device size, the model is not scalable. Also, measurement of MOS devices, especially those with a small width, becomes difficult at these frequencies due to errors introduced by inaccurate de-embedding from calibration structures and coupling between probes.

In order to appreciate the limitations imposed by models that are solely based on measurements, we consider a number of situations that arise in practice.

1) In the representative front end shown in Fig. 1, different building blocks may require vastly different transistor geometries. For example, in the receiver reported in [1], the LNA, the RF mixer, the oscillator, and the ÷2 circuit employ, in the high-frequency path, transistor widths equal to 30 μm, 20 μm, 16 μm, 8 μm, 7 μm, 6 μm, 5 μm, 4 μm, and 1 μm. Without a priori knowledge of these dimensions, fabricated stand-alone transistors would represent only a few, necessitating some type of extrapolation or interpolation for others—but suffering from uncertainties due to the change in the interconnects.
2) In addition to the width and number of gate fingers and the folding factor, other aspects of a transistor geometry may need to be tailored to the circuit environment. For example, as explained in Section III, the drain-source capacitance can be reduced at the cost of increasing the drain and source junction capacitances, a useful trade-off in common-gate (CG) and cascode stages. If the fabricated transistors do not

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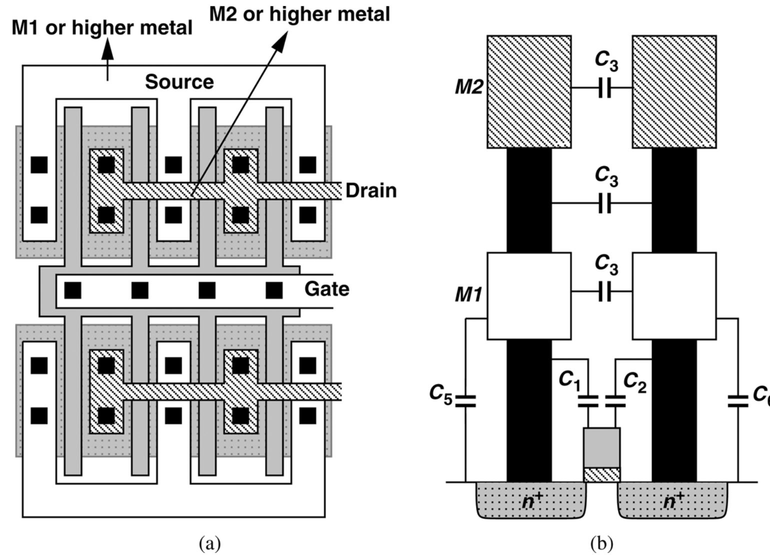

Fig. 2. (a) Folded transistor layout, and (b) layout cross section.

include such variants, the model cannot be readily applied to these cases.

3) In deep-submicron technologies, most transistors are surrounded by dummy gate fingers so as to reduce mismatches resulting from the stress due to shallow trench isolation [6], [7]. The position and number of these fingers depend on the particular circuit design and layout but they affect the extrinsic connections to the device and hence its model.
4) Reliance on measurement-based models prohibits the use of additional (perhaps unrelated) interconnects *over* the transistors lest the additional couplings may not be included correctly. In complex layouts, therefore, many of the interconnects must travel *around* the transistors, suffering from unnecessary capacitance and loss.

The use of black-box S-parameter-based models in circuit simulations also faces critical issues: for complex topologies, the simulator may not converge; different interpolation methods used to handle the discrete S-parameter values yield different results; and, most importantly, S-parameters are obtained at certain bias conditions and hence cannot represent the behavior of large-signal circuits such as mixers, oscillators, dividers, and power amplifiers.

The above observations point to the need for a modeling methodology that crosses the bridge between model accuracy and design flexibility, allowing the designer to confidently try new topologies without fear of modeling inaccuracies.

III. Proposed Transistor Modeling Methodology

Consider the transistor layout shown in Fig. 2(a), where the top and bottom sections form a folded multi-finger device, thus reducing the inductance of the horizontal interconnects. A single gate stripe is shared between the two sections so as to lower the gate resistance and inductance. The source connections may utilize metal 1 or, if the source to substrate capacitance is critical, a higher metal level. The drain connections, on the other hand, must be formed in metal 2 or a higher level. The numerous variants of this layout also exemplify the need for systematic simulation-based modeling.

Now, consider the transistor cross section shown in Fig. 2(b) (the dimensions are drawn to scale). In short-channel devices, e.g., in 90-nm technology, the source and drain metallization contributes significant capacitances: the source and drain contacts are only 90 nm away from the gate, raising the overlap capacitance (C_1 and C_2), and the source and drain metal 1 lines are spaced by only 0.28 μm, creating a large capacitance (C_3) between these two terminals. The latter becomes particularly problematic if several vias are stacked on top of the source and drain regions to meet metal current density requirements or to allow interconnections within multi-finger structures. Neglected in most circuits, the drain-source capacitance can significantly alter the performance of common-gate and cascode stages (Section V).

In order to reduce $C_1 - C_3$, the S/D areas can be widened and the contacts moved farther from the gate poly, but at the cost of higher junction capacitance and a slight increase in the S/D resistance. Since the resistance is more critical in the source terminal, one may opt to widen only the drain junction.

In the proposed methodology, each transistor layout, including the gate poly but excluding the source and drain junctions, is imported into Ansoft HFSS and simulated as a three-port network in the frequency range of interest. The parasitics are thus extracted as the network depicted in Fig. 3(a). Careful layout of the transistor can minimize the gate resistance, making the extracted components primarily capacitive. In fact, simulations confirm that the imaginary parts of the Y-parameters are one to two orders of magnitude greater than their real parts and vary linearly with frequency.[1] Fig. 3(b)

[1]Negligible resistance in series with the extrinsic capacitors does not necessarily mean that the resistance in series with the intrinsic gate capacitance is also negligible. But for a device width of 10 μm (10 1-μm fingers), the total gate resistance (including the resistance of vias) is estimated to be 5 Ω, a value much smaller than $1/g_m$ of the transistor and hence negligible [8].

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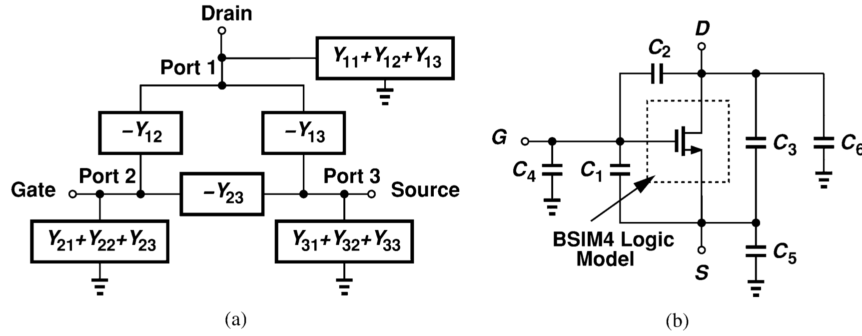

Fig. 3. (a) Three-port Y-parameter model, and (b) proposed device parasitic model.

shows the overall device model, where the core transistor is simply represented by the BSIM4 logic model and the capacitance values are obtained from the Y-parameters according to the following equations:

$$C_1 = \frac{-\mathrm{Im}\{Y_{23}\}}{\omega} \tag{1}$$

$$C_2 = \frac{-\mathrm{Im}\{Y_{12}\}}{\omega} \tag{2}$$

$$C_3 = \frac{-\mathrm{Im}\{Y_{13}\}}{\omega} \tag{3}$$

$$C_4 = \frac{\mathrm{Im}\{Y_{21} + Y_{22} + Y_{23}\}}{\omega} \tag{4}$$

$$C_5 = \frac{\mathrm{Im}\{Y_{31} + Y_{32} + Y_{33}\}}{\omega} \tag{5}$$

$$C_6 = \frac{\mathrm{Im}\{Y_{11} + Y_{12} + Y_{13}\}}{\omega}. \tag{6}$$

Note that the overall gate resistance can be included as a lumped resistor in series with the gate.

The resulting model is relatively scalable if only the number of gate fingers is varied. Fig. 4 plots the three significant capacitances as a function of transistor width, revealing only a small error in linear scaling and indicating that electromagnetic simulations are not necessary for all device widths.

An important advantage of the proposed methodology over standard extraction tools is that it computes the capacitances at the frequency of interest rather than at low frequencies. Owing to high frequency current crowding within the conductors, the capacitance values exhibit frequency dependence, incurring significant errors if calculated by extraction tools. These errors are quantified in Section VI.

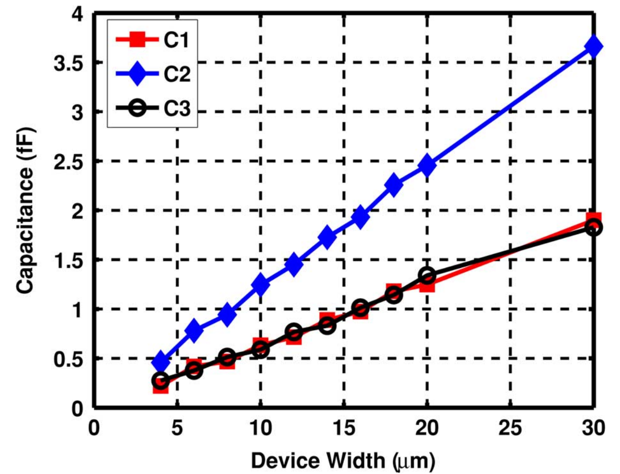

Fig. 4. Major transistor parasitics at 60 GHz.

IV. Interconnects and Inductors

A. Extrinsic Interconnects

The interconnects that appear between devices must also be modeled accurately. This can be accomplished by importing each interconnect to HFSS, simulating it as a multi-port network, and returning the resulting S or Y-parameters to the circuit simulator. Although not essential, a transmission line model can alternatively be developed for each interconnect.

A particularly problematic situation arises if a line travels above an unrelated transistor. Illustrated in Fig. 5, such a case is another example of difficulties in using measurement-based models. To determine the coupling capacitances between the line and the device, the five-port network consisting of the transistor and the segment of the line between points 4 and 5 is simulated in HFSS. The coupling capacitances between the line and the transistor are obtained from equations such as the following:

$$C_{14} = \frac{-\mathrm{Im}\{Y_{14}\}}{\omega} \tag{7}$$

$$C_{24} = \frac{-\mathrm{Im}\{Y_{24}\}}{\omega} \tag{8}$$

$$C_{34} = \frac{-\mathrm{Im}\{Y_{34}\}}{\omega}. \tag{9}$$

B. Inductors

As with interconnects, inductors can be simulated in HFSS and imported into a circuit simulator as a two-port black box. However, such a model imparts little physical understanding of the inductor's parasitics and their impact. Alternatively, a physical RLC model can be developed that provides greater insight into such properties as the quality factor and parasitic capacitances and their dependence upon single-ended or differential excitations. Fig. 6 shows an inductor model derived from that in [9] which lends itself to element-by-element extraction from Y-parameters while providing a high accuracy across a wide bandwidth, e.g., from 20 to 75 GHz. Based on the skin effect

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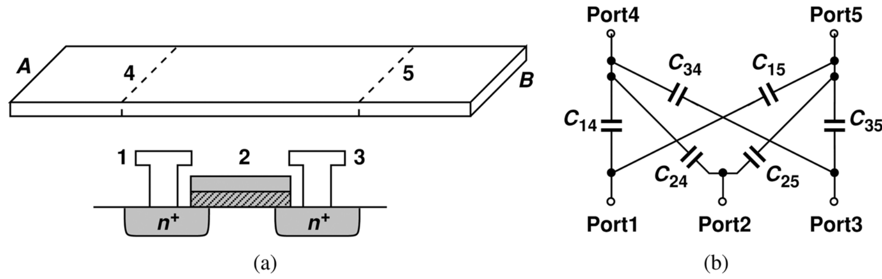

Fig. 5. (a) Line over a transistor, and (b) model of parasitics.

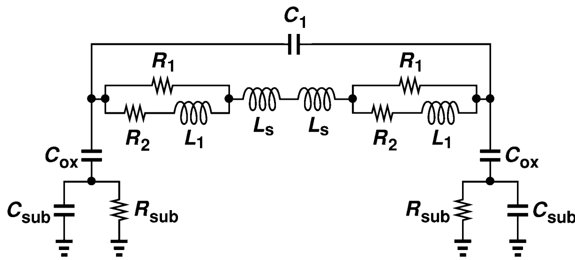

Fig. 6. Inductor model derived from that in [9].

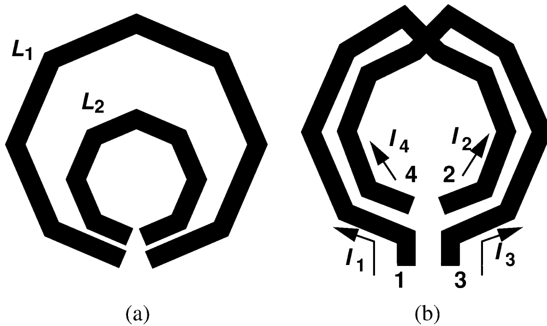

Fig. 7. (a) Nested and (b) intertwined inductors.

model in [10], this network employs the parallel combination of R_1 and $L_1 s + R_2$ to represent broadband loss.

The physical model can be extended to more complex geometries but may prove cumbersome in some cases. For example, the nested inductors depicted in Fig. 7(a), [1] experience both magnetic and electric coupling, making it difficult to fit an accurate RLC model. In the initial phases of design and layout, the structure can be modeled as two independent inductors and a simple mutual coupling factor between the two. However, one may eventually import the model from HFSS as a four-port black box in the final phase of the layout to retain the accuracy of the coupling effects.

Another example is shown in Fig. 7(b), where a symmetric structure is broken at its center tap, thereby producing two equal inductors with all four terminals in close proximity. Also, the mutual coupling between the two reduces the total required area. A general RLC model of this topology is rather complex but if the voltages at nodes 1 and 3 and those at nodes 2 and 4 are differential, each inductor, e.g., that between 1 and 2, can still be represented as a two-port network. As shown in Appendix A, such a network is governed by the following equations:

$$I_1 = (Y_{11} - Y_{13})V_1 + (Y_{12} - Y_{14})V_2 \tag{10}$$

$$I_2 = (Y_{21} - Y_{23})V_1 + (Y_{22} - Y_{24})V_2. \tag{11}$$

The equivalent Y-parameters of the two-port network are thus given by $Y_{11}-Y_{13}, Y_{12}-Y_{14}, Y_{21}-Y_{23}$, and $Y_{22}-Y_{24}$, allowing a similar RLC model to be constructed.

V. Layout Techniques

The comfort level afforded by the systematic modeling described above encourages us to try new layout techniques that can improve the performance of circuits. In this section, we present two such techniques.

As evident from Fig. 4, the largest extrinsic capacitance resulting from metallization appears between the gate and the drain—exactly where it degrades the performance the most! Experiencing Miller effect, this capacitance manifests itself in amplifiers, buffers, latches, and oscillators.

It is possible to modify the layout of the transistor in a differential pair so as to create additional *negative* Miller capacitance, thus canceling the effect of the extrinsic and intrinsic $C_{\rm GD}$. Illustrated in Fig. 8, the idea is to bend and route the drain line of each transistor next to the gate stripe of the other while maintaining symmetry. In order to obtain enough capacitance, the adjacent lines employ $M1$ through $M6$.

As an example, Table I summarizes the extrinsic capacitances of the two transistors with $W = 10$ μm (10 1-μm fingers) before and after this layout modification, obtained according to the proposed methodology. The intrinsic capacitances are also shown for reference. We note that the negative Miller capacitances, C_{D1G2} and C_{D2G1}, are raised to 2.01 fF but at the cost of a slight increase in the drain-substrate capacitance and the drain-drain capacitance. These penalties prove negligible with respect to the total capacitance at the drain node (including the input capacitance of a subsequent stage).

In the topology of Fig. 8, the additional drain line traveling next to the gate line exhibits negligible inductance, as evidenced by the small variation of the simulated extrinsic capacitances in the frequency range of 20 GHz to 80 GHz (less than 1%). Also, additional metal levels can be stacked to further increase the negative Miller capacitance and partially cancel the intrinsic $C_{\rm GS}$.

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TABLE I
EXTRINSIC AND INTRINSIC CAPACITANCES OF A DIFFERENTIAL PAIR IN CONVENTIONAL AND PROPOSED LAYOUTS

(fF)	C_{GD1}	C_{D1D2}	C_{D1G2}	C_{D2G1}	C_{GD2}	C_{G1G2}	C_{DS1}	C_{DS2}	C_{GS1}	C_{GS2}
Standard Layout	0.68	0.02	0.032	0.032	0.67	0.98	1.1	1.1	0.62	0.62
Proposed Layout	0.87	1.03	2.01	2.01	0.87	0.09	1.15	1.15	0.67	0.67
Intrinsic Capacitances	2.75				2.75				8.4	8.4

TABLE II
COMPARISON SUMMARY

	Oscillation Frequency (GHz)				
	Oscillator Type I		Oscillator Type II		
	$L_1 + L_2$		$L_1 + L_3 = L_2 + L_4$		
	500pH	400pH	430pH	270pH	200pH
Measured Frequency	41.5	47.6	83	108	128
Simulation without Parasitics	44.4	50	89.3	125	150
Simulation with Calibre Extraction Tool	42.4	49.5	84.4	118	141
Simulation with S-Parameters	42.0	46.7	84.2	109	131
Simulation with Proposed Model	42.4	47.1	84.6	111	132

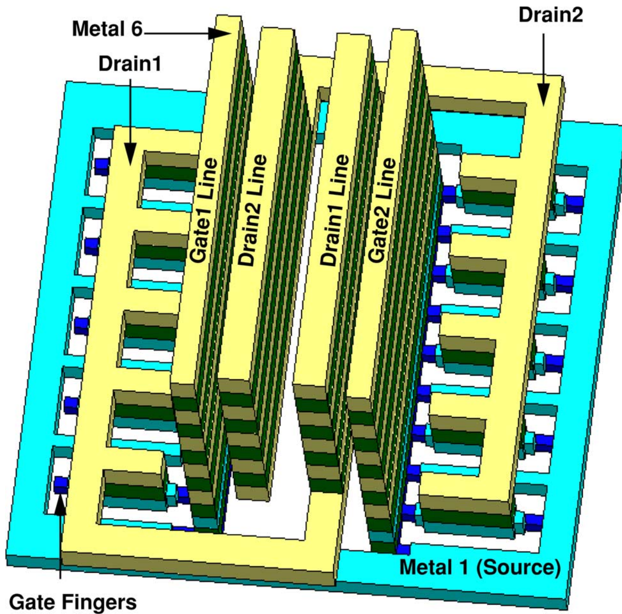

Fig. 8. 3D view of the proposed layout for a differential pair.

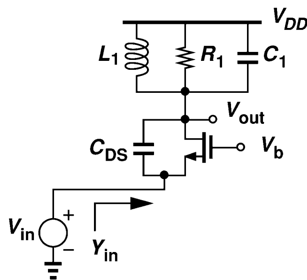

Fig. 9. The common-gate stage with drain-source capacitance.

The second layout technique relates to the effect of $C_{\rm DS}$ in common-gate and cascode stages. Consider the CG circuit shown in Fig. 9, where R_1 models the loss of L_1. As shown in Appendix B, the circuit resonates at $\omega_o = 1/\sqrt{L_1(C_1 + C_{\rm DS})}$, and at this frequency,

$$\mathrm{Re}\{\mathrm{Y_{in}}\} = g_m + g_{mb} \tag{12}$$

$$\mathrm{Im}\{\mathrm{Y_{in}}\} = -\omega C_{\rm DS}[1 - R_1(g_m + g_{mb})]. \tag{13}$$

That is, $C_{\rm DS}$ introduces a negative capacitance at the input equal to

$$C_{\rm eq} = C_{\rm DS}[1 - R_1(g_m + g_{mb})] \tag{14}$$

which is also evident from Miller's theorem. Partially canceling the effect of the input capacitance ($C_{\rm GS}, C_{\rm SB}$, and the pad capacitance), this property proves useful at very high frequencies. The key point here is that $C_{\rm DS}$ can be adjusted by simply stacking more or fewer metal levels on top of the source and drain junctions.

VI. EXPERIMENTAL RESULTS

Measurement and modeling of transistor capacitances, interconnects, and inductors become exceedingly difficult as the frequency exceeds a few tens of gigahertz. It is therefore beneficial to design *circuits* whose outputs can be readily measured and accurately correlated with the device models. Among various millimeter-wave circuits, oscillators prove an efficient modeling vehicle as their output frequency can be measured precisely with negligible errors due to the test environment, lack of calibration, or bandwidth limitations of the equipment.

Two different oscillator topologies with different transistor and inductor geometries have been employed in this work. Shown in Fig. 10(a), the first type incorporates a generic cross-

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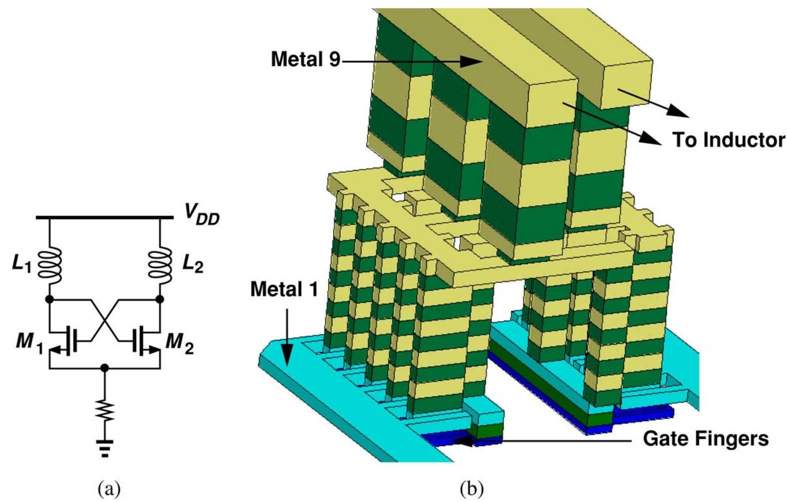

Fig. 10. (a) Cross-coupled oscillator, and (b) 3D view of core layout.

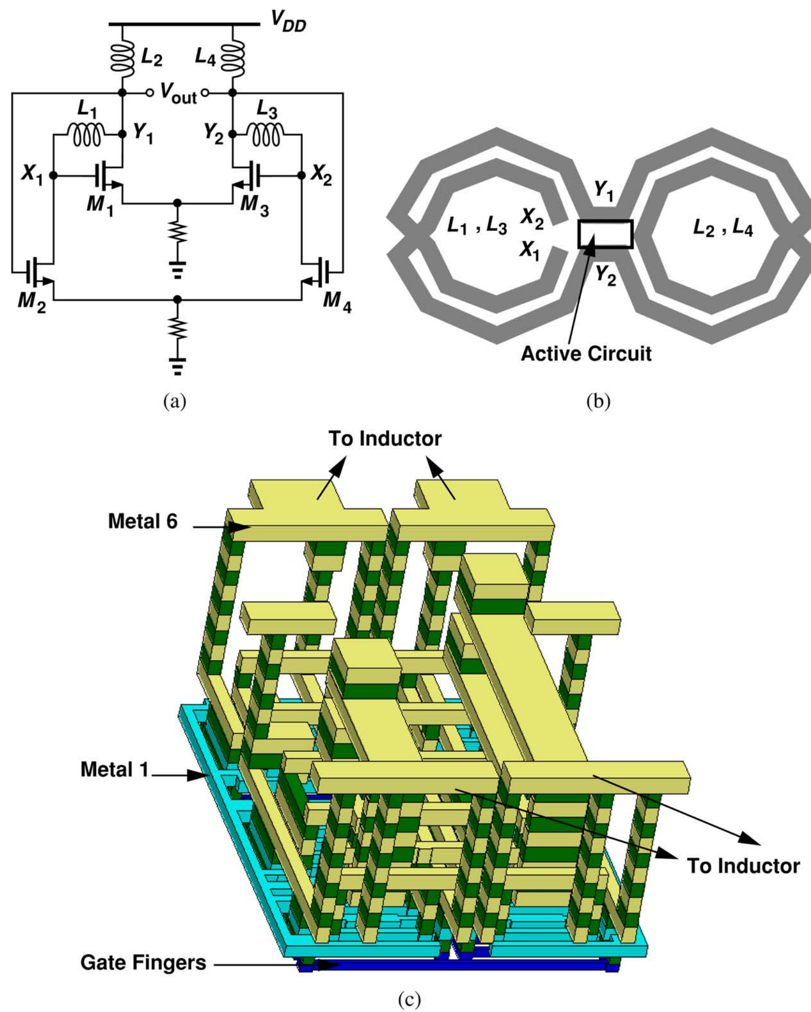

Fig. 11. (a) Oscillator reported in [11], (b) inductor arrangement for (a), and (c) 3D view of core layout.

coupled pair and a symmetric inductor. Two versions of this circuit are designed for operation at 42 GHz and 47 GHz, with $W_1 = W_2 = 10$ μm (1-μm fingers) and $L_1 + L_2 = 500$ pH and 400 pH. Fig. 10(b) depicts a three-dimensional view of the layout of the circuit's core, revealing various interconnects that travel over the transistors.

The second oscillator topology is shown in Fig. 11(a) and based on a new millimeter-wave circuit technique [11]. The

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four inductors are realized as illustrated in Fig. 11(b), thereby avoiding long interconnects among nodes X_1, Y_1, X_2, and Y_2. The limited area labeled "active circuit" in Fig. 11(b) must accommodate the core of the oscillator, leading to the complex geometry shown in Fig. 11(c), with interconnects overlapping the transistors and one another. If no lines were permitted to travel over the transistors, a much larger layout with longer interconnects would result. Three versions of this oscillator are designed for operation at 83 GHz, 108 GHz, and 128 GHz, with $W_1 - W_4 = 8$ μm (2-μm fingers) and $L_1 + L_3 = L_2 + L_4 =$ 430 pH, 270 pH, and 200 pH. The vastly different designs and layouts of the two oscillator types serve to test the robustness of the proposed modeling methodology.

The oscillators are fabricated in 90-nm CMOS technology and tested on a high-speed probe station. Fig. 12 shows the die photograph of the two types. The oscillation frequencies are measured using a spectrum analyzer and, for frequencies greater than 50 GHz, a harmonic mixer.

Table II summarizes the results of this study. The first row shows the frequencies measured on the fabricated prototypes, and the second row the simulated values in the absence of transistor metallization parasitics. Note the very large discrepancy as the frequency exceeds 100 GHz.

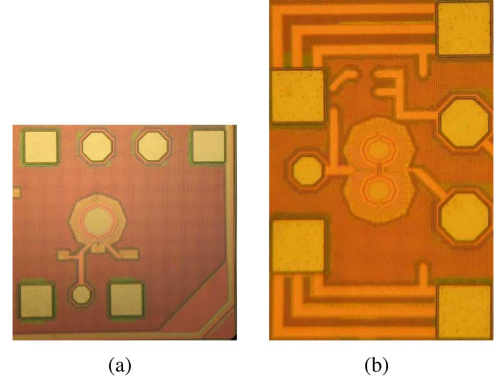
The third row displays the post-layout simulation results using the Calibre parasitic extraction tool. As mentioned in Section III, the frequency-independent nature of the extracted capacitances results in a larger error at higher frequencies. For example, the capacitances incur an error of 20% for the 128 GHz oscillator.

The fourth row shows the frequencies obtained if the inductors and the transistors are imported as a multi-port black box from HFSS into Cadence. This method accounts for all effects in the layout, including extrinsic capacitances and the distributed nature of the interconnects (but not the distributed gate resistance). However, it yields little intuition.

Finally, the fifth row summarizes the simulated values obtained with the physical model of the transistors [Fig. 3(b)] and the inductors [Fig. 6]. It is observed that the simulations and measurements differ by less than 3.2% for all prototypes. Since process variations account for a few percent of error in the frequency of LC oscillators, this level of agreement demonstrates the high accuracy of the proposed modeling methodology. It is also interesting to note that the BSIM4 logic model accurately represents the intrinsic capacitances of 90-nm technology for frequencies as high as 128 GHz.

VII. Conclusion

The modeling of devices and interconnects plays a critical role in mm-wave circuits' performance predictability. This paper has proposed a methodology based on electromagnetic and circuit simulations that allows modeling various effects while retaining physical insights into the parasitics. The approach also accommodates complex layout styles and lends itself to new layout techniques. The methodology has been applied to five CMOS oscillators in the range of 40 to 130 GHz, predicting oscillation frequencies with 3.2% error.



(a) (b)

Fig. 12. Die photographs of two oscillators.

Appendix A

Consider the four-port network shown in Fig. 13(a), where

$$I_1 = Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3 + Y_{14}V_4 \tag{15}$$

$$\vdots$$

$$I_4 = Y_{41}V_1 + Y_{42}V_2 + Y_{43}V_3 + Y_{44}V_4. \tag{16}$$

For differential excitations in Fig. 7(b), $V_1 = -V_3, V_2 = -V_4, I_1 = -I_3$, and $I_2 = -I_4$. Thus, (15) reduces to

$$I_1 = Y_{11}V_1 + Y_{12}V_2 - Y_{13}V_1 - Y_{14}V_2 \tag{17}$$

$$= (Y_{11} - Y_{13})V_1 + (Y_{12} - Y_{14})V_2. \tag{18}$$

Similarly,

$$I_2 = Y_{21}V_1 + Y_{22}V_2 - Y_{23}V_1 - Y_{24}V_2 \tag{19}$$

$$= (Y_{21} - Y_{23})V_1 + (Y_{22} - Y_{24})V_2. \tag{20}$$

In other words, for differential excitations, the four-port network can be decomposed into two independent two-port networks as shown in Fig. 13(b).

Appendix B

For the circuit of Fig. 9, it can be shown that, if channel-length modulation is neglected,

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{R_1 L_1 s(g_m + g_{mb} + C_{\text{DS}}s)}{R_1 L_1 (C_1 + C_{\text{DS}})s^2 + L_1 s + R_1}. \tag{21}$$

The denominator reaches a minimum at resonance:

$$\omega_o = \frac{1}{\sqrt{L_1(C_1 + C_{\text{DS}})}} \tag{22}$$

yielding

$$\frac{V_{\text{out}}}{V_{\text{in}}}(j\omega_o) = R_1(g_m + g_{mb} + j\omega_o C_{\text{DS}}) \approx R_1(g_m + g_{mb}). \tag{23}$$

because $g_m + g_{mb}$ $(= 1/50\ \Omega)$ is typically much greater than $\omega_o C_{\text{DS}}$.

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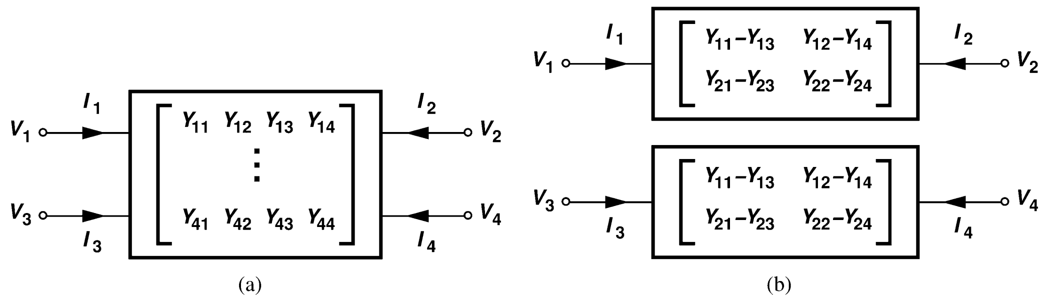

Fig. 13. (a) Y-parameters for four-port network in Fig. 7(b), and (b) the decomposition results.

The input admittance is given by

$$Y_{\rm in}(s) = \frac{(R_1L_1C_1s^2 + L_1s + R_1)(g_m + g_{mb} + C_{\rm DS}s)}{R_1L_1(C_1 + C_{\rm DS})s^2 + L_1s + R_1} \tag{24}$$

which, at $s \approx j\omega_o$, reduces to

$$Y_{\rm in}(j\omega) \approx (g_m + g_{mb}) - j\omega C_{\rm DS}[1 - R_1(g_m + g_{mb})]. \tag{25}$$

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