

# A 2-GHz CMOS Image-Reject Receiver With LMS Calibration

Lawrence Der, *Member, IEEE*, and Behzad Razavi, *Fellow, IEEE*

**Abstract**—This paper describes a sign–sign least-mean squares (LMS) technique to calibrate gain and phase errors in the signal path of a Weaver image-reject receiver. The calibration occurs at startup and the results are stored digitally, allowing continuous signal reception thereafter. Fabricated in a standard digital 0.25- $\mu\text{m}$  CMOS technology, the receiver achieves an image-rejection ratio of 57 dB after calibration, a noise figure of 5.2 dB, and a third-order input intercept point of  $-17$  dBm. The circuit consumes 55 mW in calibration mode and 50 mW in normal receiver mode from a 2.5-V power supply. The prototype occupies an area of  $1.23 \times 1.84$  mm<sup>2</sup>.

**Index Terms**—Digital-to-analog conversion, image rejection, least mean square (LMS) calibration, low-noise amplifier, mixer, radio frequency (RF) CMOS, variable-delay circuit.

## I. INTRODUCTION

THE TRADEOFF between image rejection and channel selection in heterodyne radio-frequency (RF) receivers poses many difficulties in both the choice of the system's frequency planning and the design of the building blocks. Various alternatives such as direct conversion, image-reject mixing, and heterodyning with low intermediate frequency (IF) have been introduced so as to relax the above tradeoff, but at the cost of degrading other receiver properties. It is, therefore, desirable to develop techniques that improve the image rejection without compromising other performance parameters.

This paper presents a calibration technique that improves the image-rejection ratio (IRR) of RF receivers through the use of the least mean square (LMS) algorithm. Applicable to various receiver architectures, the method is realized in a Weaver image-reject topology [1], achieving an IRR of 57 dB. The calibration occurs at the startup and does not degrade the noise, linearity, or gain of the receiver. Fabricated in a 0.25- $\mu\text{m}$  digital CMOS technology, the prototype targets a sensitivity and blocking performance commensurate with 2-GHz wideband code division multiple access (WCDMA) systems.

Section II briefly reviews image rejection issues. Section III presents the receiver architecture and the application of the LMS algorithm. Section IV describes the design of the building blocks, and Section V summarizes the experimental results.

## II. ARCHITECTURE ISSUES

Fig. 1 shows the Hartley [2] and Weaver image-reject receivers. The IRR is limited by mismatches between the local

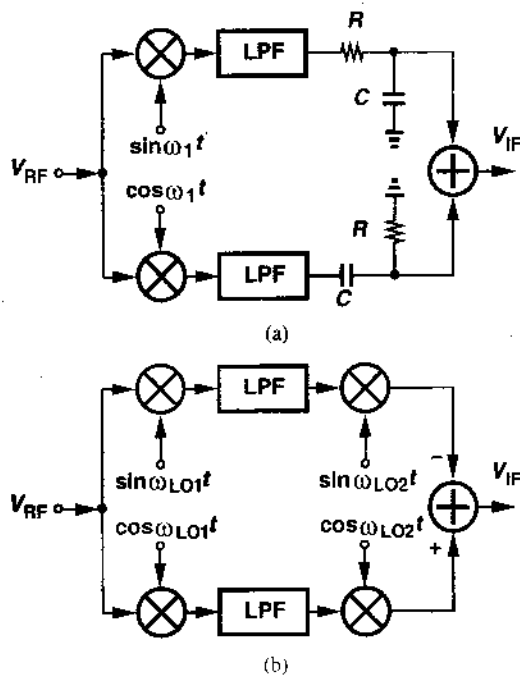


Fig. 1. (a) Hartley and (b) Weaver image-reject architectures.

oscillator (LO) phases and between the upper and lower signal paths. It can be shown that [3]

$$\text{IRR} \approx \frac{(\frac{\Delta A}{A})^2 + \theta^2}{4} \quad (1)$$

where  $\Delta A/A$  denotes the relative gain mismatch and  $\theta$  (in radians) represents the total phase mismatch. For example, an IRR of 60 dB translates to  $\Delta A/A = 0.1\%$  and  $\theta = 0.1^\circ$ , revealing very stringent matching requirements. In practice, static and, more importantly, dynamic mismatches limit IRR to 25–40 dB.

It is important to note that the above observations equally apply to polyphase filters. Despite their high power dissipation, receivers employing polyphase networks for image rejection have achieved IRRs of at most 40 dB at radio frequencies [4]–[6]. The receiver in [5] achieves an IRR of 35 dB at 2.4 GHz and 60 dB at an IF of 190 MHz. Considering that 1) a phase mismatch of  $2^\circ$  yields an IRR of 35 dB and 2) device capacitances and, hence, their mismatches become quite significant at gigahertz frequencies, we note that attempts to achieve adequate matching by layout techniques and the use of large devices may not succeed.

In order to appreciate the difficulty in obtaining a high IRR, let us consider an active implementation of the first quadrature mixer in Hartley and Weaver receivers. Shown in Fig. 2,

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The authors are with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095-1594 USA (e-mail: razavi@icsl.ucla.edu).  
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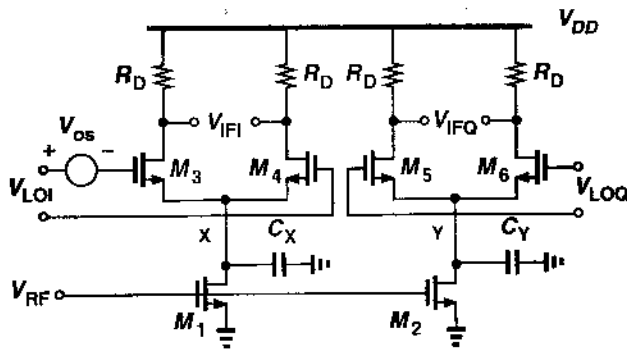


Fig. 2. Effect of threshold mismatch on IRR.

such a circuit suffers from phase and gain mismatch in the presence of MOS threshold voltage mismatches. Specifically, if the switching pair  $M_3$ – $M_4$  exhibits a mismatch of  $V_{th}$ , then the asymmetry introduces a voltage component at the LO frequency at node  $X$ . The resulting displacement current in  $C_X$  then changes the effective phase of the LO, yielding phase and gain error at the IF. Simulations indicate that a 20-mV mismatch degrades the IRR by more than 10 dB.

In addition to polyphase filters, other methods of image rejection have been reported. An analog calibration technique to correct for gain and phase mismatches independently has been implemented successfully in [7], but mandates periodic refreshing, a difficult issue for CDMA systems that must receive continuously. A digital signal processing (DSP) calibration approach has been reported in [8], but it requires substantial computational power. The receiver in [9] uses manual adjustment to achieve a high rejection.

In this paper, the Weaver architecture is chosen over the Hartley topology because the latter 1) requires a tight control on the absolute values of the resistors and capacitors (a 20% change in  $RC$  gives  $IRR = 20$  dB), and 2) does not easily lend itself to independent gain and phase calibration.

### III. RECEIVER ARCHITECTURE

Fig. 3 shows the architecture in simplified form, illustrating independent gain and phase calibration. An LMS adaptation circuit adjusts the phase and gain of the second downconversion stage without disturbing the RF mixers or the first LO. In the calibration mode, an image tone is applied at the RF input,  $y(t)$  is measured, and the coefficients  $w_1$  and  $w_2$  are updated in discrete steps until  $y(t)$  approaches zero.

Unlike single-variable negative feedback systems, where a large loop gain is typically sufficient to force the error to zero, the architecture of Fig. 3 must simultaneously adjust the phase and gain so as to arrive at the global minimum for the error. A method of multivariable feedback is the LMS update algorithm, given by [10]

$$w_{1,2}[(m+1)T] = w_{1,2}[mT] + 2\mu\epsilon[mT]x_{1,2}[mT] \quad (2)$$

where  $w_{1,2}[(m+1)T]$  denotes the values of  $w_1$  and  $w_2$  at discrete-time point  $(m+1)T$ ,  $\mu$  is the step size,  $\epsilon[mT]$  is the error, and  $x_{1,2}[mT]$  represents the values of two input "regressors,"

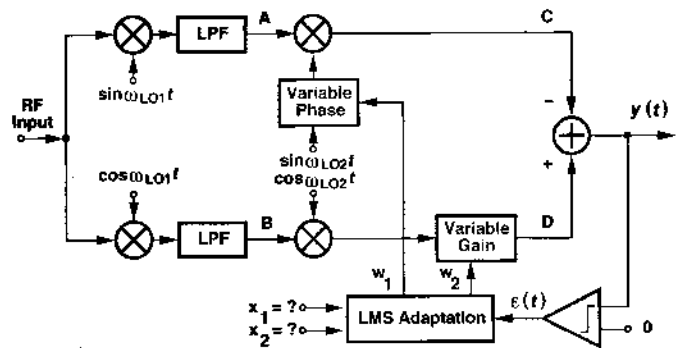


Fig. 3. Simplified receiver architecture.

i.e., two inputs with which the error must be correlated to determine the change in the coefficients.

The principal difficulty in applying the LMS algorithm to the Weaver architecture is that the input regressors  $x_1$  and  $x_2$  are not directly available. To determine how  $x_1$  and  $x_2$  must be generated, we return to the general LMS algorithm [10] and, as outlined in the Appendix, prove that  $x_1(t) \approx A(t) \cos(\omega_{LO2}t)$  and  $x_2(t) \approx B(t) \cos(\omega_{LO2}t)$  where  $A(t)$  and  $B(t)$  denote the signals at nodes  $A$  and  $B$  in Fig. 3, respectively. The gain and phase coefficients are then expressed as

$$w_1[(m+1)T] \approx w_1[mT] - 2\mu\epsilon[mT]A[mT] \cos(\omega_{LO2}[mT]) \quad (3)$$

$$w_2[(m+1)T] = w_2[mT] + 2\mu\epsilon[mT]B[mT] \cos(\omega_{LO2}[mT]) \quad (4)$$

The adaptive algorithms suggested by (3) and (4) require analog or digital multipliers, leading to high complexity. For this reason, a sign–sign (SS) LMS approach is chosen [10] whereby only the signs of the error and the input regressors are multiplied. The complicated digital multipliers are, therefore, replaced by simple exclusive OR gates.

The above observations lead to the receiver architecture shown in Fig. 4, where the blocks denoted by  $\Delta$  are variable-delay stages used to adjust the phase of the second LO. We make the following observations. First, two additional mixers,  $MX_1$  and  $MX_2$ , multiply the signals at points  $A$  and  $B$  by one phase of  $LO_2$ , thereby generating the required input regressors  $x_1(t)$  and  $x_2(t)$  is needed for the SS-LMS algorithm. It is important to note that the noise, nonlinearity, and mismatches of  $MX_1$  and  $MX_2$  are unimportant because 1) they do not appear in the signal path and 2) only the polarity of the input regressors  $x_1(t)$  and  $x_2(t)$  are needed for the SS-LMS algorithm; this allows each to be designed with a minimal power dissipation penalty (2.5 mW each). Second, three variable-delay stages ( $\Delta_1$ ,  $\Delta_2$ , and  $\Delta_3$ ) are used in this receiver. Delay stage  $\Delta_3$  duplicates the role of  $\Delta_2$  such that delay stages  $\Delta_1$  and  $\Delta_2$  see the same load, thereby avoiding systematic errors. Furthermore, since the delay lines only control the phases of  $LO_2$ , whose frequency is about 1/10 of  $LO_1$ , they operate at a low frequency and can be designed for negligible phase noise (Section IV-C). Third, the receiver is designed to be fully differential, except for the single-ended low-noise amplifier (LNA) and RF mixers. Differential signaling minimizes the effect of supply and

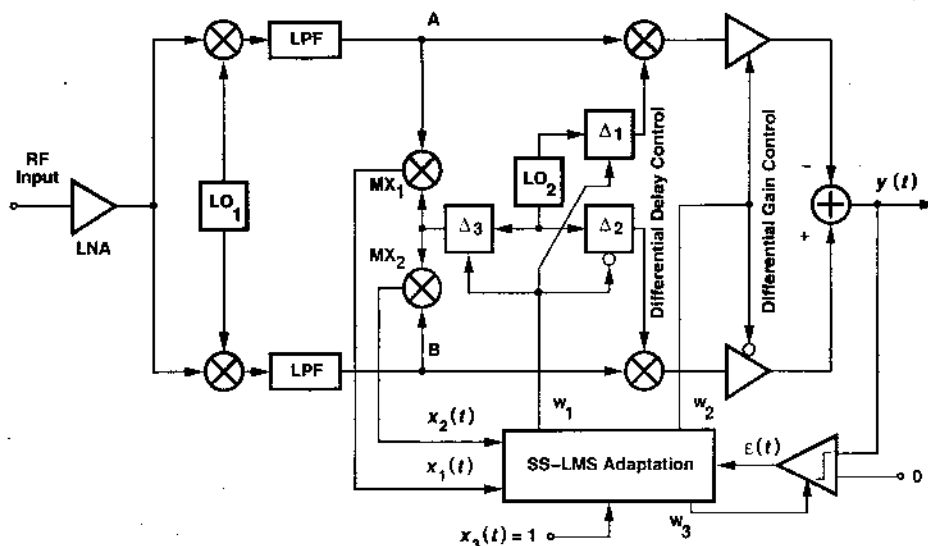


Fig. 4. Overall receiver architecture.

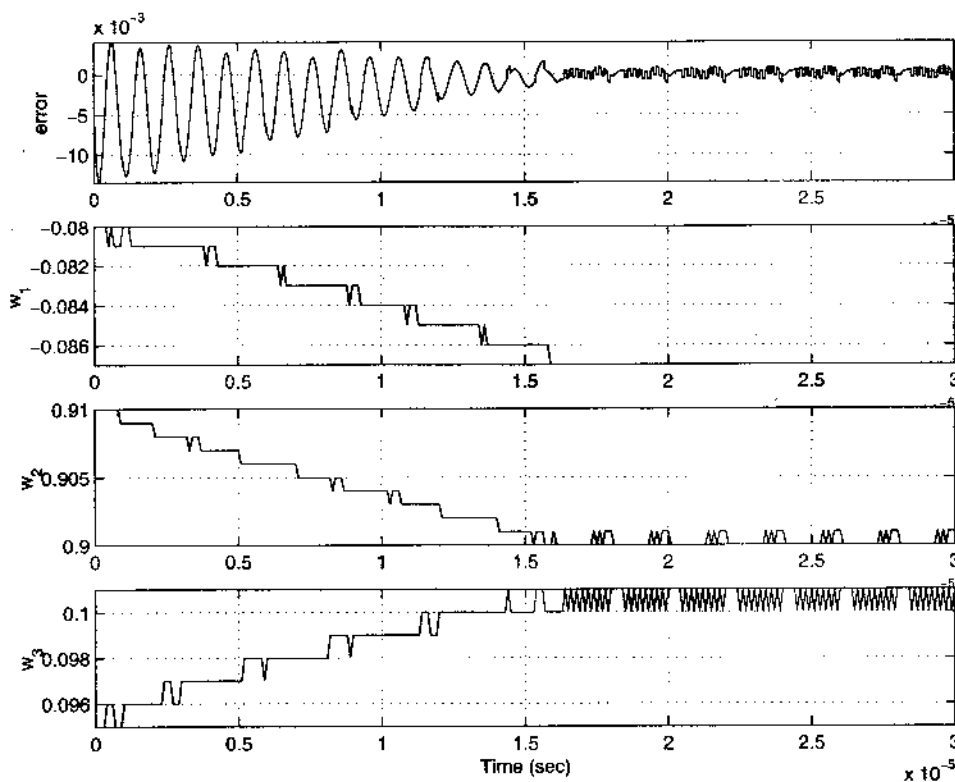


Fig. 5. Behavioral simulation of the LMS calibration.

common-mode noise.<sup>1</sup> Moreover, the phase and gain mismatch are controlled differentially to avoid systematic errors. The bubbles on the diagram represent differential control.

The SS-LMS machine lends itself to a compact mixed-signal implementation. Circuits in this block only operate at speeds near  $2f_{max}$ , where  $f_{max}$  is the maximum frequency of the down-converted image tone. Since most of the circuits in this block are not used in normal receiver mode, they can be turned off after calibration. Furthermore, digital CMOS implementation of the

<sup>1</sup>Mismatches in the differential circuits will lead to an increase in common-mode sensitivity but the SS-LMS feedback loop will minimize the overall error signal.

control circuits enables digital storage of the coefficients with zero standby current.

The accuracy of calibration is limited by the offset voltage of the comparator in Fig. 4. Fortunately, the LMS algorithm allows offset cancellation by adding a third coefficient with an input regressor  $x_{DC} = 1$  [11], [12]. This coefficient adds or subtracts a differential current in the input stage of the comparator.

Fig. 5 shows the calibration behavior of the receiver as predicted by Simulink. The LMS block adjusts the coefficients until the error approaches zero. In the steady state, the coefficients toggle by 1 least significant bit (LSB) and the error fluctuates between small positive and negative values.

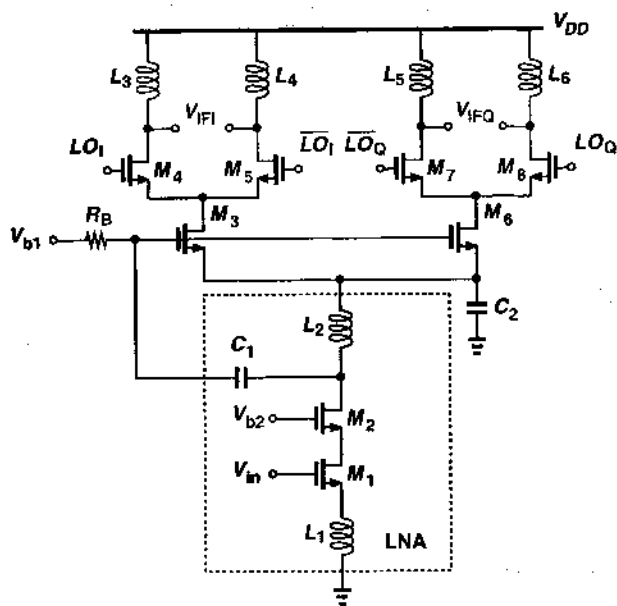


Fig. 6. Simplified schematic of the LNA and RF mixers.

In order to demonstrate the feasibility of the proposed image rejection technique, a CMOS receiver has been designed. Operating in the WCDMA band of 2.11–2.17 GHz, the receiver downconverts the input frequency to an IF of 200 MHz and then to baseband with  $f_{LO1} = 1.91$ – $1.94$  GHz and  $f_{LO2} = 200$  MHz. The image band therefore spans 1.71–1.77 GHz. Since the emphasis is on improving image rejection, other aspects of the design are optimized to a lesser extent.

With the above frequency plan, the 1.8-GHz image tone necessary for calibration can be readily generated through multiplication of  $f_{LO2}$  by 9.<sup>2</sup> Since the phase noise of the calibration is not critical, a compact phase-locked loop could perform this multiplication (and be turned off afterwards).

#### IV. BUILDING BLOCKS

##### A. LNA and RF Mixers

Fig. 6 shows a simplified diagram of the LNA and RF mixers. A cascode LNA topology using inductive degeneration is followed by single-balanced active mixers with inductive loads. The combined circuit employs a current reuse technique similar to that in [13] except that two quadrature mixers are stacked on top of the LNA. Since the RF mixers require a large current to exhibit a high IP3, this technique allows the LNA to exploit the sum of the mixer bias currents, thus achieving a low noise figure.

It is important to note that the above stacking technique is feasible because the IF loads are inductive rather than resistive. With resistive loads, the limited voltage headroom would yield conversion loss in the mixers. The total headroom consumed by  $M_1$ ,  $M_2$ , and  $M_3$  ( $M_6$ ) is equal to 800 mV. Thus, large voltage excursions at the drains of  $M_3$  and  $M_6$  and, hence, large LO swings can be accommodated.

The use of four inductive loads for an IF of 200 MHz does pose an area problem. For the RF mixers to provide adequate

<sup>2</sup>Since the actual image lies around 1.74 GHz, this choice may not lead to optimum image rejection.

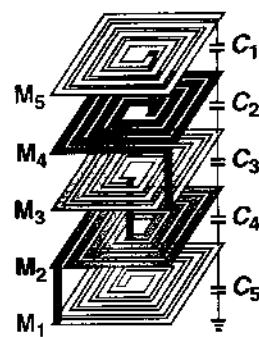


Fig. 7. Inductor structure.

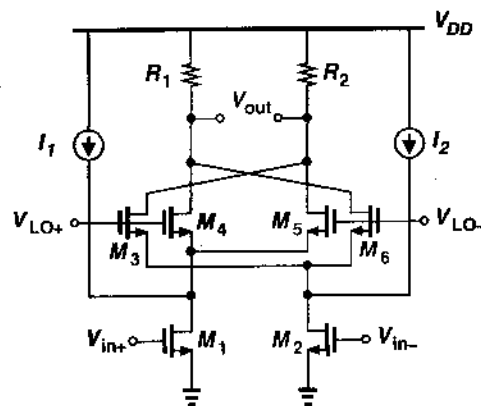


Fig. 8. Simplified diagram of the IF mixer.

conversion gain (e.g., 10–15 dB), the load impedance must fall in the range of 500–1000  $\Omega$ , in turn demanding inductance values of 100–200 nH. Fig. 7 shows the stacked spirals used here so as to achieve a 20-fold increase in the equivalent inductance [14]. In principle, the inductance should increase by a factor of 25, but due to lack of mutual inductance between orthogonal edges, the effective value falls to 20 [14]. The structure exhibits a total inductance of 260 nH and a self-resonance frequency 470 MHz. The quality factor  $Q$  is approximately equal to 3. The outputs of the circuit are capacitively coupled to the subsequent IF mixers.

Simulations of the LNA/mixer combination with a  $\gamma$  of 3 (in  $I_D^2 = 4kT\gamma g_m \Delta f$ ) indicate a noise figure of 4.35 dB, a voltage gain of 35 dB, and IIP3 of -13 dBm with a supply current of 4.5 mA.

##### B. IF Mixers and Gain Control Circuit

With 35 dB of voltage gain in the LNA and the RF mixers, the IF mixers must provide a high IP3, nearly +20 dBm. Fig. 8 depicts the IF mixer implementation. In order to achieve both a high IP3 and adequate voltage gain, the circuit must allow a high overdrive voltage for the input devices,  $M_1$ – $M_2$ , and a large voltage drop across  $R_1$  and  $R_2$ , thus facing severe headroom constraints. This issue is resolved by adding current sources  $I_1$  and  $I_2$ , each of which carries about 80% of the bias current of the input transistors. Consequently,  $R_1$  and  $R_2$  can be increased by a factor of four. Note that  $I_1$  and  $I_2$  contribute minimal noise because their overdrive voltage is four times that of  $M_1$  and  $M_2$ .

Current sources  $I_1$  and  $I_2$  offer another important benefit. Since  $M_3$ – $M_6$  carry less current, they are on simultaneously for

Fig. 9. (a) Ga

smaller  $\gamma$   
The gain  
version stage  
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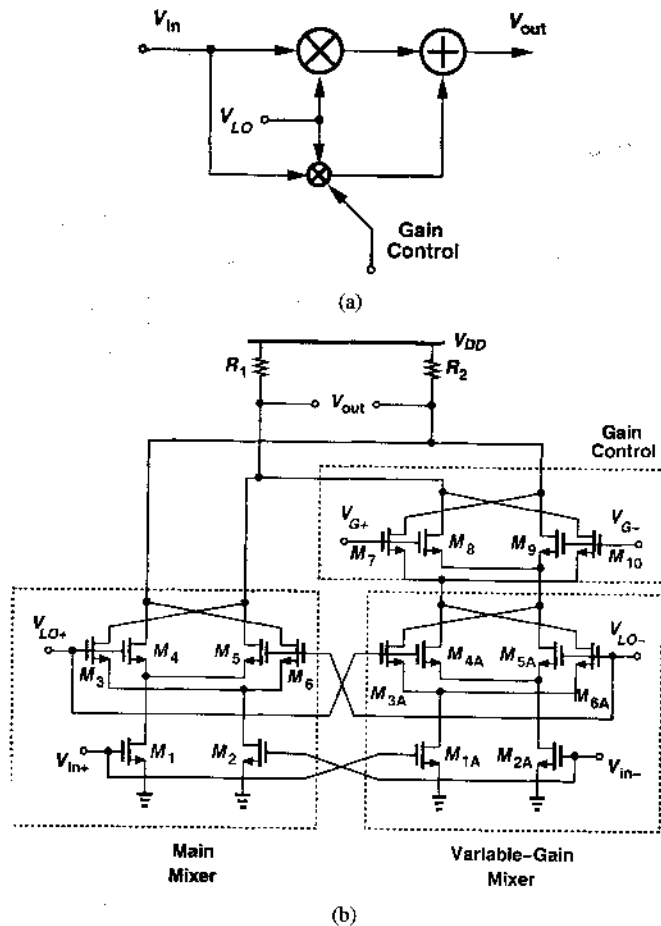


Fig. 9. (a) Gain control concept. (b) Implementation.

a smaller fraction of the LO period, thus, injecting less noise to the output.

The gain control and phase control in the second downconversion stage must be realized such that one does not affect the other as such an interaction may prohibit convergence in the LMS loop. For this reason, the gain control adjusts only a fraction of the gain of the second downconversion mixers. Fig. 9(a) illustrates the gain control concept. The input signal is applied to two mixers operating in parallel. The (larger) main mixer downconverts the input with a constant gain while the smaller mixer provides a variable gain. The outputs of these two mixers are then added to form the desired IF output. Since only a fraction of the gain is varied and since the gain variation occurs at low frequencies, the signal phase remains unaffected. Note that the two mixers exhibit equal phase shifts because one is a scaled replica of the other.

Fig. 9(b) shows the transistor-level realization, omitting the current sources ( $I_1$  and  $I_2$  in Fig. 8) for clarity. The mixer is decomposed into a main path and a variable-gain path, with the latter scaled down in both device size and bias current by a factor of 5. The gain-control circuit consisting of  $M_7$ – $M_{10}$  can add, subtract, or null signal currents from the variable-gain mixer depending on the differential gain-control voltage ( $\Delta V_G = V_{G+} - V_{G-}$ ). The outputs of the two IF mixers used in the quadrature paths of the Weaver receiver are added in the current domain and share the load resistors  $R_1$  and  $R_2$  (each equal to 1 k $\Omega$ ).

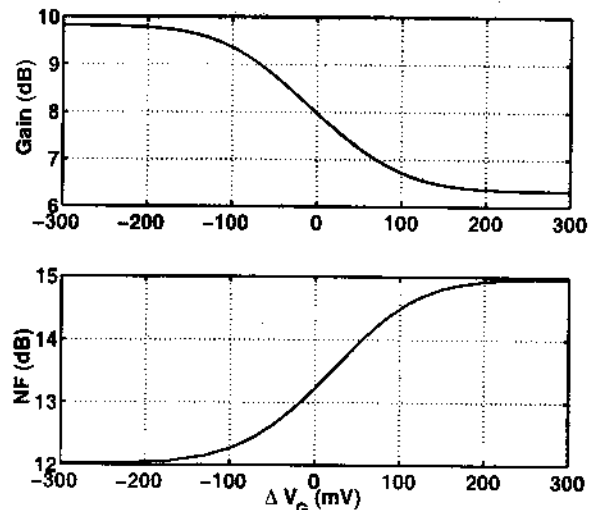


Fig. 10. Simulated gain and noise figure (NF) of IF mixer as a function of  $\Delta V_G$ .

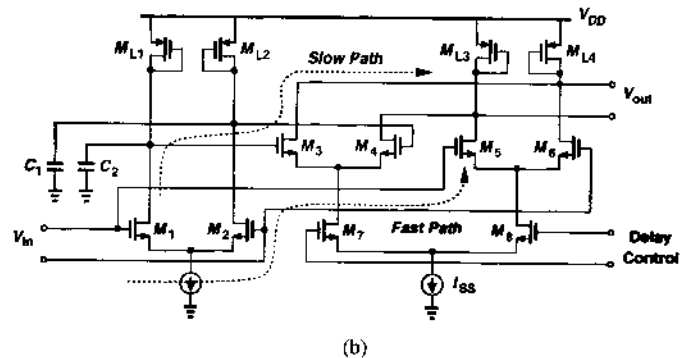
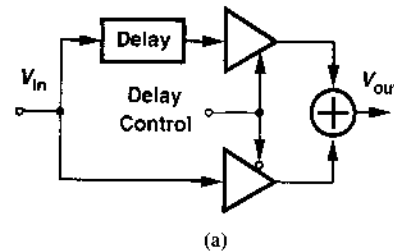


Fig. 11. Variable-delay circuit. (a) Conceptual. (b) Schematic.

Fig. 10 plots the simulated gain and noise figure of the circuit as a function of the differential control voltage  $\Delta V_G$ . The circuit exhibits a slope of about 0.0143 dB/mV with a total gain variation of approximately  $\pm 1.5$  dB around a nominal value of 8 dB.

C. Variable-Delay Circuit

A simple and practical approach to phase adjustments of the second LO is to utilize a variable-delay cell. Illustrated in Fig. 11, the circuit is realized by interpolating between the phases of a fast signal path  $M_5$ – $M_6$  and a slow signal path ( $M_1$ – $M_2$  and  $M_3$ – $M_4$ ). Phase control is achieved by steering  $I_{SS}$  between the differential pairs  $M_3$ – $M_4$  and  $M_5$ – $M_6$ , making the output phase a weighted sum of the phase delays in the two paths.<sup>3</sup> Addition of two MOS capacitors  $C_1$  and  $C_2$

<sup>3</sup>Note that complete switching of  $I_{SS}$  makes  $V_{out}$  independent of the interpolated phases.

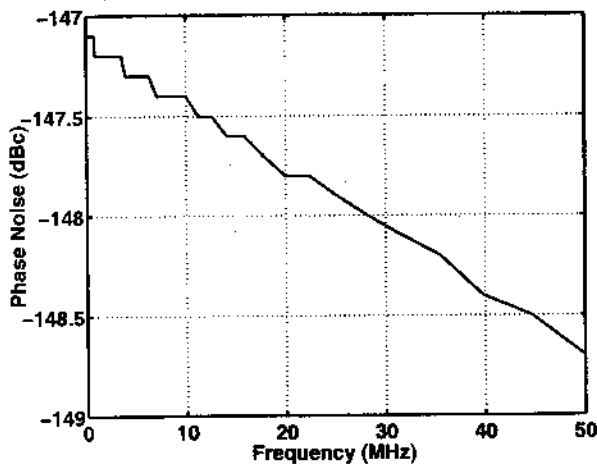


Fig. 12. Simulated phase noise of the variable-delay circuit.

yields  $\pm 25^\circ$  of phase adjustment (for a 200-MHz LO input). Such a wide range is chosen to accommodate large phase mismatches in the RF and LO paths. Also, the wide phase range obviates the need for accurate generation of quadrature phases for  $LO_1$  and  $LO_2$ .

Since the variable-delay lines operate on the phases of only  $LO_2$ , they introduce negligible phase noise. Fig. 12 plots the simulated phase noise of the variable-delay circuit for a 200-MHz sine wave input. The phase noise is very low and relatively flat over an offset frequency range of 0–50 MHz.

#### D. Sign–Sign LMS Adaptation Circuit

The SS-LMS machine lends itself to a compact mixed-signal implementation as shown in Fig. 13. The circuit consists of three comparators, two XOR gates, three up/down counters, three digital-to-analog converters (DACs), and other combinational logic omitted for simplicity. The gain, phase, and offset coefficients,  $w_1$ – $w_3$ , are updated according to the results of  $x_1 \oplus c$ ,  $x_2 \oplus \epsilon$ , and  $\epsilon$ , respectively. The updated signals are subsequently applied to up/down counters that form the inherent discrete-time integration of the SS-LMS algorithm. The output of each counter is subsequently converted to analog and applied to the receiver gain, phase, and offset circuits.

In order to achieve high calibration accuracy, each DAC has a resolution of 11 bits, providing a gain step of 0.0017 dB, a phase step of  $0.0244^\circ$ , and an offset step of  $48.8 \mu\text{V}$ . The up/down counters are 14 bits wide, providing the eleven most significant bits (MSBs) to the DAC and the three LSBs for “masking.” Masking the three LSBs minimizes the coefficient ripple after the system converges [12].

#### E. DAC

In this design, the DACs must provide 11-bit monotonicity [differential nonlinearity (DNL)] with low complexity. Since the speed and integral nonlinearity (INL) of the DACs are not critical,<sup>4</sup> a compact low-power implementation is possible. As shown in Fig. 14, the binary input is decomposed and converted into a 5-bit coarse 1-of- $n$  code and a 6-bit fine 1-of- $n$  code.

<sup>4</sup>Even if accumulation of DNL yields a large INL, the small coefficient steps guaranteed by 11-bit monotonicity minimize the overall error.

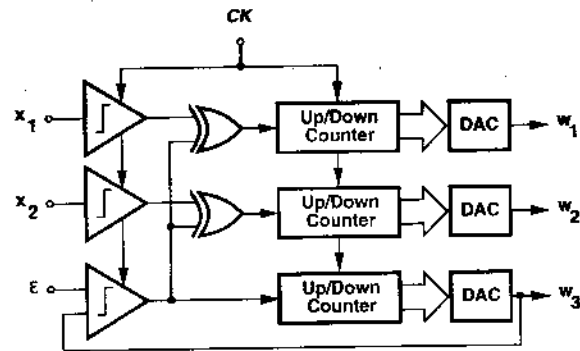


Fig. 13. Implementation of the SS-LMS adaptation circuit.

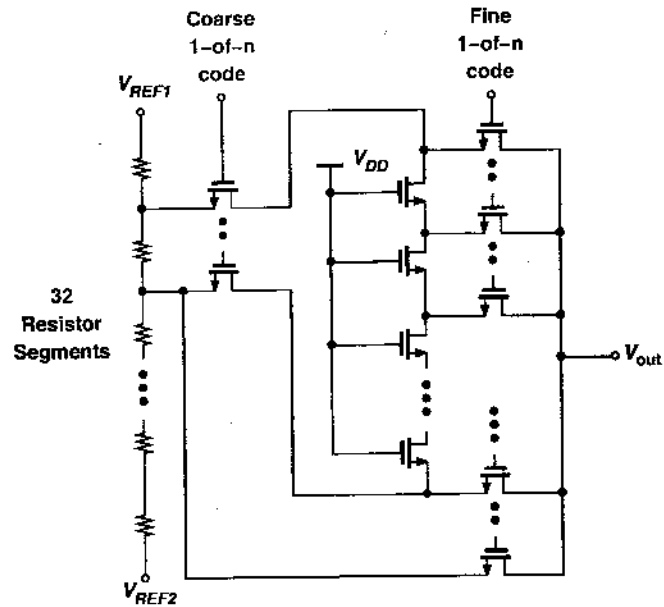


Fig. 14. One slice of the DAC.

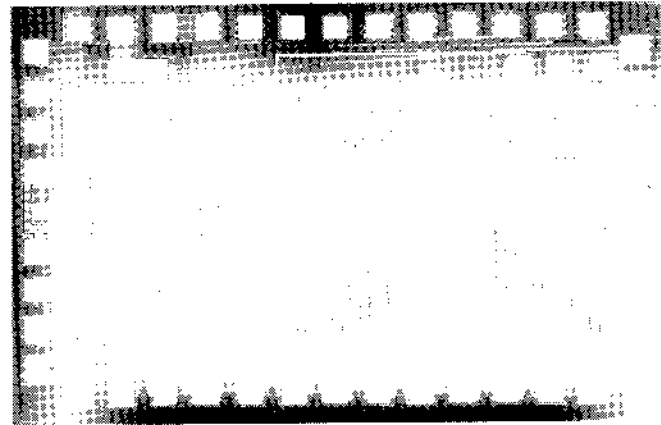
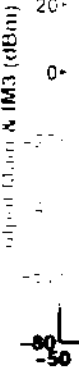


Fig. 15. Die photo of the prototype.

The former selects two consecutive tap voltages of the resistor ladder, whose difference is then subdivided by a string of 32 MOSFETs operating in the triode region. The fine code subsequently selects one of the subdivided values, generating the proper output.

A key property of the above DAC topology is its guaranteed monotonicity for arbitrarily high resolutions, a critical aspect for use in feedback systems. This benefit accrues because the



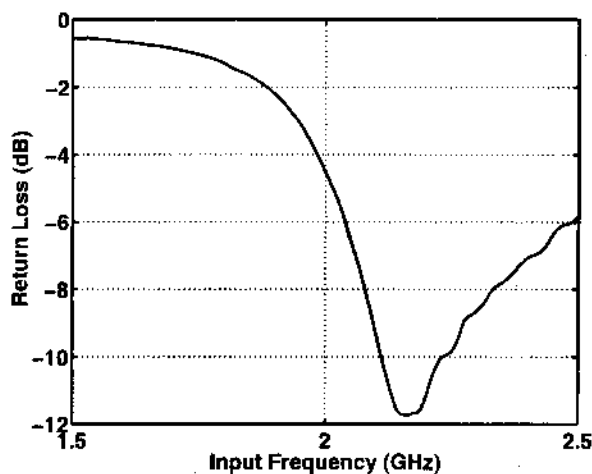


Fig. 16. Measured input return loss.

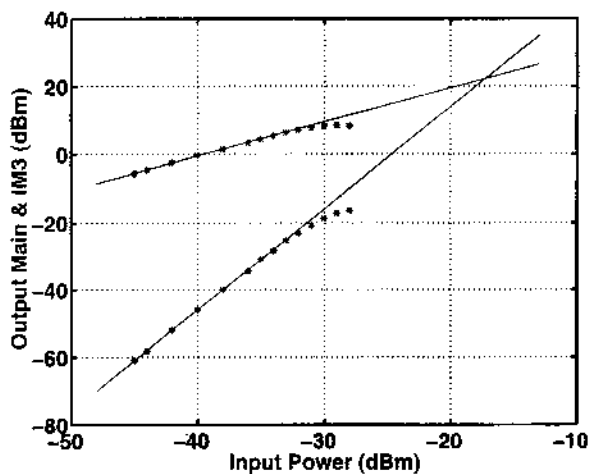


Fig. 17. Measured IIP3 of the receiver.

differential nonlinearity is constrained to less than 1 LSB for arbitrary device mismatches.

V. EXPERIMENTAL RESULTS

The receiver along with the LMS calibration has been designed and fabricated in a digital 0.25- $\mu$ m CMOS technology. Fig. 15 shows a photograph of the die, which occupies an area of  $1.23 \times 1.84$  mm. The circuit has been tested with a 2.5-V supply.

The measured input return loss of the receiver is plotted in Fig. 16, indicating a value of -11 dB across the WCDMA band (2.11–2.17 GHz). The measured noise figure and voltage gain are 5.2 and 41 dB, respectively.

The third-order nonlinearity of the receiver is measured by applying two equal power tones at frequencies 2.144 and 2.145 GHz. As shown in Fig. 17, the IIP3 is extrapolated to be -17 dBm. The -1-dB compression point is measured to be -30 dBm. The blocking performance is characterized by applying both a desired signal at -100 dBm and a blocker and raising the blocker level until the desired signal at the output drops by 3 dB. The tolerable blocking level is measured to be -33 dBm. These measurements indicate the linearity of the

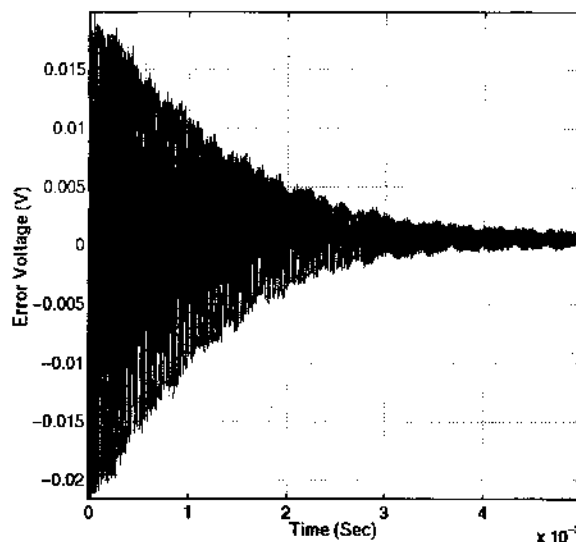


Fig. 18. Measured transient response of the SS-LMS algorithm.

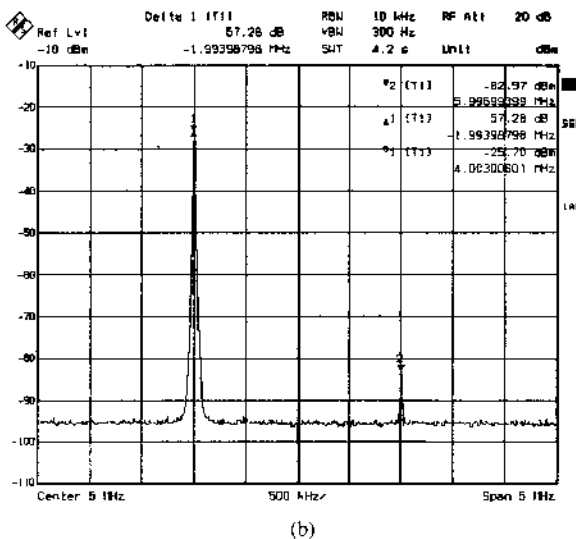
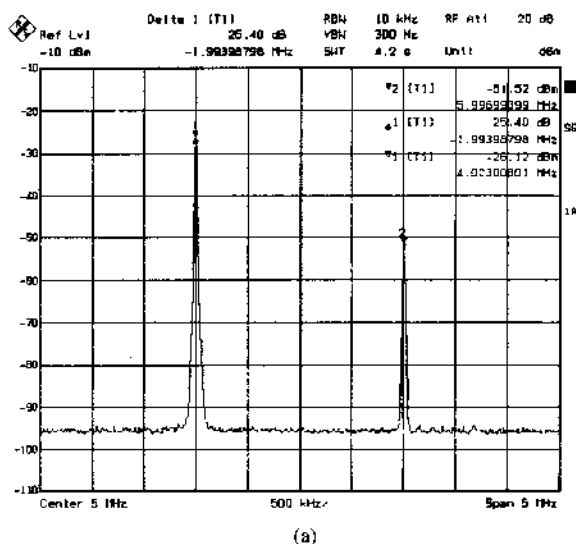


Fig. 19. Output spectrum (a) before calibration and (b) after calibration.

receiver is still limited by that of the second downconversion mixers.

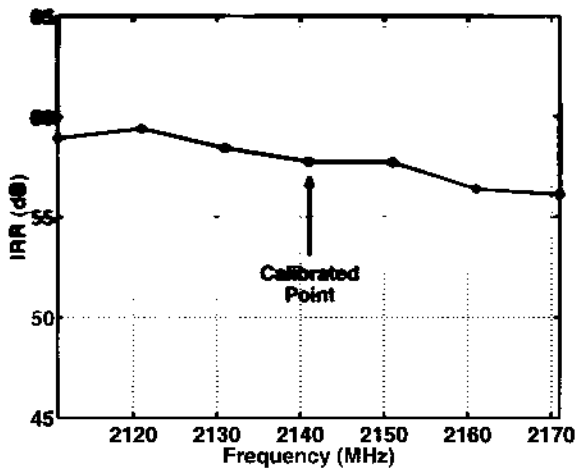


Fig. 20. Measured IRR versus input frequency.

TABLE I  
MEASUREMENT PERFORMANCE

Parameter	Measurement Results
NF	5.2 dB
IIP3	-17 dBm
Voltage Gain	41 dB
IRR	57 dB
$S_{11}$	-11 dB
$P_{DC}$ (rcv)	50 mW
$P_{DC}$ (cal)	55 mW
$V_{DD}$	2.5 V
Die Array	1.23 mm X 1.84 mm
Technology	0.25 $\mu$ m CMOS

Large mismatches in the setup limit the image-rejection ratio to 25 dB before calibration. Fig. 18 shows the measured convergence of the LMS machine during calibration with the image signal downconverted to 1 MHz and a clock rate of 5 MHz. After calibration is complete, the image rejection is measured by applying a desired tone and an image tone of equal power and measuring the difference between their amplitudes as they appear in the baseband. With  $f_{LO1} = 1.94$  GHz and  $f_{LO2} = 205$  MHz, such components fall at 4 and 6 MHz, respectively. As shown in Fig. 19, the SS-LMS calibration improves the IRR from 25 to 57 dB.

After calibration, the IRR is measured across the WCDMA frequency range by maintaining a constant baseband frequency. Fig. 20 plots the IRR, indicating only 1 dB of degradation as the input frequency deviates from the calibration point. The circuit consumes 55 mW during calibration mode and 50 mW during normal reception. Table I summarizes the measured performance.

## VI. CONCLUSION

A sign-sign LMS calibration technique has been introduced that substantially improves the image-rejection of a Weaver receiver without compromising the noise, linearity, or gain of the

receiver at the expense of a small increase in power dissipation. The Weaver architecture was chosen because it offers wideband image-rejection capability and low noise while lending itself to implementation in a standard digital CMOS process. LMS calibration techniques have been developed to adjust the gain and phase mismatches only in the IF and baseband sections of the receiver, with minimum impact on the overall receiver performance. Finally, mixed-signal implementation of the SS-LMS algorithm reduces power consumption and allows digital storage of the coefficients.

## APPENDIX

Fig. 3 shows the simplified architecture, illustrating gain and phase calibration. A common equation for the LMS coefficient algorithm [10] is, in vector notation

$$\mathbf{w}[(m+1)T] = \mathbf{w}[mT] + 2\mu\epsilon[mT]\mathbf{x}[mT] \quad (5)$$

where  $\mathbf{w}[(m+1)T]$  are the coefficient vectors at discrete-time point  $(m+1)T$ ,  $\mu$  is the step size,  $\epsilon[mT]$  is the error, and  $\mathbf{x}[mT]$  are the input regressor vectors. The principal difficulty in applying this equation to the Weaver architecture is that the input regressors,  $x_1$  and  $x_2$ , are not directly available. To determine how  $x_1$  and  $x_2$  must be generated, we return to the general LMS algorithm [10] and show that  $x_1(t) \approx A(t)\cos(\omega_{LO2}t)$  and  $x_2(t) \approx B(t)\cos(\omega_{LO2}t)$ , where  $A(t)$  and  $B(t)$  denote the signals at nodes A and B in Fig. 3, respectively.

From [10], the LMS algorithm is based on the iterative method of steepest descent where the updated value of the coefficient vector  $\mathbf{w}[(m+1)T]$  is equal to the current value of the coefficient vector  $\mathbf{w}[mT]$  plus a change proportional to the negative gradient  $\nabla[mT]$ .

$$\mathbf{w}[(m+1)T] = \mathbf{w}[mT] - \mu\nabla[mT]. \quad (6)$$

The key result of the LMS algorithm is that it approximates the gradient  $\nabla$  by taking the partial derivatives of  $\epsilon^2$  with respect to the coefficient vector rather than taking the partial derivatives of the expectation of  $\epsilon^2$  with respect to the coefficient vector, as follows:

$$\nabla \approx 2\epsilon(t) \frac{\partial \epsilon(t)}{\partial \mathbf{w}}. \quad (7)$$

Comparing (5)–(7), we find that the input regressor vector  $\mathbf{x}[mT]$  is equal to the samples of  $\partial \epsilon(t)/\partial \mathbf{w}$ . Substituting (7) into (6), we obtain the following general form for the LMS coefficient update equation:

$$\mathbf{w}[(m+1)T] = \mathbf{w}[mT] - 2\mu\epsilon(t) \left. \frac{\partial \epsilon(t)}{\partial \mathbf{w}} \right|_{t=mT}. \quad (8)$$

To apply (8) to the Weaver architecture, we first define the transfer function of the variable phase and gain blocks as

$$\theta = k_1 w_1 \quad (9)$$

$$G = k_2 w_2 \quad (10)$$

where  $\theta$  is the phase in radians,  $G$  is the gain,  $k_1$  and  $k_2$  are constants, and  $w_1$  and  $w_2$  are the coefficients. For simplicity,

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- [6] S. Tadp
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- [8] L. Yu
- [9] J. Ma
- [10] B. Wid
- [11] J. E. C
- [12] L. Der



we set the constants  $k_1$  and  $k_2$  to unity. With these definitions, we can now write the error signal  $\epsilon(t)$  as

$$\epsilon(t) = -y(t) = A(t) \sin(\omega_{LO2}t + \theta) - B(t)G \cos(\omega_{LO2}t). \quad (11)$$

Taking the partial derivative of  $\epsilon(t)$  with respect to the coefficients, we find

$$x_1(t) = A(t) \cos(\omega_{LO2}t + \theta) \quad (12)$$

$$x_2(t) = -B(t) \cos(\omega_{LO2}t). \quad (13)$$

For small phase errors, (12) can be approximated by

$$x_1(t) \approx A(t) \cos(\omega_{LO2}t). \quad (14)$$

Finally, substituting (13) and (14) in (8), we arrive at the desired gain and phase coefficients

$$w_1[(m+1)T] \approx w_1[mT] - 2\mu\epsilon[mT]A[mT] \cos(\omega_{LO2}[mT]) \quad (15)$$

$$w_2[(m+1)T] = w_2[mT] + 2\mu\epsilon[mT]B[mT] \cos(\omega_{LO2}[mT]). \quad (16)$$

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**Lawrence Der** (M'88) received the B.S. and M.S. degrees in electrical engineering from the University of California at Davis (UC Davis) in 1989 and 1994, respectively, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles (UCLA) in 2001.

He has held various design engineering, senior design engineering, and design management positions between, during, and after his studies at UC Davis and UCLA with such companies as 3COM Corporation, Micro Linear, Hyundai Wireless Telecommunications, Broadcom Corporation, and Transpectrum. Since August 2002, he has been a Design Manager with Resonext Communications, Inc. His current research interests include wireless transceivers, adaptive equalizers, and clock and data recovery circuits for high-speed data communications.

Dr. Der is a member of Eta Kappa Nu, Tau Beta Pi, and Pi Mu Epsilon. He was a corecipient of the Jack Kilby Outstanding Student Paper Award at the 2001 IEEE International Solid-State Circuits Conference.



**Behzad Razavi** (S'87-M'90-SM'00-F'03) received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1985 and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was an Adjunct Professor with Princeton University, Princeton, NJ, from 1992 to 1994, and Stanford University in 1995. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since September 1996, he has been

an Associate Professor and, currently, Professor of electrical engineering at University of California at Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. He is the author of *Principles of Data Conversion System Design* (New York: IEEE Press, 1995), *RF Microelectronics* (Englewood Cliffs, NJ: Prentice-Hall, 1998) (translated to Japanese by Tadahiro Kuroda), *Design of Analog CMOS Integrated Circuits* (New York: McGraw-Hill, 2001), and *Design of Integrated Circuits for Optical Communications* (New York: McGraw-Hill, 2002), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (Piscataway, NJ: IEEE Press, 1996).

Dr. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the best paper award at the IEEE Custom Integrated Circuits Conference in 1998. He was the corecipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 IEEE International Solid-State Circuits Conference. He served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and is currently a member of the Technical Program Committee of the Symposium on VLSI Circuits. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the *International Journal of High Speed Electronics*. He is an IEEE Distinguished Lecturer.