Brief Papers

Broadband ESD Protection Circuits in CMOS Technology

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***Abstract*—A broadband technique using monolithic T-coils is applied to electrostatic discharge (ESD) structures for both input and output pads. Fabricated in 0.18-μm CMOS technology, the prototypes achieve operation at 10 Gb/s while providing a return loss of −20 dB at 10 GHz. The human-body model tolerance is 1000 V for the input structure and 800–900 V for the output structure.**

***Index Terms*—Broadband amplifiers, high-speed ESD protection, impedance matching, T-coils, T-coil peaking.**

I. Introduction

THE problem of electrostatic discharge (ESD) continues to become more critical in today's industry [1]. In particular, three trends exacerbate the issue: 1) the speed of both analog and digital circuits is increasing, reaching several tens of gigabits per second for data communication circuits and several gigahertz for microprocessors; 2) the number of high-speed I/O pads is also rising, exceeding 100 in data communication chips and 500 in microprocessors; and 3) the device dimensions have scaled down to a gate length of 90 nm and oxide thickness of 20 Å.

From these observations, we conclude that high-speed ESD protection circuits must satisfy several difficult criteria. These circuits should: 1) provide a broad bandwidth despite the parasitic capacitance of the ESD protection device itself; 2) occupy a small area with a reasonable aspect ratio so that tens or hundreds of these devices can be integrated on chip without complicating the layout and routing; 3) create good impedance matching at the input and output to avoid corrupting the high-speed data; and 4) exhibit negligible midband loss.

This paper introduces new broadband ESD protection circuits in CMOS technology that satisfy all of these four criteria. Section II reviews the conventional techniques for ESD protection and their shortcomings. Section III describes the properties of T-coil networks as a foundation for ESD protection circuits, and Section IV presents the architecture and design of the circuits for inputs and outputs. Section V summarizes the experimental results.

II. Conventional Circuit Techniques for ESD Protection

To provide reasonable ESD tolerance, ESD protection circuits must incorporate large devices. As a result, ESD circuits introduce substantial parasitic capacitance that limits the signal bandwidth. This section reviews the conventional techniques used to minimize the effect of the ESD parasitic capacitance and describes their associated problems.

A. Inductive Peaking

In broadband applications, inductive peaking can be used along with the on-chip termination resistor to widen the signal bandwidth [Fig. 1(a)]. While improving the speed by 40% with negligible overshoot, this technique suffers from poor impedance matching. This can be seen from the input return loss plotted in Fig. 1(b) for $C_{\rm ESD} = 1.2$ pF and $R = 50\ \Omega$. The interface exhibits an S_{11} of better than −10 dB up to only 2.4 GHz. In fact, if two such I/O circuits operate at 10 Gb/s and communicate through a 4-in 50-Ω trace [Fig. 1(c)], the simulated eye diagram of the received data appears as shown in Fig. 1(d).[1]

B. Distributed ESD

A broadband technique that addresses the issue of impedance matching distributes the ESD protection device along a transmission line (T-line) as shown in Fig. 2(a) [2]. For a total ESD capacitance of $C_{\rm ESD}$, the length and width of the T-line are chosen to obtain a 50-Ω characteristic impedance:

$$Z_o = \sqrt{\frac{L}{C_{\rm ESD} + C_{\rm line}}} \tag{1}$$

where L and $C_{\rm line}$ denote the total inductance and the parasitic capacitance of the line, respectively. In practice, on-chip T-lines may run over a metal-1 ground plane to better define the line characteristics.

Distributed ESD structures satisfy two of the four criteria mentioned in Section I: broad bandwidth and good impedance matching. However, this technique suffers from a severe tradeoff between the signal loss, the ESD capacitance (and hence, the voltage tolerance), and the overall area of the distributed structure. For example, to absorb $C_{\rm ESD} = 1.2$ pF in a 50-Ω T-line (constructed using metal-6 on top of a metal-1 ground plane in 0.18-μm CMOS technology), field simulation results show that the line must have a length of 8 mm and a width of 3 μm. Such a line introduces a midband loss of around 6 dB. The simulated eye diagram at the end of a lossy T-line terminated to 50 Ω is shown in Fig. 2(b) and compared with the lossless case. This issue becomes more serious if the high-frequency losses of the

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[1]The transmitted data is a random binary sequence with no intersymbol interference.

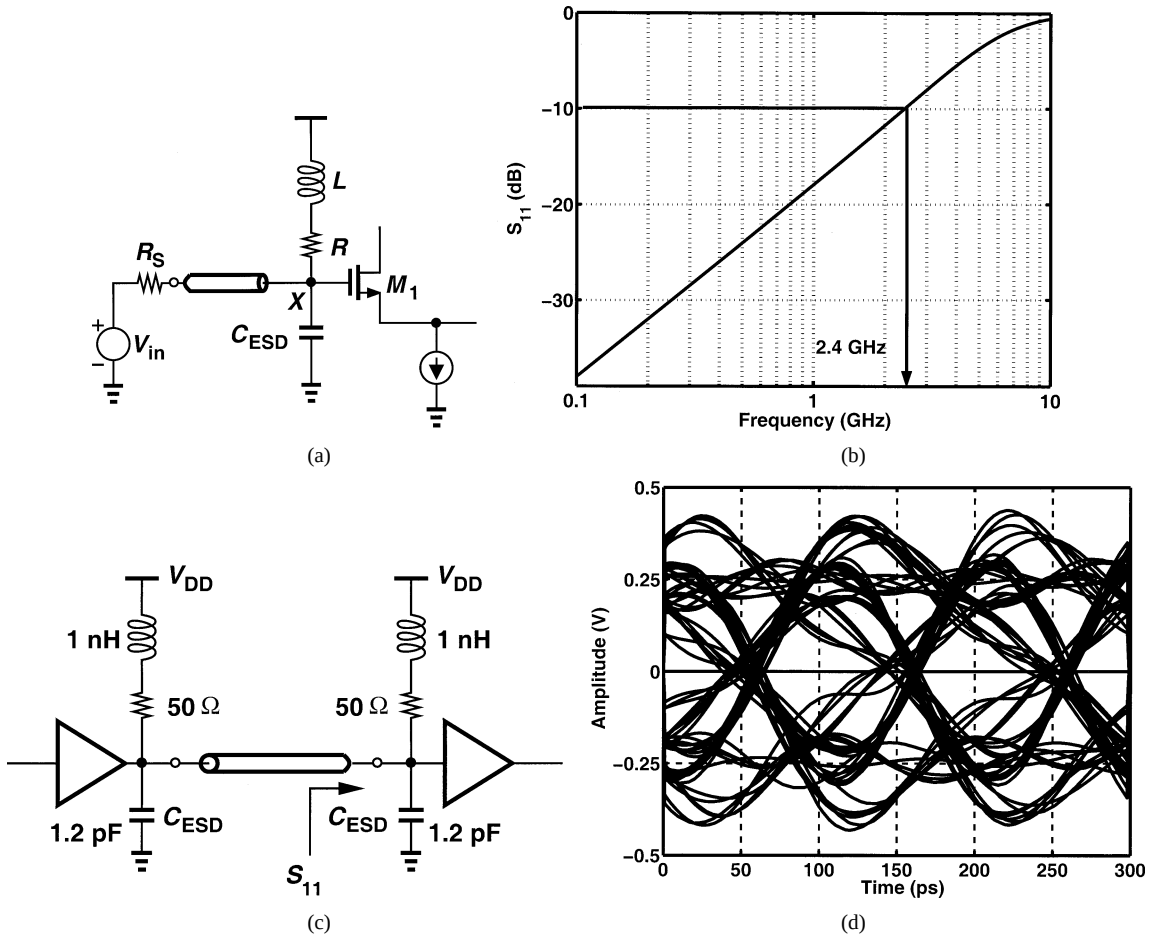


Fig. 1. (a) Inductive peaking at input. (b) Return loss at the interface. (c) Two I/Os communicating through a 4-in 50-Ω trace. (d) Simulated eye diagram of the received data.

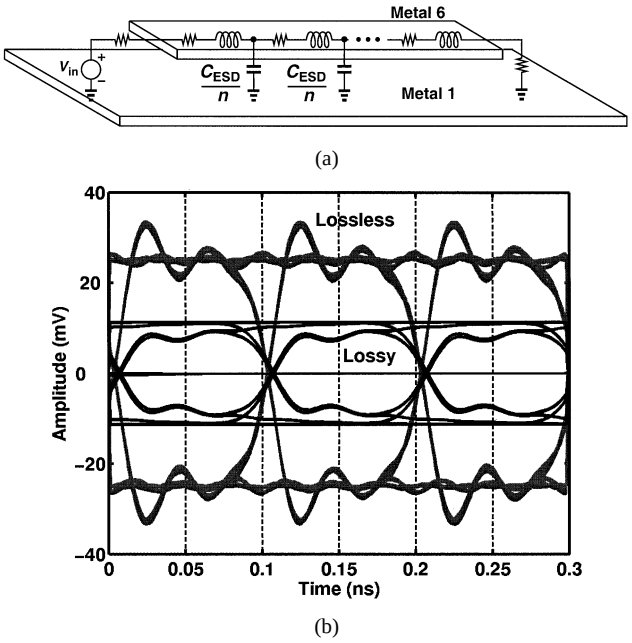


Fig. 2. Distributed ESD (a) topology and (b) simulated eye diagram.

T-line are also taken into account. Note that the long line structure creates difficulties in layout and routing of other signals even if it is folded many times.

Interestingly, the series resistance of the T-line may not allow a uniform distribution of the ESD current among different fingers. As a result, the ESD device near the I/O pad may break first, carrying a large current and incurring damage. That is, the ESD voltage tolerance may be defined by only the first few fingers.

III. T-Coil Networks in Broadband Design

T-coils have been used in discrete form in high-speed circuits for oscilloscopes [3]. Depicted in Fig. 3(a), a T-coil network consists of two coupled inductors L_1 and L_2 having a coupling coefficient of k and a bridge capacitor C_B. The input is applied to terminal A, the termination resistor R_T is connected to terminal B, and the load capacitance C_L is tied to terminal X.

T-coils offer two attributes that prove useful in ESD design. First, if designed properly, the circuit displays a purely resistive input impedance, $Z_{\text{in}} = R_T$, *independent* of the frequency and the value of C_L. This can be seen intuitively by recognizing that at low frequencies, L_1 and L_2 short the input to R_T, and at high frequencies, C_B plays the same role while L_1 and L_2 are open. It can be proved that the input impedance Z_{in} remains resistive for all frequencies if the following conditions hold:

$$L_1 = L_2 = \frac{C_L R_T^2}{4}\left(1 + \frac{1}{4\zeta^2}\right) \tag{2}$$

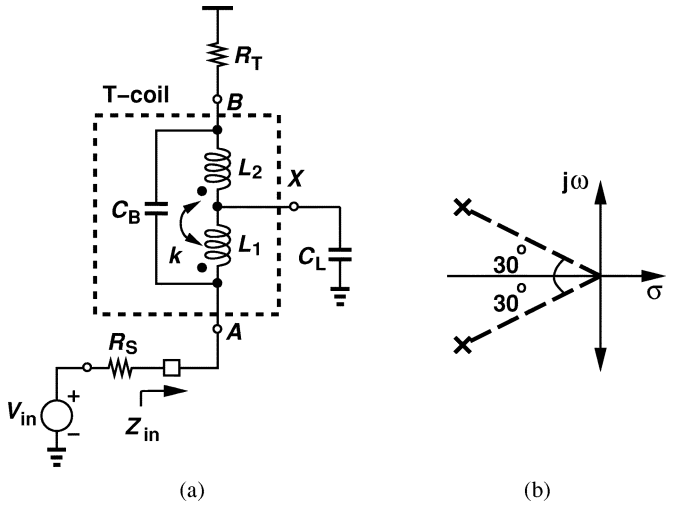


Fig. 3. (a) T-coil network. (b) Locations of poles for uniform group delay response.

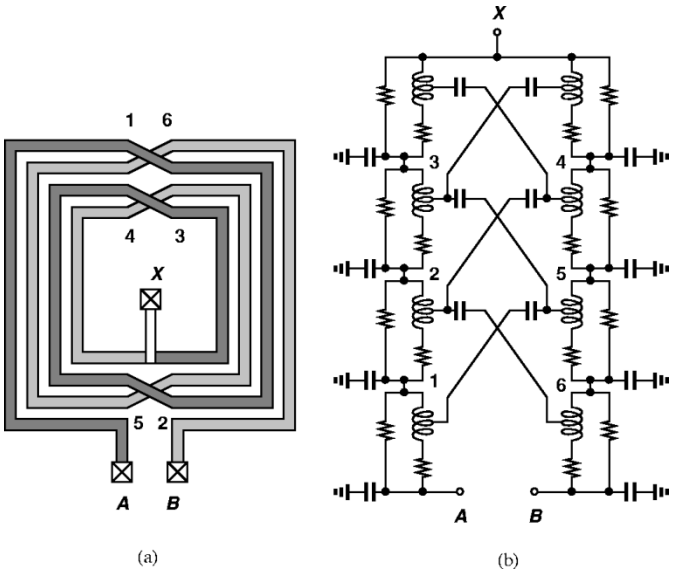


Fig. 4. T-coil network. (a) Layout. (b) Distributed model.

$$C_B = \frac{C_L}{16\zeta^2} \tag{3}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{4}$$

where ζ is the damping factor of the network transfer function $V_X/I_{\rm in}$. As these equations suggest, ζ and, hence, k are chosen to target a desired response, and other T-coil parameters are subsequently determined.

For uniform group delay, the complex poles of $V_X/I_{\rm in}$ must bear an angle of $\theta = 30°$ with respect to the real axis [Fig. 3(b)] [3]. Since $\zeta = (\sqrt{1+\tan^2\theta})^{-1}$, we have $\zeta = \sqrt{3}/2$ and, hence, $k = 1/2$. Thus, (2)–(4) reduce to

$$L_1 = L_2 = \frac{C_L R_T^2}{3} \tag{5}$$

$$C_B = \frac{C_L}{12} \tag{6}$$

$$k = 1/2. \tag{7}$$

The second attribute of T-coils is that they enhance the bandwidth to a greater extent than inductive peaking does. Under the conditions given by (2)–(4), the transfer function of the T-coil network is given by

$$\frac{V_X}{I_{\rm in}} = \frac{R_T}{\frac{1}{4}\left(\frac{1-k}{1+k}\right) R_T^2 C_L^2 s^2 + \frac{1}{2} R_T C_L s + 1}. \tag{8}$$

With $k = 1/2$ for uniform group delay, the bandwidth is broadened by a factor of 2.72, which is a 70% increase over that provided by inductive peaking having the same type of response. The maximum improvement factor for T-coils is $2\sqrt{2} \approx 2.82$ and occurs for $\theta = 45°$ and a tighter coupling $k = 7/9$.

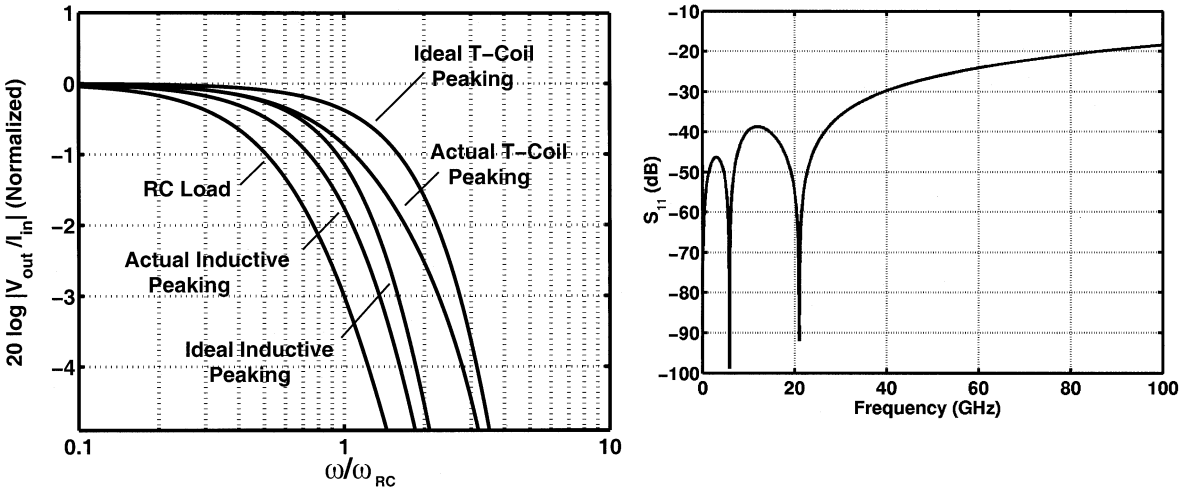
The absence of a zero in the above transfer function can be explained as follows. If for a complex frequency s, $V_X = 0$, then C_L carries no current and $I_{\rm in}$ flows entirely through R_T. Thus, for $L_1 = L_2$, the symmetry requires that V_X be equal to $V_{\rm in}/2$, contradicting the original assumption. Note that the impedance seen looking back from the circuit side has the same poles and no zeros.

The T-coil network of Fig. 3(a) provides an environment that is well suited to ESD protection, where the ESD protection device replaces C_L and R_T serves as an on-chip termination resistor. This topology satisfies at least two of the three main criteria described earlier: the network offers both broad bandwidth and good impedance matching. The other two criteria are studied below.

The fortunate coincidence $L_1 = L_2$ points to the use of a symmetric spiral realization of the T-coil [Fig. 4(a)] with the center tap representing the output terminal. To obtain the required values, $L_1 = L_2 = L = C_L R_T^2/3$ and $k = 1/2$, we first note that the total inductance between nodes A and B is equal to $2L(1+k) = 3L = C_L R_T^2$. Simulations using ASITIC [4] indicate that the coupling coefficient between the two halves in Fig. 4(a) is a strong function of the line spacing. Thus, with an initial guess for the number of turns and the outer dimension, the line width is chosen to minimize the loss, and the line spacing to obtain $k = 1/2$. Next, the outer dimension is adjusted to achieve $L_{AB} = C_L R_T^2$.

If used in broadband circuits, T-coils must be modeled such that their response remains accurate for the last decade of the band of interest. (It is assumed that the network plays a negligible role at lower frequencies.) Fig. 4(b) shows the distributed model used here. The spiral is decomposed into eight sections $(A{-}1, 1{-}2, \ldots, 6{-}B)$, each represented by an inductance, series and parallel resistances, and a parasitic capacitance to the substrate. The resistances are chosen to yield a Q of 7 at 6.5 GHz. The fringe capacitance between adjacent turns is also included. Note that this capacitance appears between nodes A and B in a distributed fashion. Thus, the bridge capacitance C_B is chosen equal to the required value minus the total interwinding capacitance.

Fig. 5(a) plots the transfer functions of three types of networks: a first-order RC load, an inductively-peaked load with ideal or realistic inductor models, and a T-coil with ideal or realistic T-coil models. (Each network is driven by an ideal current source and the frequency is normalized to the original RC bandwidth.) It can be seen that T-coils outperform inductive



(a) (b)

Fig. 5. (a) T-coil performance comparison. (b) Return loss of the distributed T-coil model for $C_L = 1.2$ pF.

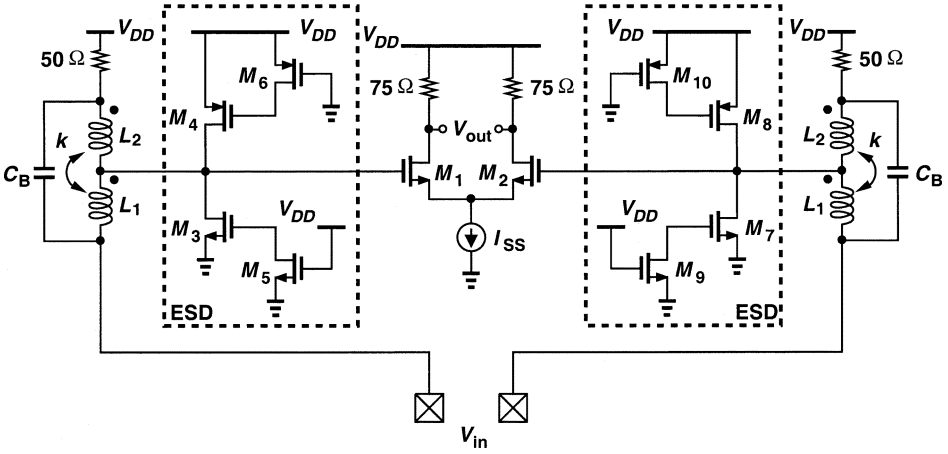


Fig. 6. Input ESD protection circuit.

peaking by 50% even with realistic models. With all of the nonidealities included, the T-coil network also displays high-quality matching. Fig. 5(b) shows the simulated return loss with the broadband model of Fig. 4(b) and $C_L = 1.2$ pF, suggesting that S_{11} remains better than -40 dB for frequencies as high as 25 GHz.

The utility of T-coils is nonetheless limited to low-impedance interfaces. As suggested by (2), the dependence of L_1 and L_2 upon R_T^2 leads to high inductance values if R_T is relatively large.

IV. ESD Protection Circuits

A. Input and Output Circuits

Fig. 6 depicts the input ESD protection circuit. Each input pad is followed by a T-coil network and the ESD device (obtained from the foundry). The differential pair M_1–M_2 serves as a typical input stage, also allowing high-speed testing by sensing the output of the T-coils and driving a 75-Ω on-chip termination and a 50-Ω off-chip load. In this design, $L_1 = L_2 = 1$ nH and the symmetric inductor measures 85 μm $\times$ 85 μm, which is an area and shape comparable with those of the ESD device itself.

For output ESD protection, the T-coil can be used as shown in Fig. 7(a), where the output current is drawn from the center tap and the load is tied to node A. We note that $Z_{\rm out}$ exhibits the same behavior as $Z_{\rm in}$ in Fig. 3(a). Furthermore, since the network topology remains unchanged, the circuits of Figs. 3(a) and 7(a) contain identical poles. This configuration is also free of a zero. If $V_{\rm out} = 0$ for some value of s, then with $L_1 = L_2$, symmetry requires that R_L and R_T carry no current, $V_X = -I_{\rm out}/(C_{\rm ESD}s)$, and $V_{\rm out} = V_X$, contradicting the original assumption. Thus, the input and output protection circuits exhibit identical transfer functions.

The finite output resistance of $I_{\rm out}$ in Fig. 7(a) does introduce some error in the above calculations. Fig. 7(b) depicts a modification [5] whereby resistor R_2 is added in series with L_2 to account for the effect of R_o. If $R_o \gg R_T$, the equations in [5] can be simplified as

$$L_1 = L_2 = \frac{C_L R_T^2}{2(1+k)}\left(1+\frac{R_T}{R_o}\right) \tag{9}$$

$$R_2 = \frac{R_T^2}{R_o} \tag{10}$$

$$C_B = \frac{C_L}{4}\frac{1-k}{1+k}\left(1+\frac{R_T}{R_o}\right). \tag{11}$$

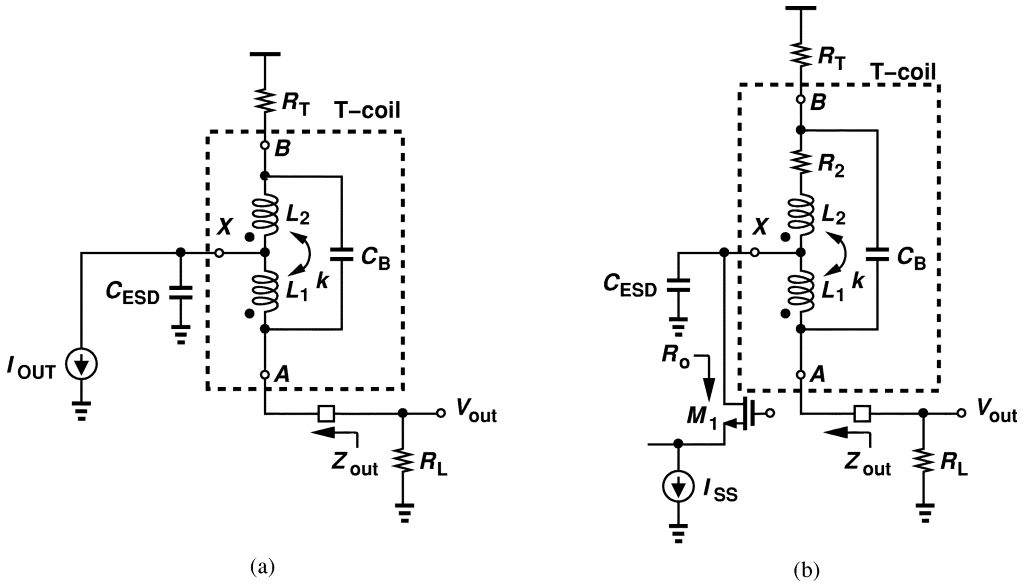


Fig. 7. (a) Output T-coil network. (b) R_2 is added to account for R_o.

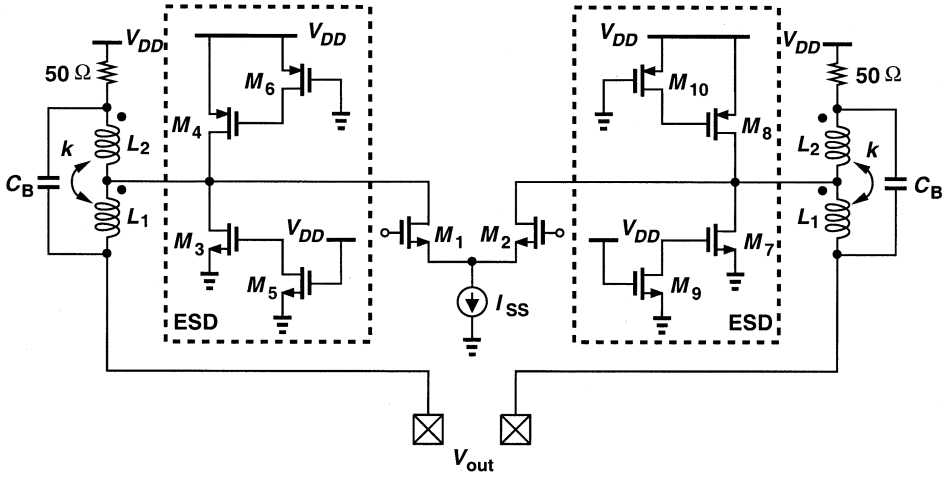


Fig. 8. Output ESD protection circuit.

These results reduce to (2)–(4) if $R_o = \infty$ because $4\zeta^2 = (1+k)/(1-k)$. In this design, R_o is sufficiently large to justify eliminating R_2.

The output protection circuit is shown in Fig. 8, where the differential pair M_1–M_2 represents a typical output stage. The T-coil and ESD devices are identical to those used in the input circuit.

B. Midband Loss Behavior

An important attribute of the proposed ESD circuits is that the series resistance of the T-coil does not translate to signal loss. As shown in Fig. 9 for the input circuit, equal resistors placed in series with the T-coil inductors leave the signal amplitude at node X unchanged as long as the input is driven by a source impedance equal to R_T. The same argument applies to the output circuit as well. This is in sharp contrast to the distributed ESD technique and the results illustrated in Fig. 2(b).

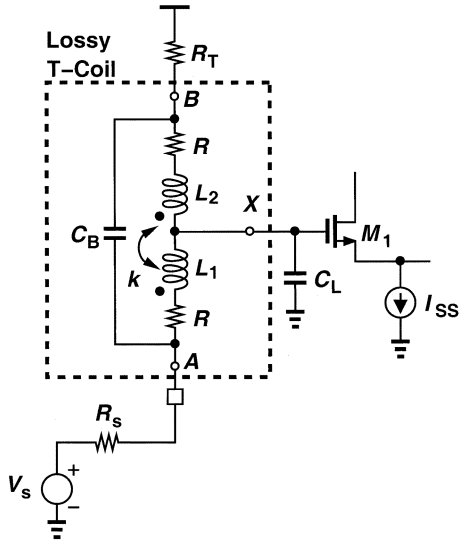
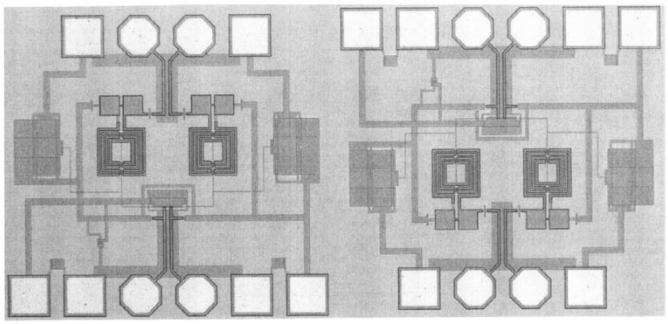
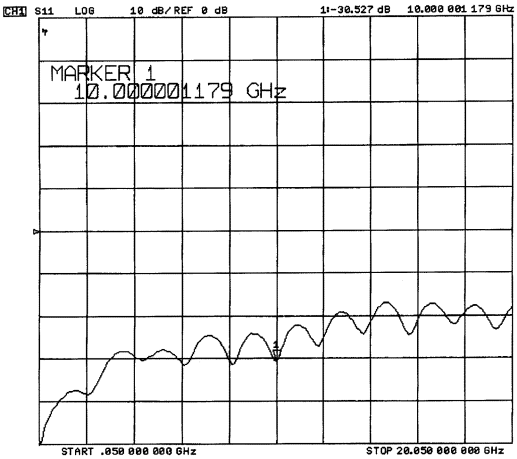


Fig. 9. Midband loss behavior of input ESD circuit.

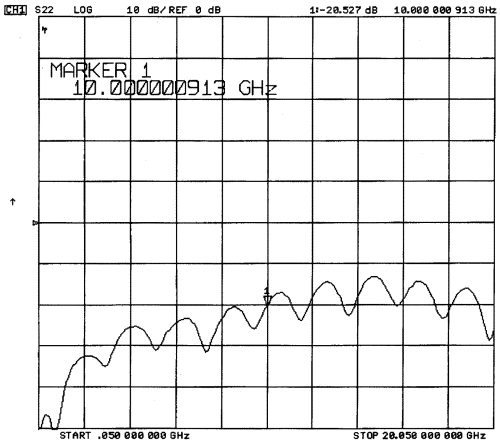


(a) (b)

Fig. 10. Die photograph of (a) input and (b) output ESD circuits.



(a)

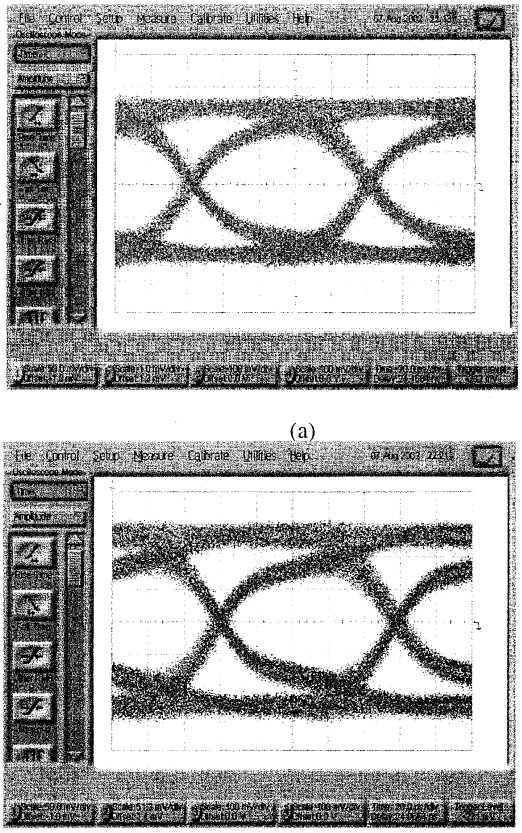


(b)

Fig. 11. Measured return loss of (a) input (S_{11}) and (b) output (S_{22}) ESD circuits. (Horizontal scale: $\sim$2 GHz/div., vertical scale: 10 dB/div.)

V. Experimental Results

The input and output ESD circuits have been fabricated in 0.18-μm CMOS technology and tested with a 1.8-V supply.The die photographs for both circuits are shown in Fig. 10. The T-coils have been placed away from the high-frequency pads to minimize the effect of the pads on the inductance of the T-coils.[2] The measured single-ended return loss for both the input and the output ESD circuits is shown in Fig. 11. For frequencies as high as 10 GHz, the input circuit exhibits $S_{11} < -24$ dB and the output circuit $S_{22} < -20$ dB. Single-ended return loss measurements are quite pessimistic since the bond wire inductance of the supply lines appears in series with the T-coil, which is not the case for actual differential operation. The input and output circuits are also tested with a pseudorandom $10^{23}-1$ input bit stream. As shown in Fig. 12, both circuits provide a reasonable eye opening at 10 Gb/s.



(a)

(b)

Fig. 12. Measured eye digram for (a) input ESD circuit and (b) output ESD circuit. (Horizontal scale: 20 ps/div., vertical scale: 50 mV/div.)

TABLE I
ESD Voltage Tolerance of Input and Output Circuits

	Zapping Voltage	
ESD Circuit	HBM	MM
Input	1000 V	100 V
Output	800-900 V	100 V

Both circuits have been tested according to the JEDEC standards, JESD22-A114-B [6] for the human-body model (HBM)

[2]In a more aggressive design, the T-coils can be placed near their respective pads because the pads appear in series with the T-coils and are at approximately the same potential. ASITIC simulations suggest an inductance variation of less than 5% and a Q variation of less than 1% as the spacing varies from a few micrometers to tens of micrometers.

and JESD22-A115-A [7] for the machine model (MM) using positive and negative pulses with a 0.5-s cooldown period. Failure is defined as 10% increase in the leakage current of the I/O pad after the ESD stress is applied. The zapping voltage is varied from 200 V to 2 kV in steps of 100 V for the HBM test and from 50 to 200 V in steps of 50 V for the MM test. Table I summarizes the voltage tolerance of the ESD circuits.

The relatively low ESD zapping voltage may arise from the series resistance of the T-coil, which uses a line width of 4 μm for the spiral. It is possible to place in parallel with this spiral replicas in metal-5 and metal-4 layers so as to reduce this resistance.

VI. Conclusion

New broadband input and output ESD protection circuits realized in CMOS technology are presented. The circuits provide a broad bandwidth, good impedance matching, and low midband loss while occupying reasonable area. The proposed circuits are fully compatible with standard CMOS technology.

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