A 0.4–6 GHz Receiver for Cellular and WiFi Applications

Hossein Razavi, *Graduate Student Member, IEEE*, and Behzad Razavi, *Fellow, IEEE*

***Abstract*— A wideband RF receiver employs a multi-loop architecture to ease the tradeoff between noise and linearity, a new method of harmonic rejection that relaxes gain and phase matching requirements, and a new op amp topology to achieve a wide bandwidth with low power consumption. Furthermore, multiple techniques are introduced to improve the out-of-band and in-band linearity, input matching, and stability. Fabricated in 28-nm CMOS technology, the prototype accommodates channel bandwidths from 200 kHz to 160 MHz and exhibits a noise figure of 2.1–4.42 dB while drawing 23–49 mW. It demonstrates an out-of-band IIP3 of 2.8–9.8 dBm and provides more than 60 dB of rejection for blockers at the third and fifth harmonics of the LO.**

***Index Terms*— Harmonic rejection, linearity, multi-loop, op amp, wideband.**

I. Introduction

THE demand for accommodating a greater number of bands and standards in mobile devices continues to challenge RF designers. Receivers serving in such an environment typically require numerous off-chip filters, occupy a large chip area, and present severe difficulties with respect to the generation and distribution of local oscillator (LO) signals. Concepts such as the "software radio" [1], the "software-defined radio" [2], and the "universal radio" have been introduced to deal with these issues, and a great deal of research has been expended on such solutions [3]–[37].

This article describes a receiver (RX) that targets long-term evolution (LTE) and Wi-Fi standards, operating with an input frequency range of 400 MHz to 6 GHz and a channel bandwidth (CBW) from 200 kHz to 160 MHz [3]. A number of new architecture and circuit techniques are presented that deliver a noise figure (NF) of 2.1–4.42 dB and a harmonic blocker rejection of greater than 60 dB with no calibration.

Section II provides a brief background on universal receiver challenges, and Section III presents the proposed receiver architecture. Section IV describes the circuit techniques required to develop such a receiver, and Section V summarizes the experimental results.

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Hossein Razavi is with Broadcom Inc., Irvine, CA 92617 USA (e-mail: shrazavi@ucla.edu).

Behzad Razavi is with the Department of Electrical and Computer Engineering, University of California at Los Angles, Los Angeles, CA 90095 USA (e-mail: razavi@ee.ucla.edu).

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II. Background

A receiver supporting LTE and Wi-Fi must satisfy the exacting specifications of these standards while maintaining, across a wide input frequency range, a low NF, high linearity, and proper input matching. In essence, such a receiver bears each standard's heaviest burden and must accommodate a multitude of conflicting requirements. In this section, we summarize some of the prominent issues that we face in this endeavor.

The development of our universal RX entails four principal challenges. First, it must deal with large blockers as stipulated by LTE. For example, a 0-dBm GSM blocker at a 23-MHz offset with respect to the desired signal must not desensitize the RX chain excessively. Among prior investigations of this issue, Darabi [4], Ayazian and Gharpurey [5], and Safarian *et al.* [6] propose the use of feedforward filtering to suppress the large out-of-band blocker at RF before it compresses the receiver chain, but the performance is limited by the phase and gain mismatches of the main path and the filtering path. The approach taken by Andrews and Molnar [7], [8], Yang *et al.* [9], Lien *et al.* [10], [11], and Pini *et al.* [12] introduces a mixer-first receiver architecture to filter the blocker before reaching a gain stage but at the cost of a high NF and power consumption. The technique proposed in [13]–[15], on the other hand, suggests the use of N-path filters, but it requires large switches to provide sufficient out-of-band rejection, thus increasing the power consumed in the clock path and degrading the performance at higher input frequencies. While Miller multiplication of N-path filters (see [16] and [17]) alleviates these issues up to 2.4 GHz [16], the large switches that inevitably load the receiver input would degrade the performance at 6 GHz even if they remain OFF. We address this point in Section III.

The second challenge relates to harmonic blockers. Due to its broad bandwidth, the receiver must reject blockers that appear at the LO harmonics, a task typically performed by harmonic-reject mixing [18]. However, as explained in Section III, this approach would demand phase mismatches as low as 35 fs. Ru *et al.* [19], [21], Murphy *et al.* [20], van Liempd *et al.* [22], and Borremans *et al.* [23] introduce various enhancement techniques in the analog and digital domains that are discussed in Section III, but each has its own drawbacks.

The third challenge stems from the flicker noise of the receiver's baseband (BB) section. To ensure a low NF for narrowband LTE channels, the BB chain must employ large transistors. This, however, severely limits the circuit's bandwidth, prohibiting operation with Wi-Fi's 160-MHz channels. Alternatively, we can allocate a greater RF gain, but the linearity suffers, making it difficult to process LTE's 64 QAM

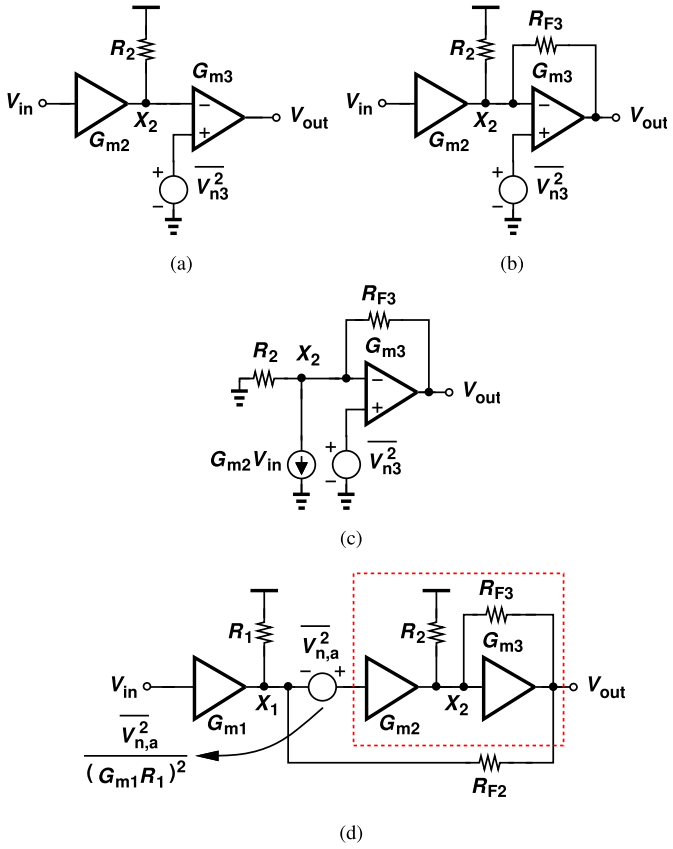


Fig. 1. (a) Cascade of two stages, (b) cascade with the second stage in a feedback loop, (c) first stage of the cascade replaced with its equivalent circuit, and (d) nested feedback network with three stages.

and Wi-Fi's 256-QAM signals. We return to this issue in Section III.

The fourth challenge concerns the necessary linearity for Wi-Fi's 160-MHz signals in the presence of adjacent and alternate-adjacent channels. Since the BB chain must remain far below compression, power-hungry op amps with relatively high supply voltages appear necessary. This condition is eased by a new op amp topology described in Section IV.

III. Proposed Receiver Architecture

This section presents the evolution of our receiver architecture in the context of the four challenges described above.

A. Multi-Loop Topology

We begin with the third challenge, namely, the problem of BB flicker noise. Consider the simple cascade shown in Fig. 1(a), where $\overline{V_{n3}^2}$ models the input-referred noise of the second stage. This quantity is divided by $(G_{m2}R_2)^2$ as it is referred to V_{in}. Now, suppose that the second stage is placed in a feedback loop so as to create a virtual ground at X_2 and improve the linearity [see Fig. 1(b)]. From the equivalent circuit shown in Fig. 1(c), we have

$$V_{\text{out}} = G_{m2}V_{\text{in}}R_{F3} + \left(1 + \frac{R_{F3}}{R_2}\right)V_{n3}. \tag{1}$$

The output noise voltage is, thus, divided by $G_{m2}R_{F3}$ as it is referred to the input, yielding

$$\overline{V_{n,a}^2} \approx \frac{\overline{V_{n3}^2}}{(G_{m2}R_2)^2} \tag{2}$$

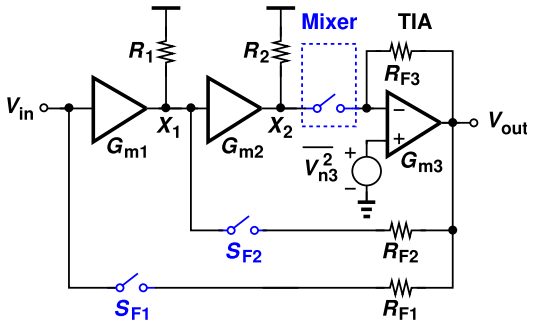


Fig. 2. Simplified multi-loop RX architecture with mixer and feedback upconversion switches.

if $R_{F3} \gg R_2$. The key point here is that the cascade's NF remains fairly unchanged even though feedback lowers the voltage gain. This property holds whether the chain operates entirely at RF, at BB, or at RF and BB.

Let us extend the forgoing concept and "nest" the above circuit within a topology like itself [see Fig. 1(d)]. Here, $\overline{V_{n,a}^2}$ is still due to G_{m3}. According to our previous derivations, we can refer $\overline{V_{n,a}^2}$ to the input of G_{m1}:

$$\overline{V_{n,b}^2} \approx \frac{\overline{V_{n,a}^2}}{(G_{m1}R_1)^2} \approx \frac{\overline{V_{n3}^2}}{(G_{m1}R_1G_{m2}R_2)^2} \tag{3}$$

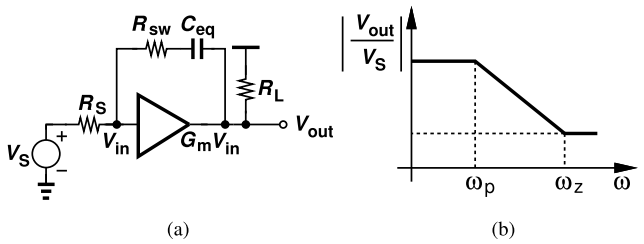
if $R_{F2} \gg R_1$. For this three-stage chain, we have $|V_{\text{out}}/V_{\text{in}}| \approx G_{m1}R_{F2}$. The remarkable result obtained here is that the input signal experiences a low voltage gain and virtual grounds at X_1 and X_2, whereas the noise voltage of G_{m3} is divided by $G_{m1}R_1G_{m2}R_2$. In other words, V_{in} benefits from the high linearity at X_1 and X_2, while V_{n3} is divided by the *open-loop* gain.

The multi-loop architecture of Fig. 1(d) can readily include BB operations as well. Illustrated conceptually in Fig. 2 is such a realization where G_{m3} is embedded within the BB transimpedance amplifier (TIA). In this case, R_{F2} returns the BB signal, which is upconverted by S_{F2} before arriving at X_1. We recognize that the high flicker noise of the TIA can be greatly suppressed by the preceding RF gain without sacrificing the receiver linearity.

The broadband input matching necessary for the receiver prohibits the use of inductive degeneration. In a manner similar to [24] and [25], our work employs R_{F1} and S_{F1} for this purpose. However, as explained in Section IV, this approach suffers from unwanted peaking due to the finite phase shift around the loop, requiring proper compensation. The switching circuits in Fig. 2 can be constructed as four-phase or eight-phase networks driven by nonoverlapping LO waveforms (see Section IV).

B. Blocker Rejection

The proposed multi-loop architecture of Fig. 2 maintains low-voltage swings at X_1 and X_2 for the desired signal and moderately large interferers. Nonetheless, its linearity does not suffice for LTE's out-of-band blocker rejection. The use of N-path filters proves effective here [13], [14], [26]. For example, placing such a filter around an amplifier provides Miller multiplication of the capacitors and Miller reduction of switch resistances [16], [17]. As demonstrated in [16], a 0-dBm blocker tolerance can be achieved with low



(a) (b)

Fig. 3. (a) BB equivalent model of an N-path filter placed around a gain stage and (b) its frequency response.

"open-loop" compression points. In our work, two Miller N-path networks raise $P_{1-\mathrm{dB}}$ to +14 dBm at a 23-MHz offset.

It has been observed in the prior art that the out-of-channel or out-of-band rejection of the N-path filters is limited by the ON-resistance of their switches, R_{sw} [16], [27]. This poses severe difficulties in our receiver because, if the switches are wide enough to suppress the 0-dBm blocker at, for example, 1 GHz, then their parasitics degrade the performance at 6 GHz even if they remain OFF. Since the maximum tolerable value of R_{sw} is independent of the number of paths, the issue becomes more severe if an RX employs eight-phase filters to allow harmonic rejection (see Section IV). Interestingly, the situation is different when they are placed in a feedback loop. Consider the equivalent BB model of such an arrangement, as shown in Fig. 3(a). We have

$$\left|\frac{V_{\mathrm{out}}}{V_S}\right| = G_m R_L \left|\frac{1 + j\left(R_{\mathrm{sw}} - \frac{1}{G_m}\right)C_{\mathrm{eq}}\omega}{1 + j[R_{\mathrm{sw}} + R_L + (1 + G_m R_L)R_S]C_{\mathrm{eq}}\omega}\right| \tag{4}$$

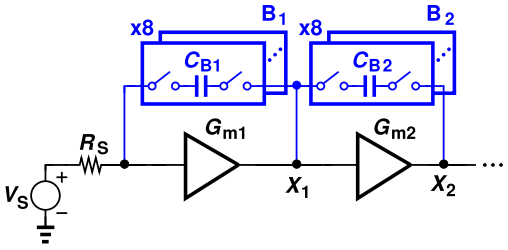
where ω denotes the offset frequency with respect to the carrier. Notably, the circuit exhibits a zero whose absolute value, ω_z, is greater than that of the pole, ω_p, leading to the response depicted in Fig. 3(b). Thus, the rejection beyond ω_z is bounded by

$$\left|\frac{V_{\mathrm{out}}}{V_S}(\omega = \infty)\right| = \frac{\left|R_{\mathrm{sw}} - \frac{1}{G_m}\right|}{R_{\mathrm{sw}} + R_L + (1 + G_m R_L)R_S} G_m R_L. \tag{5}$$

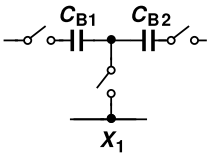
Interestingly, the gain beyond ω_z can be zero if $R_{\mathrm{sw}} = 1/G_m$. This is also seen from Fig. 3(a) by noting that $G_m V_{\mathrm{in}} = (V_{\mathrm{in}} - V_{\mathrm{out}})/R_{\mathrm{sw}}$.

The key observation here is that we can benefit from unlimited rejection if $R_{\mathrm{sw}} = 1/G_m$, i.e., R_{sw} need not be minimized. The rejection is ultimately dictated by the mismatch between R_{sw} and $1/G_m$. This unique property is, of course, absent in "passive" N-path filters and is studied in more detail in Appendix I. On the other hand, a Miller N-path filter requires the amplifier to absorb the blocker current [16]. In this work, a 0-dBm blocker at a 23-MHz offset generates about 10 mA, of which 8.8 mA are absorbed by Stage 1 in Fig. 4(a) through Bank 1. This is possible by virtue of this stage's class-AB action [16]. Equivalently, the 1-dB compression point at this offset is about +14 dBm.

In this work, we have chosen $R_{\mathrm{sw}} \approx 3/G_m$ to allow even narrower switches, a necessary compromise in terms of switch parasitics in the signal path and the power consumption in the LO path. To ensure sufficient linearity in the presence of a 0-dBm blocker, we attach two Miller filters, Bank 1 and Bank 2, to the first two stages of the receiver [see Fig. 4(a)]. This circuit merits several remarks. First, in the presence of the feedback paths depicted in Fig. 2, the first and second stages provide voltage gains equal to 9 dB $\equiv$ 2.8 and 7 dB $\equiv$ 2.2, respectively, allowing proportional reduction of the capacitor values and switch widths in their banks. Second, since $G_{m2} \approx 0.5G_{m1}$ (to save power), the devices in Bank 2 are scaled down by this factor with respect to those in Bank 1. Thus, the two banks, in fact, introduce smaller parasitics than a single bank providing the same amount of rejection. The number of switches is further decreased by "factoring out" those attached to the right plate of C_{B1} and the left plate of C_{B2} [see Fig. 4(b)], allowing another twofold reduction for the switches on the right plate of C_{B2}. Third, we wish



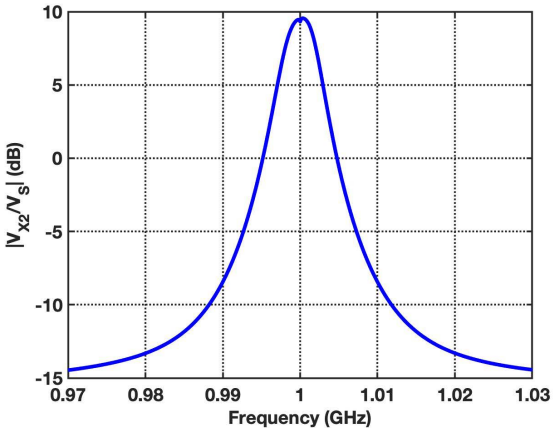
(a)



(b)

	Bank1	Bank2
Unit Capacitor (pF)	100	25
Switch Width (μm)	30.4	7.2
Rejection at 23-MHz offset (dB)	15.6	7.5
Output Voltage Swing (mV_{pp})	273	263

(c)



(d)

Fig. 4. (a) Two eight-path banks placed around the first two gain stages of the receiver, (b) switch sharing between the two banks at X_1, (c) design parameters and performance of blocker rejection banks for GSM, and (d) its frequency response for $f_{\mathrm{LO}} = 1$ GHz.

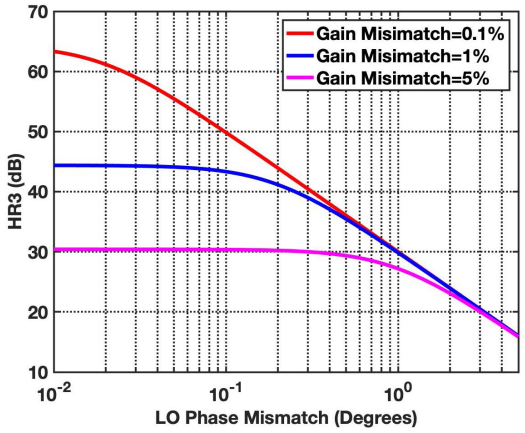


Fig. 5. Third-harmonic rejection versus phase mismatch for different values of gain mismatch.

to attenuate a 0-dBm blocker at a 23-MHz offset by at least 20 dB before it reaches the downconversion mixers. From these points emerge the design values shown in Fig. 4(c). Note that the moderate voltage swings at X_1 and X_2 afford a fairly linear chain. Fig. 4(d) plots the simulated frequency response from V_S to V_{X2} indicating a rejection of 23.06 dB at a 23-MHz offset.

We should remark that out-of-band linearity, e.g., IP3, is greater in mixer-first receivers [10]–[12] but at the cost of NF, power, and RF bandwidth. The measured values are presented in Section V and benchmarked in Table I.

C. Harmonic Rejection

As mentioned in Section II, the wide RF bandwidth of the proposed receiver demands that harmonic blockers be rejected by a large factor. This is particularly necessary for the standards up to about 2 GHz. We assume that such blockers are negligible for the 5-GHz Wi-Fi as the bands around 10 and 15 GHz are relatively quiet.

Harmonic-reject mixers (HRMs) have been studied extensively [19]–[23]. The principal challenge facing these structures stems from gain and phase mismatches. For the former, it is possible to reject the harmonics in two stages so that the gain mismatches multiply [19]–[21]. The latter can be corrected by digital adaptive interference cancellation in the digital BB [19] or by "brute-force calibration" [22], but the calibration suppresses either the third or the fifth harmonic and not both.

To appreciate the severity of phase mismatch, let us consider the rejection of the third harmonic in an eight-phase HRM [19]

$$\mathrm{HR3} = \frac{\sin^2(\pi/8)}{9\sin^2(3\pi/8)\left[(\sigma_A/12)^2 + (\sigma_\phi/4)^2\right]} \tag{6}$$

where σ_A and σ_ϕ denote the standard deviations of the gain and phase mismatches, respectively. Fig. 5 plots HR3, revealing that a rejection of, for example, 60 dB with a gain mismatch of 0.1% is possible only if $\sigma_\phi < 0.025°$. For a carrier frequency of 2 GHz, this translates to $\sigma_\phi < 35$ fs. Similar constraints apply to the fifth harmonic as well. This extremely tight bound poses daunting challenges in the generation and distribution of LO phases.

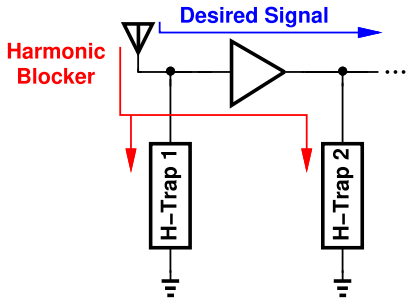


Fig. 6. Concept of H-traps.

Our proposed harmonic rejection method follows a "divide-and-conquer" principle and implements several *independent* mechanisms, each providing some rejection. As illustrated conceptually in Fig. 6, we surmise that narrowband grounded impedances tied to the signal path can act as "harmonic traps" (H-traps), suppressing the blockers in different stages. Thus, the matching requirements of the final HRMs are relaxed by the product of the traps' rejections.

The H-traps in Fig. 6 must nonetheless satisfy certain conditions. First, they must negligibly affect the desired signal. Second, their center frequency must be precise and tunable, pointing to realization based on N-path filters. We propose the transistor-level design of these traps in Section IV.

The overall receiver architecture is shown in Fig. 7. Channel-selection filtering for different standards is performed primarily within the TIA by programmable capacitors and resistors. This eases the linearity required of the succeeding stages in the presence of in-band interferers. In addition to the design elements developed thus far, the RX also employs N-path filter B_3, feedback capacitors C_{F1}–C_{F3}, and "hold" capacitors C_{H1}–C_{H3}. The role of these components is described in Section IV.

IV. Proposed Circuit Design Techniques

A. Problem of Input Matching

Recall from Fig. 2 that the translational Miller effect of R_{F1} provides input matching. However, since the TIA includes channel-selection filtering, the loop gain falls near the edge of the channel bandwidth, degrading S_{11}. This effect can be formulated with the aid of the equivalent BB model shown in Fig. 8(a). Here, the amplifier models the BB equivalent of the first two RF stages and mixers, the first BB stage, and the two inner feedback loops, i.e., R_{F2}, C_{F2}, R_{F3}, and C_{F3} in Fig. 7. This TIA contains a pole whose frequency is half of the CBW, e.g., $\omega_0 = 2\pi(100\ \mathrm{kHz})$ for GSM. We write Z_{in} as

$$\begin{aligned} Z_{\mathrm{in}} &= \frac{R_{F1}}{1 + \frac{A_0}{1+\frac{s}{\omega_0}}} \\ &= \frac{1+\frac{s}{\omega_0}}{\frac{s}{\omega_0} + 1 + A_0} R_{F1}. \end{aligned} \tag{7}$$

The zero in Z_{in} causes an inductive behavior that begins to manifest itself as the frequency approaches ω_0. Noting that $(1 + A_0)R_S = R_{F1}$, we can write S_{11} at $s = j\omega_0$ as

$$\begin{aligned} S_{11} &= \frac{Z_{\mathrm{in}} - R_S}{Z_{\mathrm{in}} + R_S} \\ &= j\frac{R_{F1} - R_S}{j(R_{F1} + R_S) + 2R_{F1}}. \end{aligned} \tag{8}$$

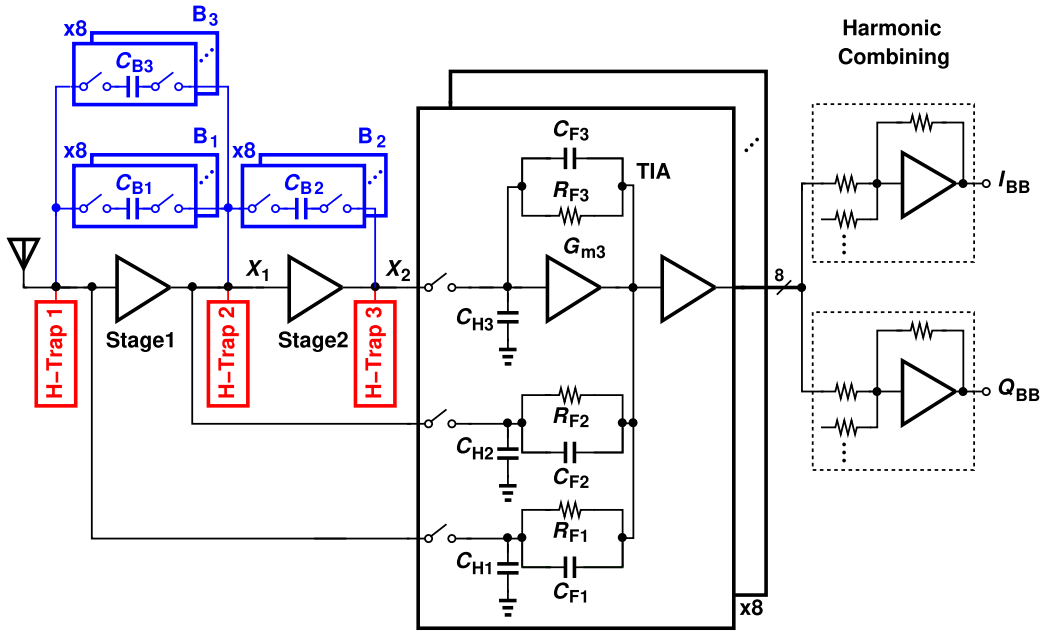
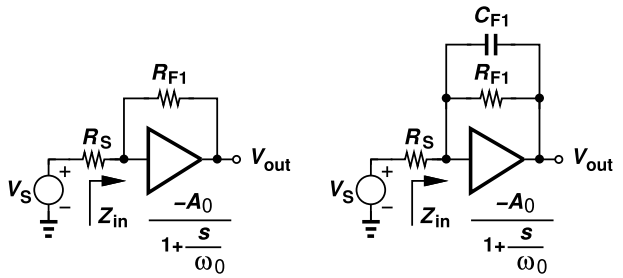


Fig. 7. Proposed receiver architecture.



(a) (b)

Fig. 8. (a) Single-pole amplifier with the resistive feedback and (b) addition of C_{F1} to introduce a zero.

If $R_{F1} \gg R_S$

$$|S_{11}|^2 = \frac{1}{5} \equiv -7 \text{ dB}. \tag{9}$$

This issue can be resolved by adding a zero to the loop, e.g., by placing C_{F1} in parallel with R_{F1}, as shown in Fig. 8(b). We now rewrite (7) as

$$Z_{\text{in}} = \frac{1+\frac{s}{\omega_0}}{\frac{s}{\omega_0}+1+A_0} \cdot \frac{R_{F1}}{R_{F1}C_{F1}s+1} \tag{10}$$

recognizing that $R_{F1}C_{F1} = 1/\omega_0$ eliminates the zero at ω_0. This simple modification provides a low $|S_{11}|$ for a much wider frequency range. Note that the parasitics of C_{F1} are upconverted and do not degrade the RF signal path.

It is important not to confuse the TIA and op amp bandwidths. We should remark that the (open-loop) op amp bandwidth remains at its maximum for different CBWs, providing a high rejection at large frequency offsets. The cancellation stipulated above is achieved by simply programming C_{F1} in tandem with C_{F3}. The feedback resistors are constant.

Fig. 9 plots the simulated input return loss of the receiver for a GSM channel before and after C_{F1} is added. We observe that $|S_{11}|$ is < -10 dB across 145 kHz in the former case and across 13 MHz in the latter. This pole–zero cancellation is relatively robust with respect to mismatches. As shown in Fig. 9, a 20% mismatch still guarantees an S_{11} of better than -15 dB.

An unintended consequence of the feedback topology in Fig. 8(a) is that the closed-loop bandwidth, B_c, is equal to $2\omega_0$ rather than ω_0, dictating a twofold increase in the TIA capacitors. This point can be seen by noting that: 1) B_c is given by ω_0 times one plus the open-loop gain and 2) the loop gain, $[R_S/(R_S+R_{F1})]A_0$, is approximately equal to unity. Alternatively, in Fig. 8(a), we have

$$\begin{aligned}\frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{Z_{\text{in}}}{Z_{\text{in}}+R_S} \cdot \frac{-A_0}{1+\frac{s}{\omega_0}} \\ &= \frac{-R_{F1}A_0}{R_S\left[\left(1+\frac{R_{F1}}{R_S}\right)\frac{s}{\omega_0}+\frac{R_{F1}}{R_S}+A_0+1\right]}.\end{aligned} \tag{11}$$

Since $R_{F1} = (A_0+1)R_S$, the pole frequency is given by $2(A_0+1)\omega_0/(A_0+2) \approx 2\omega_0$.

Interestingly, C_{F1}, added in Fig. 8(b) for input matching, also resolves this issue. With the pole–zero cancellation in (10), we have $Z_{\text{in}} = R_{F1}/(s/\omega_0+1+A_0)$, and hence, from (11)

$$\begin{aligned}\frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{R_{F1}}{2R_{F1}+\frac{s}{\omega_0}R_S} \cdot \frac{-A_0}{1+\frac{s}{\omega_0}} \\ &= \frac{R_{F1}}{R_S\left[\frac{s}{\omega_0}+2(1+A_0)\right]} \cdot \frac{-A_0}{1+\frac{s}{\omega_0}}.\end{aligned} \tag{12}$$

The dominant pole is still given by ω_0, halving the CBW. Capacitor C_{F2} plays a similar role.

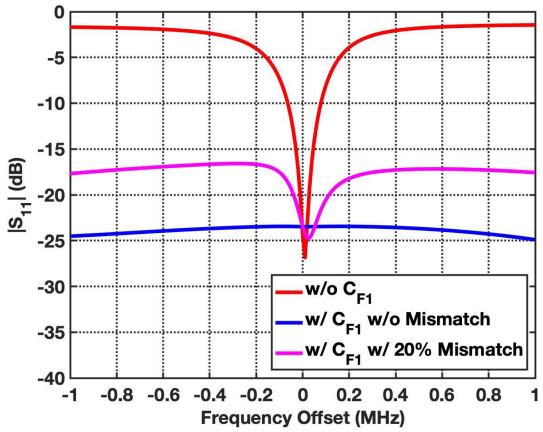


Fig. 9. Input matching with and without C_{F1} for GSM standard.

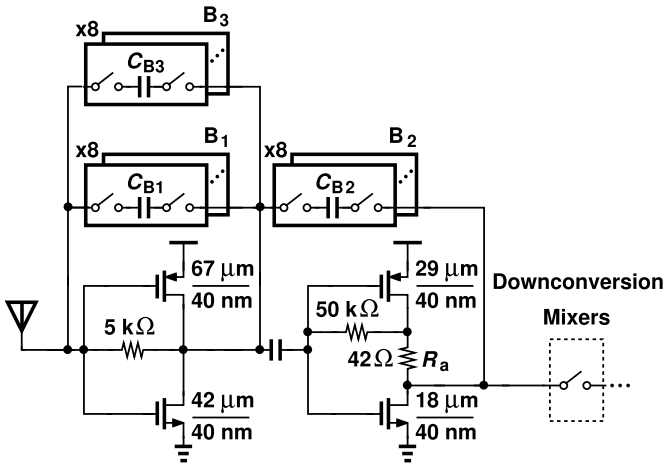


Fig. 10. RF front end realization.

B. RF Front End

The low-noise amplifier and the transconductance stage are realized as self-biased inverters (see Fig. 10), drawing bias currents of 7.8 and 2.8 mA, respectively. Resistor R_a provides a level shift of about 120 mV, so as to provide a proper common-mode (CM) level for the PMOS transistors in the BB TIAs. The cascade provides an open-loop voltage gain of 33 dB with an NF ranging from 1 to 1.4 dB across a bandwidth of 400 MHz to 6 GHz with B_1 and B_2 OFF. The simulated in-band input 1-dB compression point is -37.8 dBm.

As explained in Section III, N-path filter banks B_1 and B_2 reject strong, out-of-band blockers for cellular bands. Each consists of eight branches that are driven by LO phases having a 12.5% duty cycle. We have $C_{B1} = 100$ pF and $C_{B2} = 25$ pF.

Enabled for CBWs greater than 40 MHz, B_3 improves the stability and the RX frequency response. This phenomenon is analyzed in Section IV-G. In this bank, $C_{B3} = 400$ fF.

The downconversion mixers in Fig. 10 employ NMOS switches with $W/L = 7.2\ \mu$m/30 nm and are driven by a 12.5% duty cycle.

C. Harmonic Traps

Recall from Section III that the H-traps must provide a low impedance at the higher harmonics of the LO and, hence, shunt harmonic blockers to the ground. As illustrated in Fig. 11(a), this is accomplished by attaching to the signal path a feedback amplifier whose open-loop transfer function, $H(s)$, exhibits a null at f_{LO} and a peak at $3f_{LO}$. The Miller multiplication of C_F, thus, yields a low impedance at $3f_{LO}$ without affecting the desired signal.

We surmise that the amplifier itself can be implemented as a common-source (CS) stage having a load impedance, Z_{L1}, that exhibits the same behavior as $|H|$ in Fig. 11(a) [see Fig. 11(b)]. We now approximate Z_{L1} by a PMOS load embedded in a feedback loop that provides a *peak* equal to A_0 at f_{LO} and a *null* at $3f_{LO}$ [see Fig. 11(c)]. That is, Z_{L1} is equal to $(A_0 g_{m2})^{-1}$ at f_{LO} and r_{o2} at $3f_{LO}$. The former value ensures a sufficiently *low* gain for the Miller multiplication of C_F

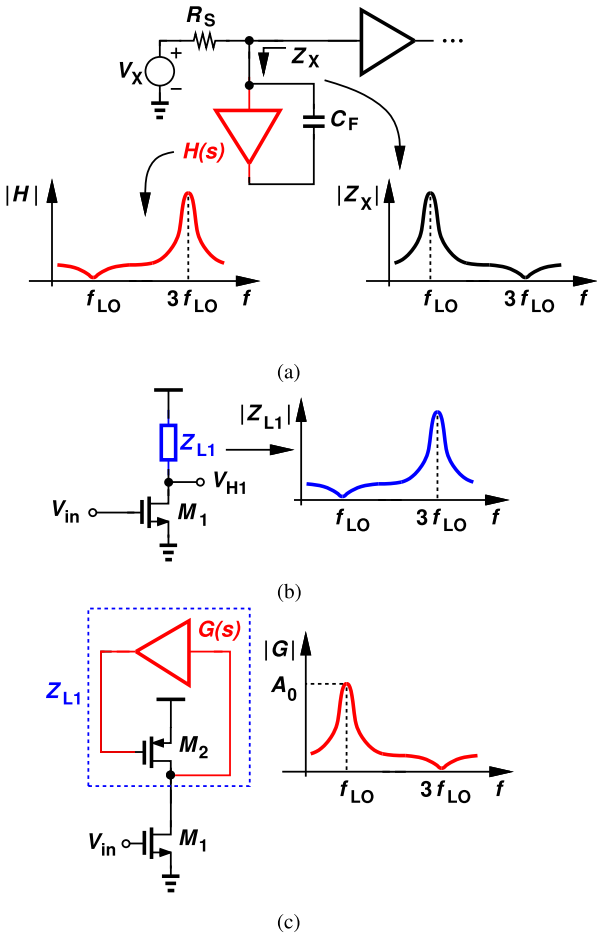


Fig. 11. (a) Concept of building an H-trap, (b) implementation of harmonic amplifier, and (c) implementation of the load in the harmonic amplifier.

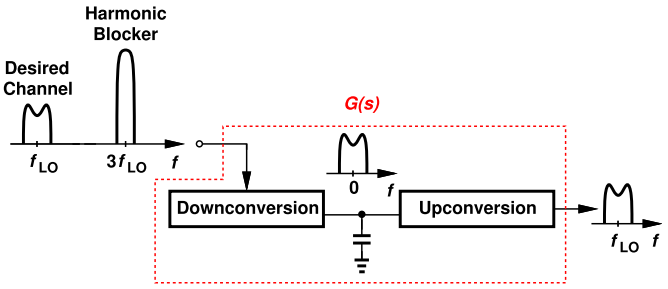


Fig. 12. Implementation of $G(s)$ based on translational circuits.

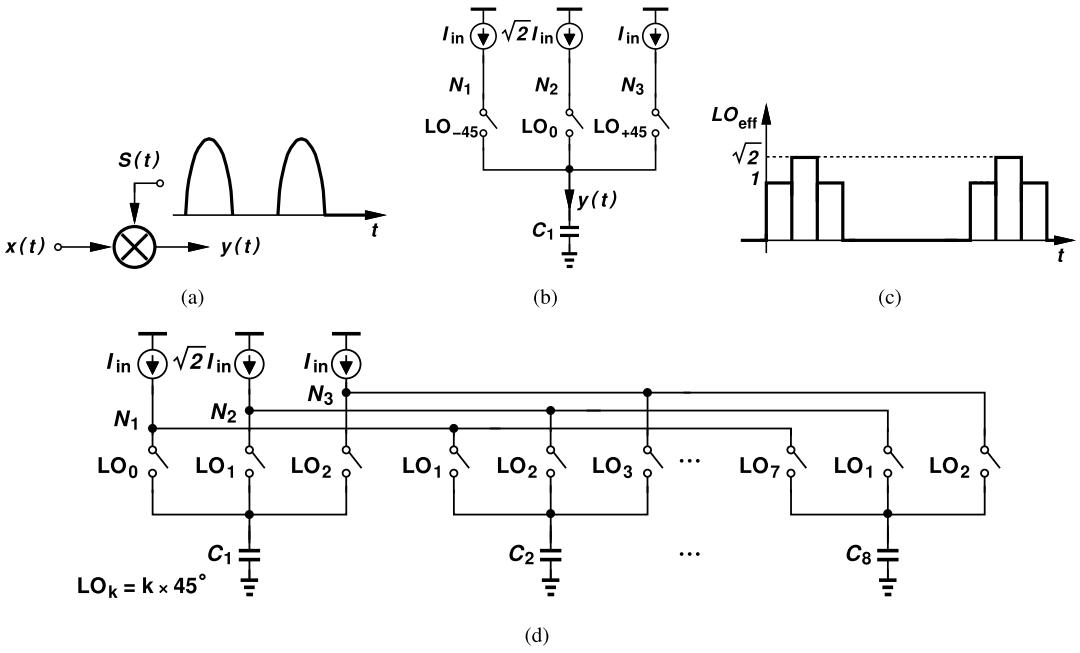


Fig. 13. (a) Conceptual half-sine mixer, (b) its implementation using nonoverlapping LOs, (c) half-sine approximation realized by nonoverlapping LOs, and (d) eight-phase implementation of the half-sine mixer.

in the desired band, and the latter yields a voltage gain of $g_{m1}(r_{o1}||r_{o2})$ for the CS stage at $3f_{\rm LO}$. The challenge, thus, reduces to synthesizing $G(s)$ such that its peak and null frequencies are precise and programmable. This is possible if a translational circuit downconverts only the desired signal [and not the harmonic blocker(s)] and upconverts the results to a center frequency of $f_{\rm LO}$ (and not to other harmonics). Fig. 12 illustrates the concept.

In order to benefit from N-path filters in the design of $G(s)$, we introduce a new concept called "half-sine mixing." As illustrated in Fig. 13(a), suppose that an analog signal $x(t)$ is mixed with a half-rectified sine wave, $S(t)$. The Fourier series of $S(t)$ reads

$$S(t) = 0.5\sin(\omega t) + \sum_{n=1}^{\infty} \frac{\cos[2(n-1)\omega t] - \cos[2(n+1)\omega t]}{(2n-1)\pi}. \tag{13}$$

An important observation is that $S(t)$ contains only the fundamental and even harmonics. The mixing action, therefore, downconverts only such components in $x(t)$, a key enabler of our proposed rejection technique.

Next, we approximate half-sine mixing by three weighted-sum mixers, as shown in Fig. 13(b). Three LO phases at $-45°$, $0°$, and $+45°$ chop $I_{\rm in}$, $\sqrt{2}I_{\rm in}$, and $I_{\rm in}$, respectively, synthesizing the effective LO waveform shown in Fig. 13(c). This result resembles the rectified sine of Fig. 13(a) and exhibits the fundamental but not the third and fifth harmonics. The output, $y(t)$, must now be upconverted, so as to mimic the illustration in Fig. 12. This can be accomplished efficiently by noting that the switches in Fig. 13(b) upconvert the BB voltage across C_1 to $f_{\rm LO}$, producing the desired RF signal at N_1, N_2, and N_3. Nonetheless, to suppress upconversion to higher harmonics, an eight-phase arrangement is necessary [see Fig. 13(d)]. Here, the voltages at N_1, N_2, and N_3 are free

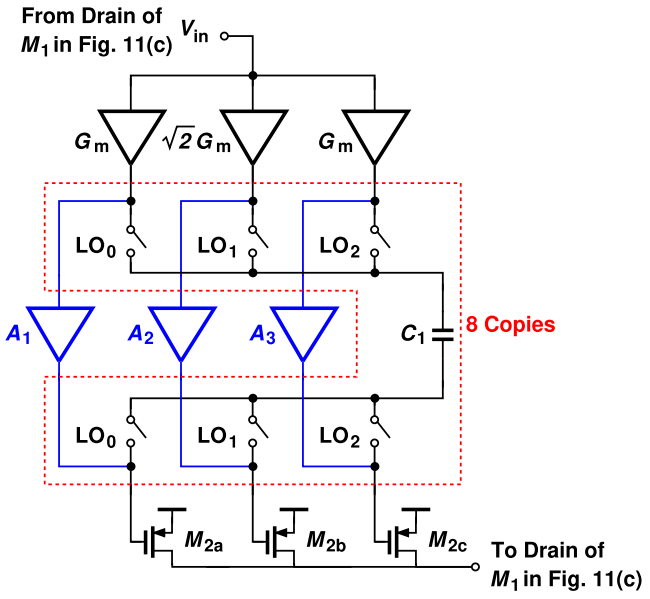


Fig. 14. Eight-phase realization of half-sine mixer utilizing the Miller effect and feedforward zero.

from odd harmonics and can be simply summed; the resulting circuit would act as $G(s)$ in Figs. 11(c) and 12.

The principal difficulty in the realization of Fig. 13(d) is that the switch resistance greatly limits the amount of harmonic blocker rejection. As with blocker rejection concepts developed in Section III, we surmise that the Miller effect and the feedforward zero can be exploited here as well to alleviate this issue. We, therefore, place the capacitors and the switches around voltage amplifiers, as depicted in Fig. 14. Here, the G_m stages produce the weighted input currents, and the outputs are summed by M_{2a}, M_{2b}, and M_{2c}. Note that M_{2a}, M_{2b}, and

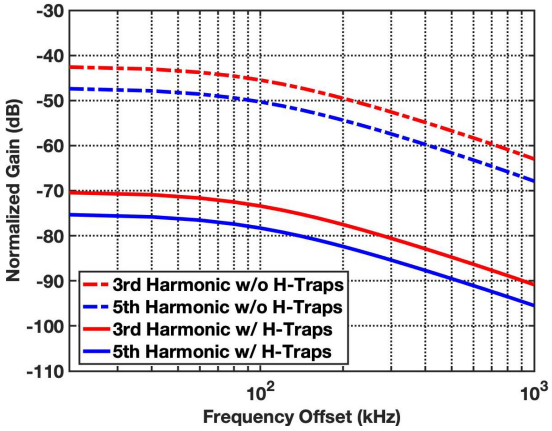


Fig. 15. Simulated response of receiver with and without H-traps for GSM with a 1-GHz LO.

M_{2c} are the distributed version of M_2 in Fig. 11(c) with their drains connected to the output of the harmonic amplifier, i.e., the drain of M_1.

Our "divide-and-conquer" approach to harmonic rejection affords significant robustness against phase and gain mismatches. Fig. 15 plots the simulated harmonic response of the receiver with and without the three H-traps shown in Fig. 7. A gain mismatch of 2% is added to the BB harmonic combiner, limiting the rejection to 40 dB. We observe that the rejection of the third and fifth harmonics is improved by 27.8 and 27.9 dB, respectively.

In order to evaluate the efficacy of our H-trap technique with respect to phase mismatch, we ran Monte Carlo simulations for 200 samples. The results are depicted as histograms in Fig. 16 for a standard deviation of 220 fs. The average HR3 without H-traps is 51.96 dB [see Fig. 16(a)]. With the H-traps turned on, the harmonic rejection is increased by more than 19 dB, allowing it to reach 71.27 dB [see Fig. 16(b)]. A similar trend is observed for HR5. In summary, the H-traps improve the harmonic rejection by more than 27 dB in the case of gain mismatch and 19 dB in the case of phase and gain mismatches. It is also instructive to study the effect of H-traps on even harmonics. Half-sine mixing yields a finite rejection even in the ideal case. Monte Carlo simulations of the receiver suggest that our proposed method increases HR2 from 57 to 66 dB and HR4 from 65 to 74 dB.

One may wonder whether the proposed stage in Fig. 13(b) can also be applied to the main signal path. While this is possible, such an approach would limit the receiver's harmonic rejection to that of this stage. As a "shunt" path, on the other hand, the circuit's rejection limit does not constrain that of other stages.

D. Translational Virtual Ground

Recall from Section III that the receiver incorporates multiple resistive feedback paths to lower the node impedances. An undesirable phenomenon in the multi-loop architecture of Fig. 7 relates to the loading effect presented to G_{m3} by R_{F1}, R_{F2}, and R_{F3}. We expect that increasing these resistors eases this issue but at the cost of compromising the input match and the virtual grounds at X_1 and X_2. The following analysis indicates that, ultimately, G_{m3} must bear the tradeoff

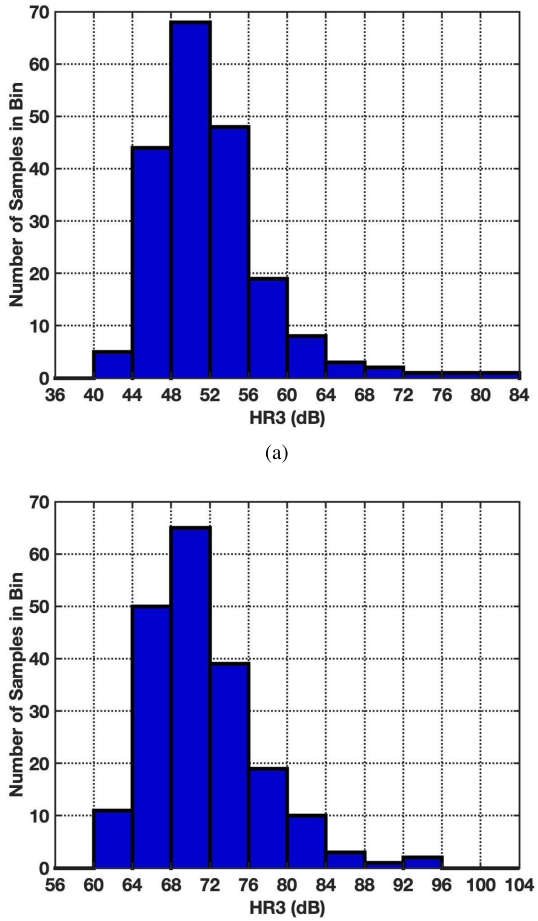


Fig. 16. Monte Carlo harmonic rejection simulation results for 1-GHz LO with 200 samples (a) without H-traps and (b) with H-traps.

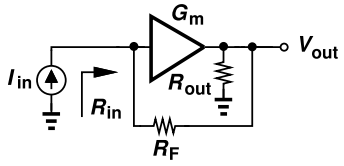


Fig. 17. Amplifier with resistive feedback.

and consume high power to drive these resistors. Consider the simplified loop shown in Fig. 17, where R_{out} denotes the output resistance of the transconductance stage. We have

$$\frac{V_{\text{out}}}{I_{\text{in}}} = \frac{R_{\text{out}} - G_m R_{\text{out}} R_F}{1 + G_m R_{\text{out}}} \approx \frac{-G_m R_{\text{out}} R_F}{1 + G_m R_{\text{out}}} \tag{14}$$

if $|G_m R_F| \gg 1$. Also,

$$R_{\text{in}} = \frac{R_{\text{out}} + R_F}{1 + G_m R_{\text{out}}}. \tag{15}$$

The input resistance can be lowered by decreasing R_F, approaching a lower bound of $1/G_m$, but at the cost of closed-loop gain. Alternatively, we can increase G_m by burning

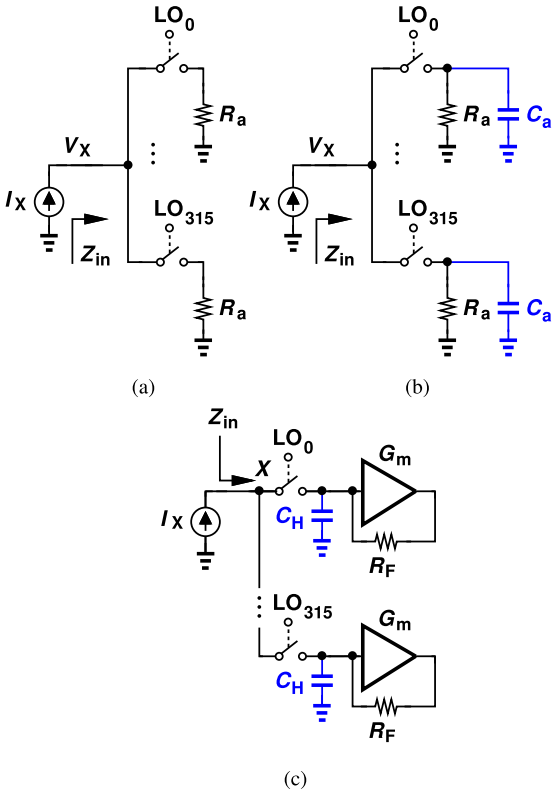


Fig. 18. (a) Memoryless eight-path circuit with resistive load, (b) eight-path circuit with resistive and capacitive loads, and (c) its counterpart using TIAs.

higher power.[1] With four differential G_{m3} blocks necessary for our receiver, the power consumption problem proves serious.

We propose herein the concept of the "translational virtual ground" as a means of alleviating this issue. We begin with the memoryless N-path circuit in Fig. 18(a), and note that $Z_{\text{in}} = V_X/I_X = R_a$. In Fig. 18(b), on the other hand, the parallel combination of R_a and C_a is upconverted, yielding

$$Z_{\text{in}} = \frac{R_a}{8[1 + jR_aC_a(\omega - \omega_{\text{LO}})]} \tag{16}$$

if $T_{\text{LO}}/2\pi \ll R_aC_a$. Selecting $1/(2\pi R_aC_a)$ much greater than the CBW, we have $Z_{\text{in}} \approx R_a/8$. We can intuitively explain this eightfold reduction in the time domain as follows. Let us assume in Fig. 18(b) that the input frequency is close to f_{LO} such that I_X changes negligibly while one switch is turned on. The charge delivered to the corresponding capacitor is, thus, equal to $I_X(T_{\text{LO}}/8)$. The charge drained from the capacitor in one LO cycle is approximately equal to $(V_X/R_a)T_{\text{LO}}$ if $R_aC_a \gg T_{\text{LO}}$. In the steady state, therefore, the charge delivered by I_X must be equal to that absorbed by R_a; $I_X(T_{\text{LO}}/8) \approx (V_X/R_a)T_{\text{LO}}$, and hence, $V_X/I_X \approx R_a/8$. A more general analysis in the frequency domain is provided in Appendix II.

Next, we apply this idea to the feedback network around an amplifier, as illustrated in Fig. 18(c). The same reasoning suggests that the input impedance is now approximately equal to $(1/G_m)/8$, as if G_m were boosted by a factor of 8. We call node X a "translational virtual ground." We can, therefore, choose a high value for R_F to avoid loading the amplifier and yet achieve a low impedance at X. This technique reduces the power consumption of the BB TIAs by about a factor of 8. We point out that the role of a grounded capacitor at the TIA input has been studied extensively (see [8], [9], [19], and [28]–[30]). However, the use of C_{H1} and C_{H2} in Fig. 7 is, to the best of our knowledge, a new concept that introduces two more low-impedance nodes in a nested feedback architecture and maintains high in-band linearity and low NF with low power consumption.

[1]The value of G_m can also be raised by preceding this stage by a voltage amplifier but at the cost of stability and, hence, bandwidth.

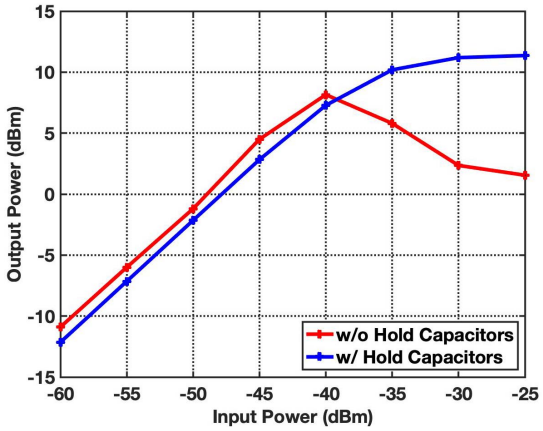


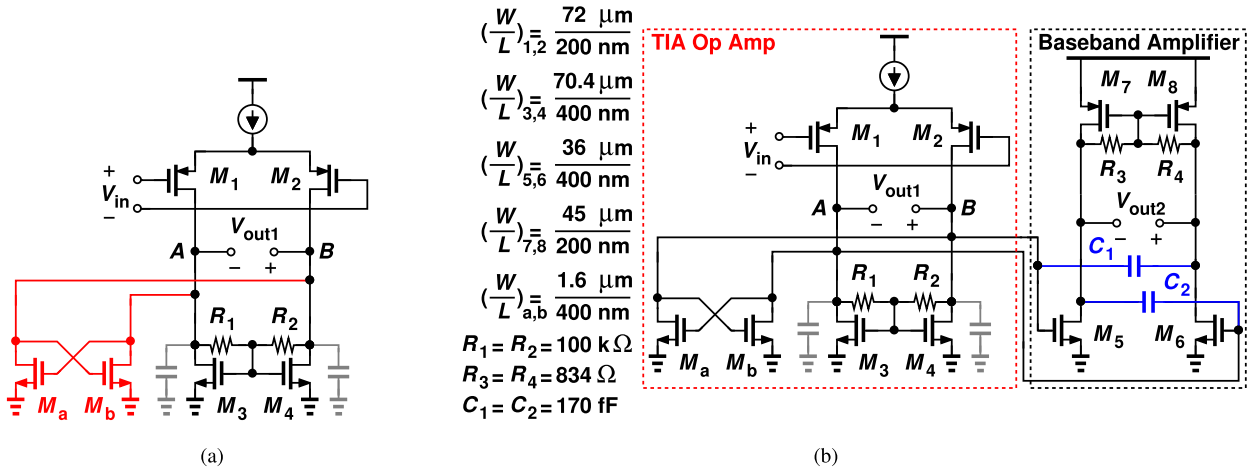
Fig. 19. Simulated 1-dB compression point at the output of the TIA with and without hold capacitors.

The proposed RX in Fig. 7 incorporates translational virtual grounds at the main input and at X_1 and X_2. To appreciate the efficacy of this method, we consider two cases: 1) $C_{H1} = C_{H2} = C_{H3} = 0$ and 2) $C_{H1} = C_{H2} = C_{H3} = 3.2$ pF. We also choose $R_{F1} = 45$ kΩ (for 50-Ω input matching), and $R_{F2} = R_{F3} = 15$ kΩ. Fig. 19 plots the simulated compression characteristics of the two cases at 1 GHz, revealing a 5-dB improvement in linearity. We should also remark that the voltage swing at X_2 in Fig. 2 drops by 17 dB in the presence of these "hold" capacitors.

It is also interesting to consider the current delivery required of the op amp in the presence of a 0-dBm blocker. Simulations reveal a peak of about 3.9 mA flowing through the three feedback networks in Fig. 7, most of which is absorbed by the translational virtual ground capacitors, C_{H1}–C_{H3}. In fact, each of the eight BB op amps needs to provide a peak current of 0.48 mA.

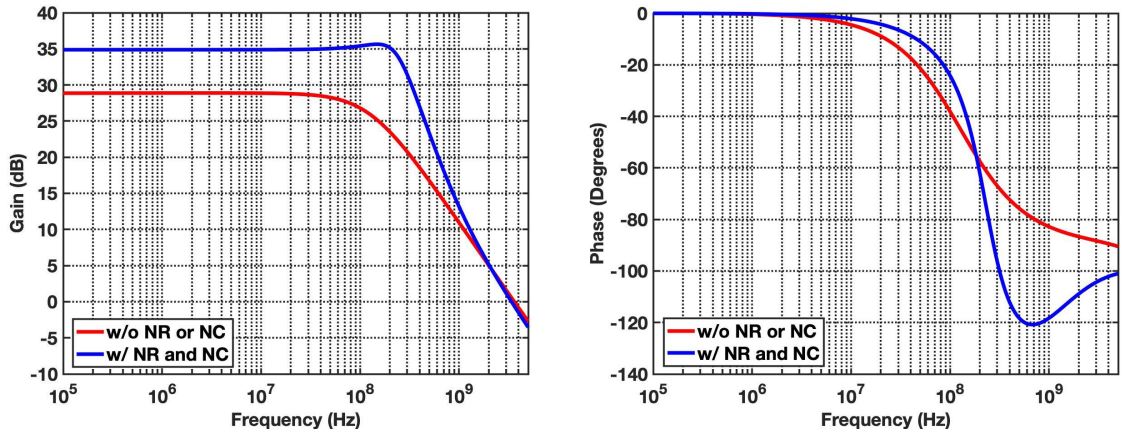
E. Proposed Op Amp Topology

The op amp forming the core of the BB TIAs plays a critical role in the overall performance. To accommodate a Wi-Fi CBW of 160 MHz with 256 QAM, we wish to maintain low-voltage swings at node X_2 in Fig. 7 even for the alternate-adjacent channel. That is, the op amp must maintain a high gain up to about 400 MHz. To avoid the need for frequency compensation, we prefer a one-stage op amp within each TIA. Even though the translational virtual ground concept eases the loading effect presented by the feedback resistors, the op amps must still drive three feedback paths while maintaining a high gain.



(a) (b)

Fig. 20. (a) Op amp with negative resistance at its output and (b) addition of negative capacitance and BB amplifier.



(a) (b)

Fig. 21. Open-loop frequency response of one-stage op amp [(a) gain, and (b) phase] before and after two modifications (with loading due to R_{F1}–R_{F3} in Fig. 7 included) (NR: negative resistance and NC: negative capacitance).

A serious difficulty arises from the finite output resistance of the op amps. From the simplified circuit shown in Fig. 17, one can readily prove that R_{in} is minimized, and V_{out}/I_{in} is maximized if $R_{out} \to \infty$. This issue is alleviated through the use of negative resistance at the op amp output, as illustrated in Fig. 20(a). Transistors M_a and M_b partially cancel the output resistance of M_1–M_4, resistors R_1 and R_2, and feedback resistors R_{F1}–R_{F3} in Fig. 7. To ensure that M_a and M_b do not cause latch-up, we must have $g_{mab}R_{out} < 1$, where $R_{out} \approx r_{o1}||r_{o3}||R_1||R_{F1}||R_{F2}||R_{F3}$. In this work, we have chosen $g_{mab}R_{out} \approx 0.5$ to allow a safe margin for PVT variations.

In addition to static errors, the op amp shown in Fig. 20(a) also exhibits bandwidth limitations arising from the transistor capacitances. This, in turn, degrades the quality of the translational virtual grounds in the adjacent or alternate-adjacent channels. To further suppress this effect, we incorporate negative Miller capacitors in the BB chain [see Fig. 20(b)]. With $C_1 = C_2 = 170$ fF, the net capacitance at nodes A and B falls from 370 to 80 fF.

Fig. 21 plots the simulated open-loop frequency response of the one-stage op amp before and after the two modifications.

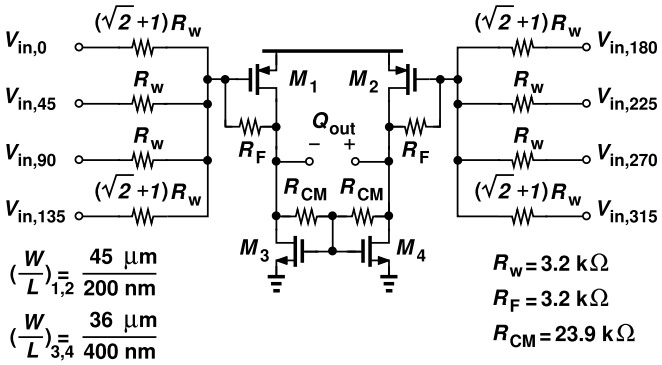
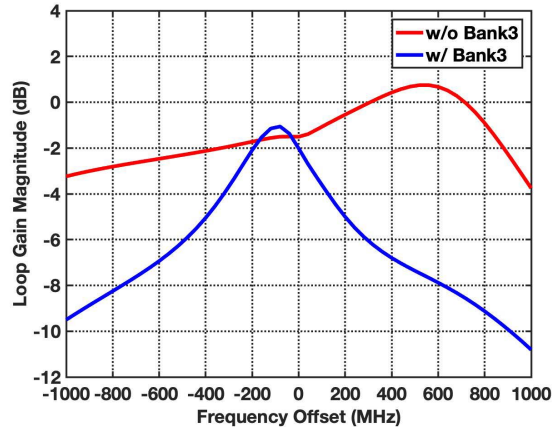
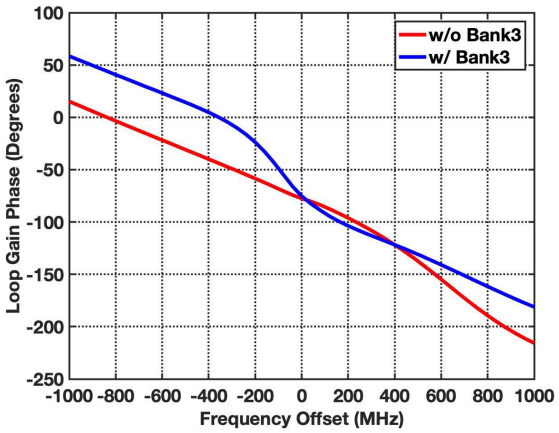


Fig. 22. BB combiner circuit.

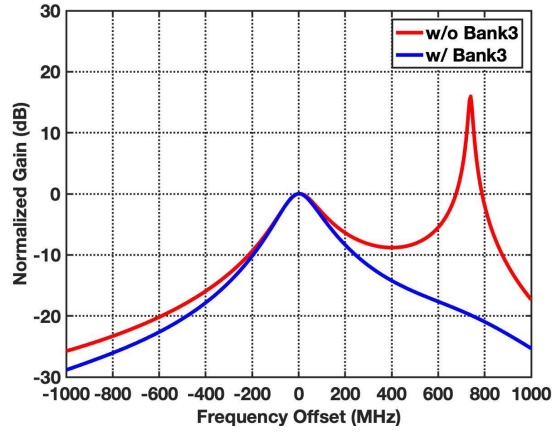
We note that the gain rises by 6 dB and the −3-dB bandwidth by about a factor of 2.3. The op amp draws 1.4 mW. It is beneficial to review the RX chain design process in view of linearity. In Fig. 7, channel selection is provided by the three feedback loops. For in-band linearity and, hence, low-voltage swings along the chain, the op amp must provide sufficient



(a)



(b)



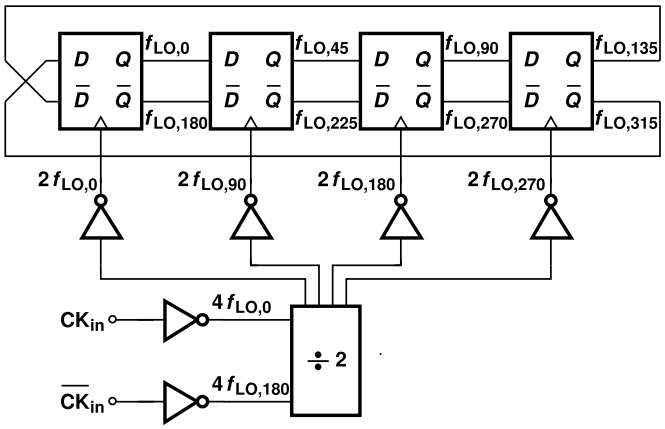
(c)

Fig. 23. (a) Loop gain magnitude of the outermost loop of the receiver, (b) loop gain phase of the outermost loop of the receiver, and (c) response of the receiver with and without B_3 simulated for 6-GHz LO.

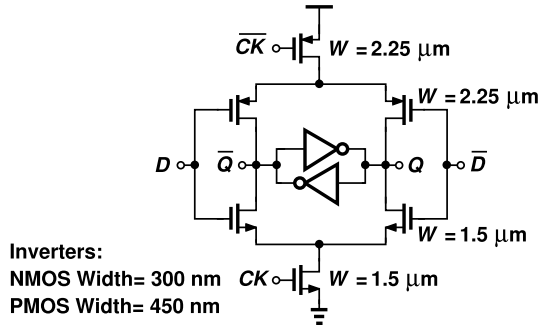
gain. For out-of-band blockers, the RF nodes are of primary concern and are "protected" by Bank 1 and Bank 2.

F. Harmonic Combiner

The receiver generates four sets of differential BB signals that must be combined so as to provide harmonic rejection and deliver I and Q outputs. With 55 dB of voltage gain preceding the combiners, their linearity, especially for 256-QAM signals, becomes critical, calling for negative feedback.



(a)



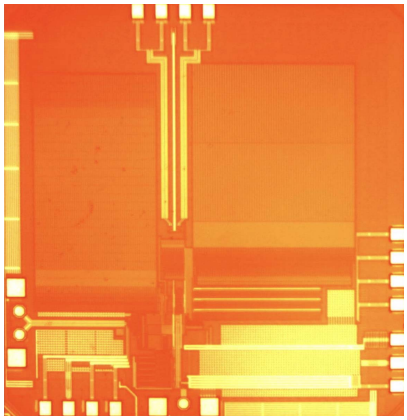
(b)

Fig. 24. (a) LO phase generation and (b) latch circuit used in the ÷2 circuit and the counter. ($L = 30$ nm.)

Fig. 22 depicts the harmonic combiner implementation. A simple pseudo-differential stage with feedback offers a reasonable compromise among noise, nonlinearity, and power consumption. The combining occurs at the virtual grounds, yielding a harmonic rejection accuracy commensurate with the matching of polysilicon resistors. Tracking the bias current of the second stage in Fig. 20(b), M_1 and M_2 achieve a higher linearity than a regular differential pair and consume 0.5 mW.

G. Stability Considerations

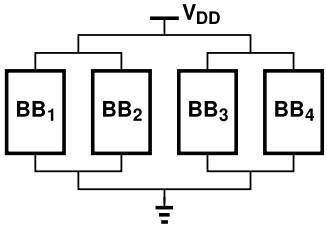
The presence of multiple feedback loops in the proposed receiver of Fig. 7 raises concern about stability and frequency response flatness. This issue is particularly acute for 160-MHz channels as even high-frequency poles in the feedforward and feedback paths can introduce significant peaking in the RX response. We open the outermost loop (which includes R_{F1} and C_{F1}), while the inner loops remain intact. Without the third bank, B_3, in Fig. 7, we obtain the loop transmission magnitude and phase plotted in Fig. 23 for $f_{LO} = 6$ GHz. The loop gain drops to 0 dB at a 700-MHz offset with a phase margin of 5°. To overcome this difficulty, the feedback can be *weakened* as the offset approaches 700 MHz. This is accomplished by reducing the gain of the first RF stage at high offset frequencies by means of a Miller N-path filter, B_3. As depicted in Fig. 23, the loop gain now remains below 0 dB at all frequencies. Fig. 23(c) illustrates the efficacy of this technique in solving the problem of gain peaking while receiving a 160-MHz channel. The experimental results presented in



(a)

RF Amplifiers	9.5 mW
Baseband Amplifiers and Combiners	6.4 mW
H-traps	10.5 mW
LO Phase Generation and Distribution	7.4-28.8 mW
Total	23.3-49.2 mW

(b)



(c)

Fig. 25. (a) Receiver die photograph, (b) receiver power breakdown, and (c) H-tree routing of supply and ground lines for BB stages preceding harmonic combiners.

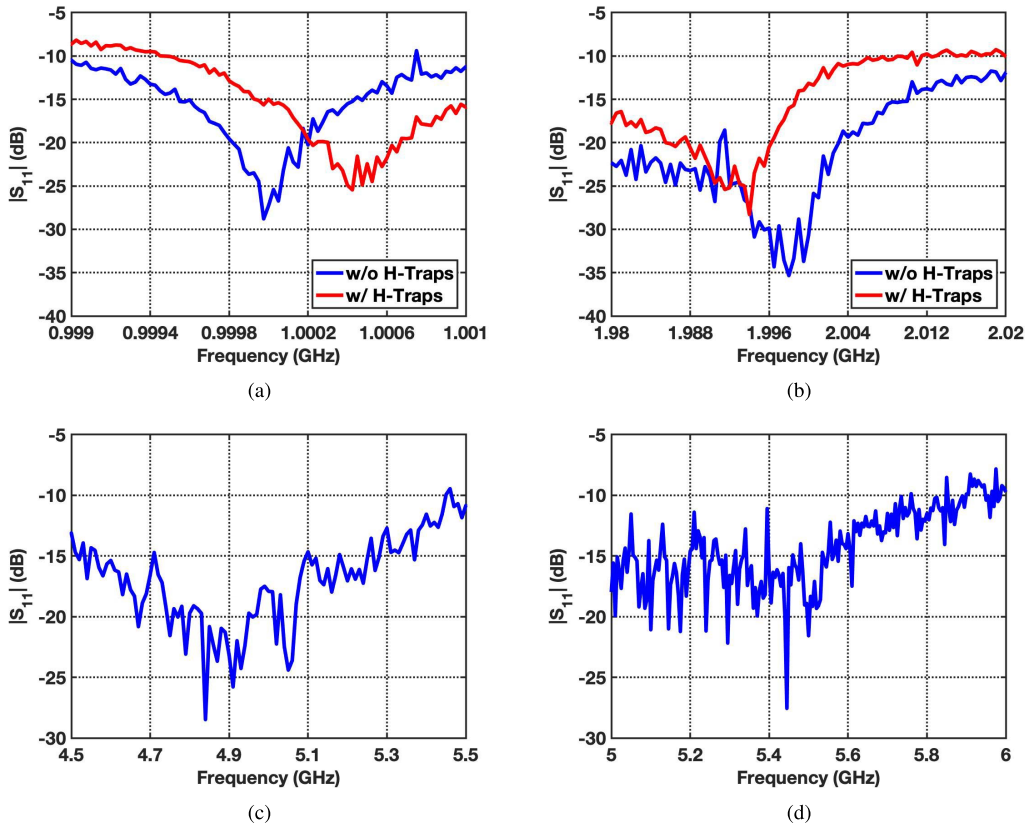


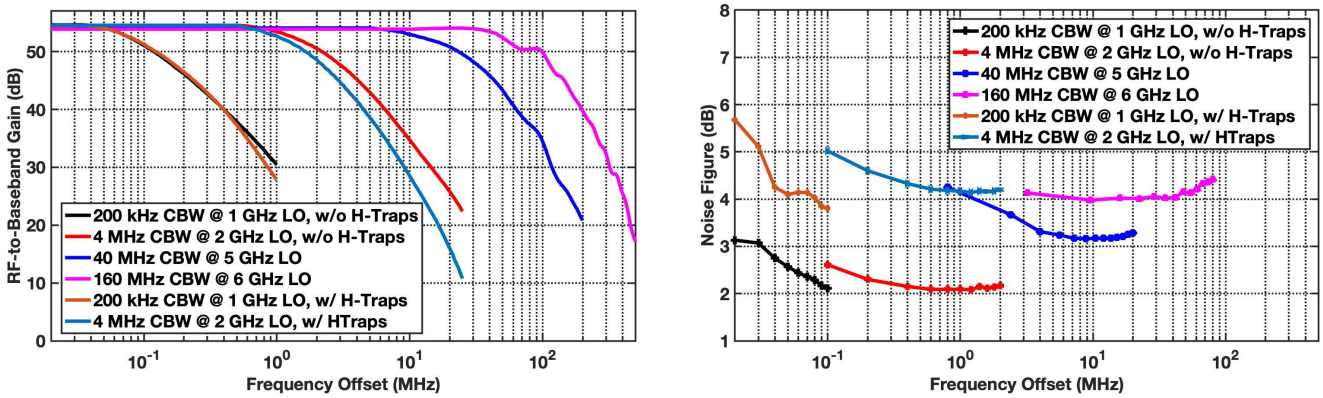
Fig. 26. Input matching measured for (a) 200-kHz CBW around 1 GHz, (b) 4-MHz CBW around 2 GHz, (c) 40-MHz CBW around 5 GHz, and (d) 160-MHz CBW around 5.5 GHz.

Section V also verify that the overall RX response exhibits no peaking. A detailed analysis of stability and frequency response is presented in Appendix III.

H. LO Phase Generation

The receiver relies on eight LO phases with a duty cycle of 12.5% to perform blocker rejection, harmonic rejection, and downconversion. Fig. 24(a) shows the phase generator [16], which consists of a ÷2 stage and four latches forming a ring counter. Each latch within the ÷2 circuit and the counter is realized, as depicted in Fig. 24(b). Following the counter are eight NOR gates that combine their phases and retime the results using the $4f_{LO}$ signals, thus reducing both phase noise and phase mismatches.

The phase generator exhibits a simulated phase noise of −137.5 dBc/Hz at a 1-MHz offset. At 1 GHz, it draws 7.35 and 12.45 mW with harmonic rejection OFF or ON, respectively. At 6 GHz, the power rises to 28.69 mW.



(a) (b)

Fig. 27. (a) RF-to-BB gain and (b) NF for different configurations.

V. Experimental Results

The proposed receiver has been fabricated in TSMC's 28-nm CMOS technology. As shown in Fig. 25(a), the die occupies an area of 1.37 mm × 1.38 mm. Fig. 25(b) summarizes the receiver power breakdown with a 1-V supply.

A critical issue in the RX layout stems from the matching required of the BB stages before harmonic combining occurs. Specifically, voltage drops on the ground and supply lines can lead to mismatches among the stages, degrading the harmonic rejection ratio. This difficulty is alleviated through the use of H-trees for the power lines [see Fig. 25(c)]. Here, BB_j denotes the BB chain consisting of the stages shown in Fig. 20(b).

The receiver performance has been characterized by tens of tests. This section presents the results. The capacitor arrays in various parts of the RX are programmed through a serial bus.

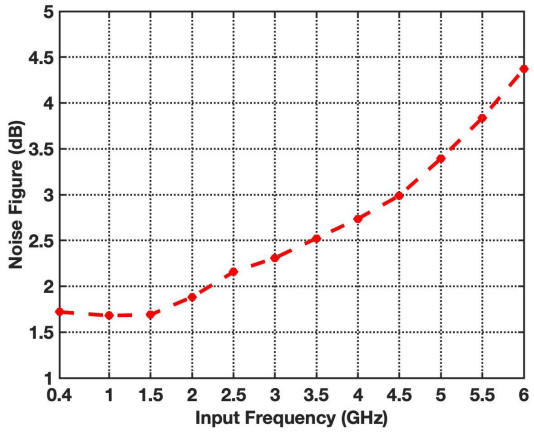


Fig. 28. NF measured over the entire input frequency range.

A. Input Matching, Gain, and Noise Figure Tests

Fig. 26 plots the measured magnitude of S_{11} for different RF channel bandwidths and different frequency bands. For 1- and 2-GHz cellular bands, the effect of H-traps is also illustrated. We observe that $S_{11} < -10$ dB for all CBWs, verifying the efficacy of the approach described in Section IV.

Shown in Fig. 27(a) are the RF-to-BB responses of the receiver for six different configurations: CBW = 200 kHz at 1 GHz, with and without H-traps, CBW = 4 MHz at 2 GHz with and without H-traps, CBW = 40 MHz at 5 GHz, and CBW = 160 MHz at 6 GHz. The gain is about 55 dB.

Fig. 27(b) depicts the NF for the same six configurations. The RX achieves an NF as low as 2.1 dB at 100 kHz around 1 GHz and 2.5 dB around 2 GHz. With the H-traps turned on, the NF raises by 1.6–2.1 dB. The NF in the 5-GHz band is greater than predicted by 2.3 dB because of the LO leakage to the RX input (around −52 dBm) and, hence, a large dc offset in the BB. This dc offset creates an imbalance between the gain experienced in the eight BB paths and degrades harmonic rejection, which results in more noise being folded on the desired BB signal from the higher harmonics of the LO. It is expected that BB offset cancellation lowers this NF. The spot NF has been measured as a function of the carrier frequency and plotted in Fig. 28. To evaluate the lowest NF that the RX can achieve, we have turned off Banks 1 and 2 here.

B. Linearity and Blocker Tests

The RX linearity is first characterized by the third and the second input intercept points, IIP3 and IIP2, respectively. These quantities are measured for four different CBWs and at different carrier frequencies.

The IIP3 is obtained by applying two equal-amplitude tones with a small frequency difference and a variable offset with respect to f_{LO}. Fig. 29 plots the IIP3 as a function of this offset for different scenarios.

The IIP2 is measured in a similar manner, except that the spacing between the tones is chosen equal to 0.8 times the offset frequency so that the second-order intermodulation product falls near the main tones, experiencing the same voltage gain. The results are shown in Fig. 29.

The rejection of blockers is studied as follows. We apply a blocker at a 20-MHz offset around 1 GHz (the most stringent case) and measure the NF as the blocker level increases to 0 dBm. The principal challenge here is that the blocker cannot be supplied by typical RF generators due to their high noise floor (about −152 dBc/Hz). We instead use a 1-GHz crystal

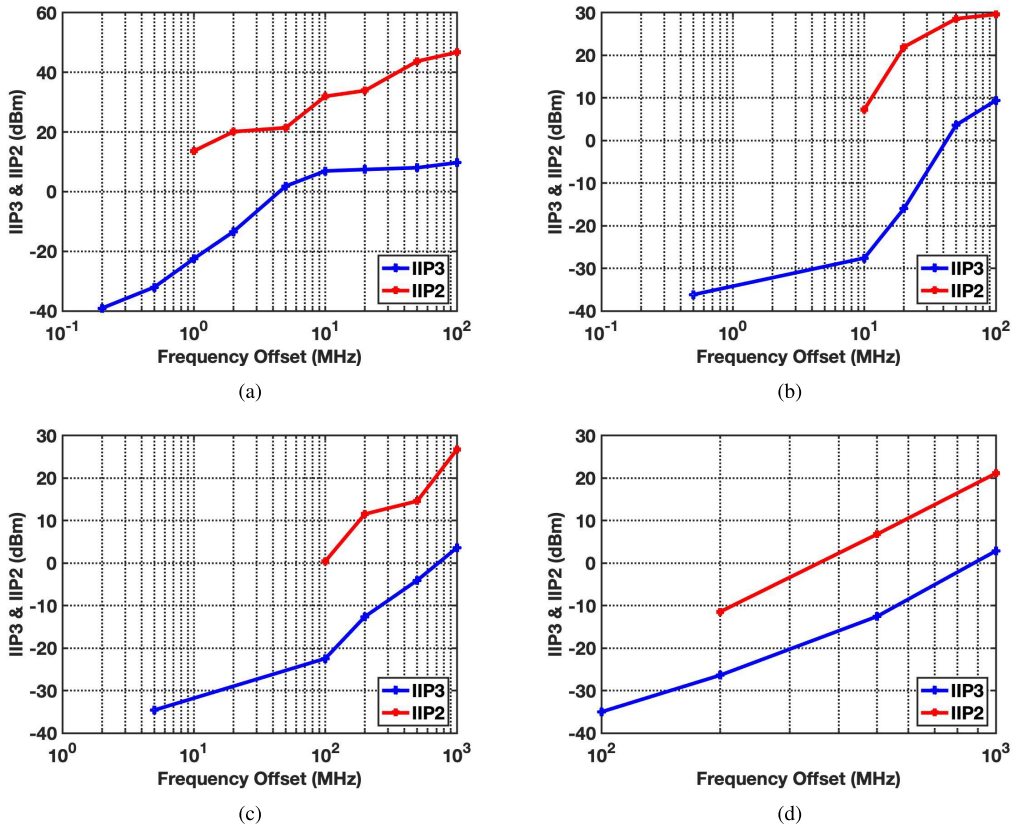


Fig. 29. Linearity test results for (a) 200-kHz CBW around 1 GHz, (b) 4-MHz CBW around 2 GHz, (c) 40-MHz CBW around 5 GHz, and (d) 160-MHz CBW around 5.5 GHz.

TABLE I
RECEIVER PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	[16]	[31]	[10]	[11]	[12]	[22]	[20]	[32]	This work
RF Input	Single-ended	Single-ended	Differential	Differential	Differential	Differential	Single-ended	Single-ended	Single-ended
Input Frequency [MHz]	80-2700	0.2-2000	0.2-8	0.1-2	0.5-2	400-6000	600-3000	500-3000	400-6000
Channel Bandwidth [MHz]	0.35-20	N/A	20	13	260	1-100	0.4-6	40-98	0.2-160
Gain [dB]	38	40	21	16	32.4	70/58[3]	N/A	38-46	54
NF [dB]	2.9	2.1-2.5	2.3-5.4[1,2]	4.1-10.3[2]	5.5	2.4[2,4]/3.1[2,5]	1.8[4]/3[6]	2.5-5	2.1-4.42
0-dBm OB-Blocker NF [dB]	5.1	6.7	4.7[2]	8.1[2]	9.7	10[2,7]/14[2,5]	9[4]/13[6]	9 (–5 dBm)	5.2[4]/7.4[6]
OB-IIP3 [dBm]	10	14	39	44	21	8[7]/3[6]	10	4	9.8/2.8[8]
Harmonic Rejection (HR) [dB] $3f_{LO}/5f_{LO}$	35/45	N/A	N/A	N/A	N/A	70/75	52/54	80	60.5/62.3[9]
EVM (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	–22.1[10]/ –25.2[11]
HR Calibration	N/A	N/A	N/A	N/A	N/A	Yes	No	Yes	No
Power Consumption [mW]	20	68-95	56-290	34-96	25.5-37.2	40	38.8-70	28-31	23-49
CMOS Technology	65 nm	45 nm SOI	45 nm SOI	28 nm	28 nm	28 nm	28 nm	28 nm	28 nm

[1]0.5-6 GHz [2]Balun loss not included [3]Above 3 GHz [4]Low noise mode [5]Standard operation [6]Harmonic rejection mode [7]LNA optimized [8]With B1 and B2 turned off and B3 turned on for channel bandwidths more than 4 MHz with less stringent blocker requirements [9]Reported at 1 GHz for fair comparison with prior art [10]LTE [11]WiFi 6

oscillator with a noise floor of −170 dBc/Hz and subject its output to a printed-circuit notch filter that provides 11 dB of rejection at a 20-MHz offset. Plotted in Fig. 30, the NF begins to climb as the blocker power exceeds −15 dBm, reaching 5.2 dB at 0 dBm when the H-traps are OFF. For the case where both a 0-dBm blocker at a 20-MHz offset and harmonic

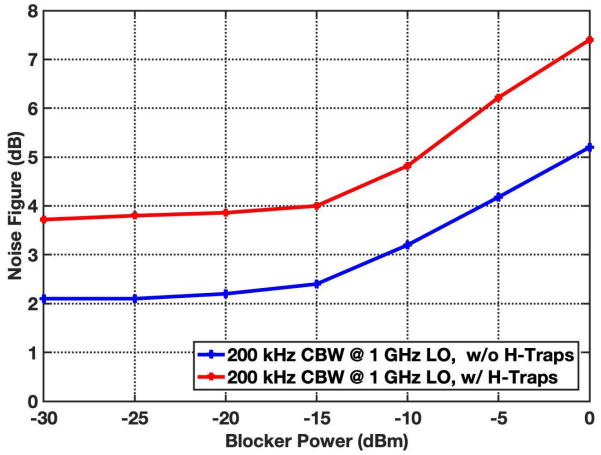


Fig. 30. NF measurement results in the presence of a blocker at a 20-MHz offset.

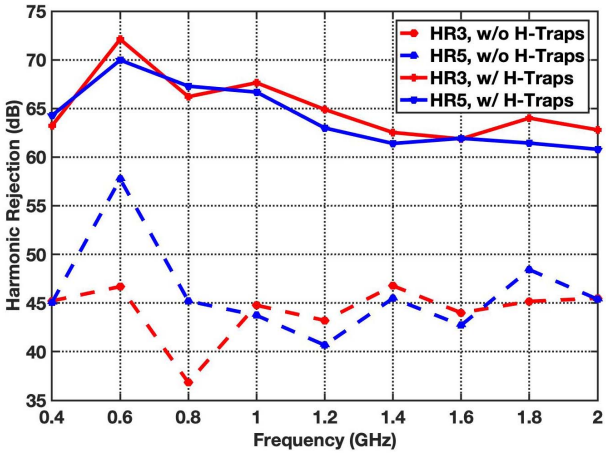


Fig. 31. HR3 and HR5 measured from 400 MHz to 2 GHz with and without H-traps.

blockers are present, we enable the H-traps and observe an NF of 7.4 dB.[2] With a noiseless LO, simulations indicate NF = 1.12 and 1.59 dB in the absence or presence of a 0-dBm blocker, respectively. This suggests negligible compression. The measured NF values, on the other hand, are 2.1 and 5.2 dB, respectively, revealing that reciprocal mixing with the LO phase noise is the principal contributor.

C. Harmonic Rejection Tests

The harmonic rejection tests have been conducted over a range of frequencies from 400 MHz to 2 GHz as the third and fifth harmonics of the LO can potentially fall in busy bands. Plotted in Fig. 31 are HR3 and HR5 before and after the H-traps are turned on. The rejection improves by an average of 18 dB; the performance is ultimately limited by the LO phase mismatches. We should remark that the proposed technique maintains both HR3 and HR5 above 60 dB across the entire frequency range.

In order to demonstrate the low sensitivity of the proposed technique to mismatches, we have measured HR3 and HR5 for ten chips. The results are shown in Fig. 32 for $f_{LO} = 1$ GHz so as to allow a fair comparison with the prior art. The average rejection is about 65 dB.

[2]The lack of low-noise oscillators at higher frequencies precludes this type of measurement at, e.g., 2 GHz.

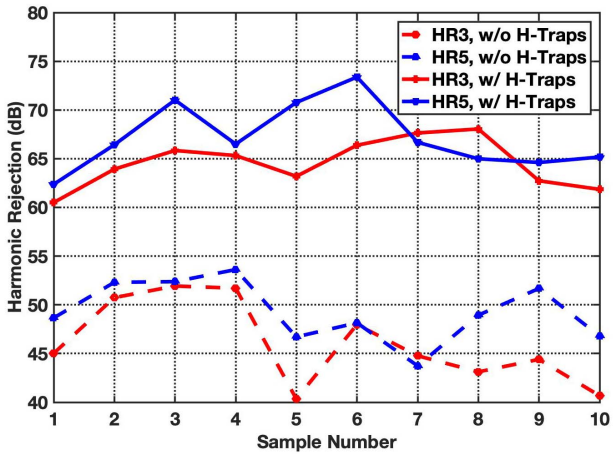
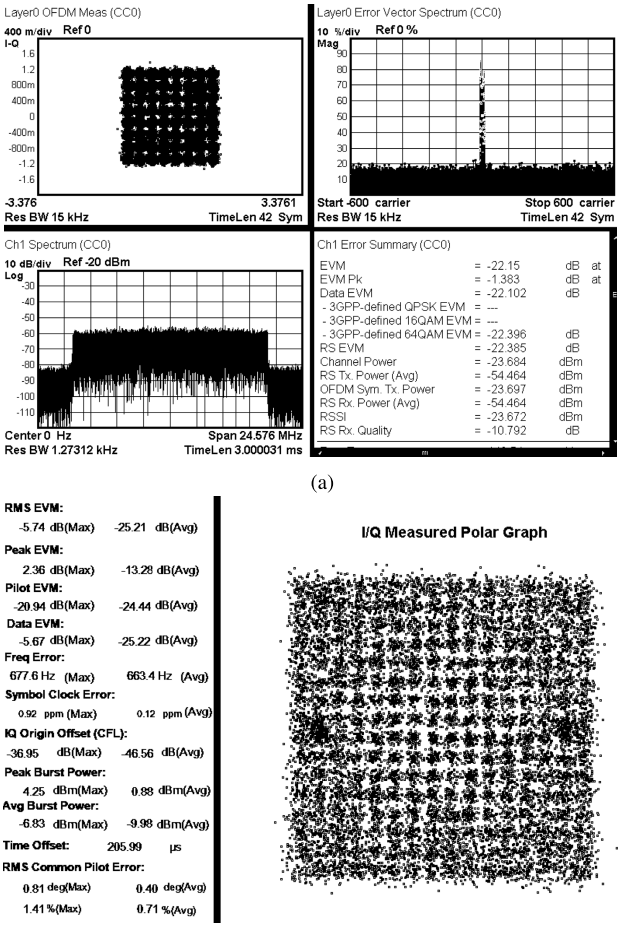


Fig. 32. HR3 and HR5 measured at 1 GHz for ten different chips.



(a)

(b)

Fig. 33. EVM test results for (a) LTE signal and (b) 802.11ax signal.

D. Tests With Modulated Signals

The RX imperfections collectively manifest themselves in error-vector magnitude (EVM) measurements of modulated

signals. The signals are provided by Keysight's N5182B MXG vector signal generator, and the receiver's quadrature BB outputs are captured by Keysight's N9030A PXA signal analyzer. Fig. 33(a) shows the signal constellation and EVM for a 2-GHz 64-QAM LTE signal with a CBW of 20 MHz. The EVM is −22.15 dB at an input level of −74 dBm. Fig. 33(b) repeats the measurement for a 5-GHz 256-QAM 802.11 ax signal with a CBW of 80 MHz. The EVM reaches −25.21 dB at an input level of −57 dBm.

Table I summarizes the measured performance of our receiver and compares it with the state of the art. We make a number of observations. First, only the design in [22] achieves an input bandwidth accommodating both cellular and 5-GHz Wi-Fi signals. Second, the 0-dBm-blocker NF reported in [22] is 5–7 dB higher than that of our RX. Third, the harmonic rejection in [22] appears to rely on manual adjustments of mismatches. Fourth, this work requires external tones at the harmonic frequencies for calibration purposes, which are difficult to generate. Fifth, as mentioned in Section III, the RX in [22] cannot reject the third and fifth harmonics simultaneously. We should also remark that none of the prior-art receivers in Table I has been tested with modulated signals.

VI. Conclusion

This article has proposed a number of new concepts that can improve the performance of wideband RF receivers. Examples include a multi-loop receiver architecture, harmonic rejection by traps, blocker rejection without the need for large switches, the translational virtual ground, and a new op amp topology. The receiver operates from 400 MHz to 6 GHz, accommodating LTE and Wi-Fi signals.

Appendix I

As explained in Section III-B, the choice of $R_{sw} = 1/G_m$ maximizes blocker rejection at the output. We must, nonetheless, study the rejection at the *input* as well and, hence, determine whether the linearity is limited at the input or at the output. The transfer function from V_S to V_{in} in Fig. 3(a) is given by

$$\frac{V_{in}}{V_S} = \frac{1 + j(R_{sw} + R_L)C_{eq}\omega}{1 + j[R_{sw} + R_L + (1 + G_m R_L)R_S]C_{eq}\omega}. \quad (17)$$

For out-of-band attenuation, we assume a large ω

$$\frac{V_{in}}{V_S} \approx \frac{1}{1 + G_m R_S\left(\frac{1+G_m R_L}{G_m R_{sw}+G_m R_L}\right)} \quad (18)$$

noting that the input attenuation improves as R_{sw} becomes much smaller than R_L, e.g., as R_{sw} approaches zero. With typical values of $G_m R_L = 3$ and $G_m R_S = 5$, we obtain input attenuations of 15.6 and 17.7 dB for $R_{sw} = 1/G_m$ and $R_{sw} = 0$, respectively. That is, the choice of $R_{sw} = 1/G_m$ incurs a penalty of 2.1 dB at the input.

At the output, however, $R_{sw} = 1/G_m$ offers a much greater advantage. The input–output transfer function expressed by (5) yields an output attenuation of 17.7 dB if $R_{sw} = 0$ and 32.1 dB if $R_{sw} = 1.2/G_m$ (20% mismatch). That is, the output swing is reduced by about 14.4 dB.

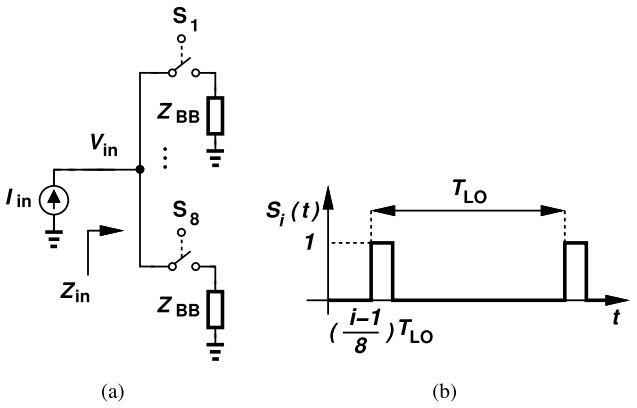


Fig. 34. (a) Eight-path structure with the load of Z_{BB} in each path and (b) corresponding LO waveform.

Appendix II

In this appendix, we prove the eightfold reduction in the translated impedance, a property exploited in Section IV to create a translational virtual ground.

Consider the arrangement shown in Fig. 34(a) where the current reaching each BB impedance can be expressed as $i_{in}(t)S_i(t)$ and $S_i(t)$ is the periodic LO waveform in Fig. 34(b). The resulting voltages on the eight impedances are "scanned" by the switches, yielding an input voltage equal to their sum

$$v_{in}(t) = \sum_{i=1}^{8}\{[i_{in}(t)S_i(t)] * z_{BB}(t)\}S_i(t) \quad (19)$$

where $z_{BB}(t)$ denotes the impulse response of Z_{BB}. We assume that Z_{BB} is a low-pass impedance that drops to a negligible value at ω_{LO} and its harmonics. Taking the Fourier transform and considering only the components near the LO frequency, we have

$$Z_{in}(j\omega) = 8\left[\frac{\sin\left(\frac{\pi}{8}\right)}{\pi}\right]^2 Z_{BB}(\omega - \omega_{LO}) \approx \frac{1}{8}Z_{BB}(\omega - \omega_{LO}). \quad (20)$$

Appendix III

In this appendix, we study the stability of the multi-loop architecture in more detail. We start from the innermost loop and move toward the outermost loop as we guarantee stability for the inner ones. We initially disregard the effect of Banks 1–3. The innermost loop in Fig. 7 provides partial channel selection, has a bandwidth of ω_0, and consists of only G_{m3}, R_{F3}, C_{F3}, and C_{H3}; hence, it is stable. We then add the second feedback loop (R_{F2}, C_{F2}, C_{H2}, and Stage 2), noting the poles contributed by nodes X_1 and X_2. Plotted in Fig. 35, the simulated magnitude and phase of this loop transmission suggest a sub-unity gain and, hence, a stable response.

In the next step, we construct a model for the outermost feedback loop, representing the poles at X_1 and X_2 by ω_1 and ω_2, respectively. As shown in Fig. 36, the model contains

$$A(j\omega) = -\frac{A_0}{\left(1 + j\frac{\omega}{\omega_0}\right)\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)}. \quad (21)$$

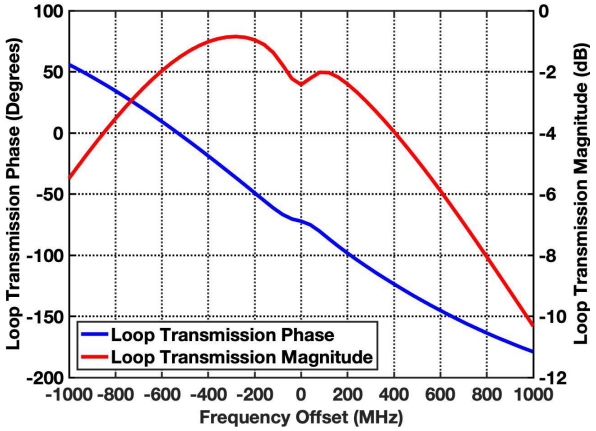


Fig. 35. Loop transmission magnitude and phase for the second loop.

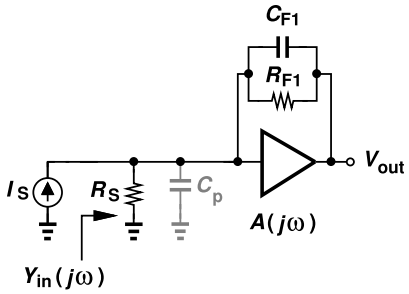


Fig. 36. Simplified model of the outermost loop.

The parasitic C_p is the RX input capacitance. To obtain the closed-loop input admittance, $Y_{\text{in}}(j\omega)$, we recall from (10) and its associated zero cancellation that $R_S = R_{F1}/(j\omega/\omega_0 + 1 + A_0)$. Assuming $A(j\omega) \gg 1$ at the frequency offset of interest, we have

$$Y_{\text{in}}(j\omega) = \frac{1}{R_S} + jC_p\omega_{\text{LO}} + \frac{\frac{1}{R_S}}{1 + j\frac{\omega}{\omega_a} - \left(\frac{\omega}{\omega_b}\right)^2} \tag{22}$$

where $\omega_a = \omega_1\omega_2/(\omega_1 + \omega_2)$ and $\omega_b = \sqrt{\omega_1\omega_2}$. At moderate frequency offsets, $|1 + j\omega/\omega_a| \gg (\omega/\omega_b)^2$, leading to

$$Y_{\text{in}}(j\omega) = \frac{1}{R_S} + jC_p\omega_{\text{LO}} + \frac{\frac{1}{R_S}}{1 + j\frac{\omega}{\omega_a}}. \tag{23}$$

The third term on the right signifies an inductive or capacitive admittance at positive or negative frequency offsets, respectively; the frequency response, thus, incurs some asymmetry around ω_{LO}, a pronounced effect for the 160-MHz channel.

In order to remove the third term's frequency dependence in (23), we can add an admittance of the form $[R_S(1 - j\omega_a/\omega)]^{-1}$, which, surprisingly, represents an eight-path filter with $R_{\text{sw}} = R_S$ and $C = 1/(8R_S\omega_a)$. Bank B_3 in Fig. 7 plays this role. At higher frequency offsets, i.e., if $\omega/\omega_b > 1$, the third term in (22) contains a negative conductance, posing potential instability. Fortunately, Bank 3 also introduces a positive conductance equal to $1/R_S$ at larger frequency offsets and overwhelms the negative component.

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Hossein Razavi (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees from the Sharif University of Technology, Tehran, Iran, in 2014 and 2016, respectively, and the Ph.D. degree from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 2021, all in electrical engineering.

Following his Ph.D. degree, he held a post-doctoral scholar position at the Communication Circuits Laboratory, UCLA. He has been with Broadcom Inc., Irvine, CA, USA, since 2021. His research interest includes RF, millimeter-wave, analog and mixed-mode integrated circuit designs for wireless transceivers, and frequency synthesizers.

Dr. Razavi received the UCLA Department of Electrical and Computer Engineering Fellowship in 2017, the Analog Devices Outstanding Student Designer Award in 2018, the Broadcom Foundation Fellowship in 2018, and the UCLA Dissertation Year Fellowship in 2019.

Behzad Razavi (Fellow, IEEE) received the B.S.E.E. degree from the Sharif University of Technology, Tehran, Iran, in 1985, and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, USA, in 1988 and 1992, respectively.

He was with AT&T Bell Laboratories, Holmdel, NJ, USA, and Hewlett-Packard Laboratories, Palo Alto, CA, USA, until 1996. He was an Adjunct Professor with Princeton University, Princeton, NJ, USA, from 1992 to 1994, and Stanford University in 1995. Since 1996, he has been an Associate Professor and subsequently a Professor of electrical engineering with the University of California at Los Angeles, Los Angeles, CA, USA. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998 and 2012) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001 and 2016) (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003, and Wiley, 2012), *Design of CMOS Phase-Locked Loops* (Cambridge University Press, 2020), and *Fundamentals of Microelectronics* (Wiley, 2006, 2014, and 2021) (translated to Korean, Portuguese, and Turkish) and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996) and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003). His current research interests include wireless and wireline transceivers, and data converters.

Prof. Razavi is also a member of the U.S. National Academy of Engineering and a fellow of the U.S. National Academy of Inventors. He received the Beatrice Winner Award for Editorial Excellence at the 1994 Technical Program Committees of the International Solid-State Circuits Conference (ISSCC), the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998, and the McGraw-Hill First Edition of the Year Award in 2001. He was a co-recipient of the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, and the CICC Best Invited Paper Award in 2009 and 2012. He was a co-recipient of the 2012 and the 2015 VLSI Circuits Symposium Best Student Paper Awards and the 2013 CICC Best Paper Award. He was also recognized as one of the top-ten authors in the 50-year history of ISSCC. He received the 2012 Donald Pederson Award in Solid-State Circuits. He was a recipient of the American Society for Engineering Education PSW Teaching Award in 2014 and the 2017 IEEE CAS John Choma Education Award. He has served on the ISSCC from 1993 to 2002 and the VLSI Circuits Symposium from 1998 to 2002. He has served as a Guest Editor and an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and *International Journal of High Speed Electronics and Systems*. He has served as the founding Editor-in-Chief of the IEEE SOLID-STATE CIRCUITS LETTERS. He has served as an IEEE Distinguished Lecturer.