A 2.4 GHz 4 mW Integer-N Inductorless RF Synthesizer

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***Abstract*—The high phase noise of ring oscillators has generally discouraged their use in RF synthesis. This paper introduces an integer-N synthesizer that employs a type-I loop to achieve a wide bandwidth, allowing the use of ring oscillators, and a master-slave sampling loop filter along with harmonic traps to suppress spurs. A 2.4 GHz prototype fabricated in 45 nm digital CMOS technology provides a loop bandwidth of 10 MHz and a spur level of −65 dBc. The phase noise is −114 dBc/Hz at 1 MHz offset.**

***Index Terms*—Frequency synthesizer, harmonic trap, phase-locked loop (PLL), reference spur, voltage-controlled oscillator (VCO), Δ modulator.**

I. Introduction

RF SYNTHESIS has generally shied away from ring oscillators due to their much more severe phase noise-power trade-offs than those of LC topologies. Today's multiband, multimode radios, however, require a number of synthesizers and can greatly benefit from compact, flexible implementations afforded by ring oscillators.

This paper proposes a phase-locked loop (PLL) architecture that can achieve a wide loop bandwidth, thus suppressing the voltage-controlled oscillator (VCO) phase noise and allowing the use of a ring topology. An integer-N synthesizer based on this architecture also incorporates "harmonic traps" on the VCO control line to reduce the output sidebands [1]. Most of the concepts introduced here are applicable to other PLL and oscillator topologies as well. Implemented in the TSMC 45 nm digital CMOS technology, an experimental prototype exhibits a phase noise of −114 dBc/Hz up to 10 MHz offset with a spur level of −65 dBc.

Section II provides the motivation for this work and reviews the bandwidth limitations of traditional PLLs. Section III describes the evolution of the proposed synthesizer architecture. Section IV deals with phase noise considerations, and Section V is concerned with spur reduction. Section VI presents the experimental results.

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II. Background

A. General Considerations

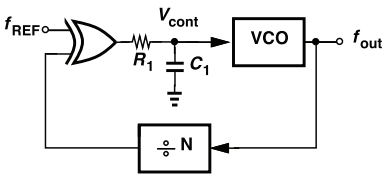
The need for LC oscillators in RF synthesis has been solidified by various studies revealing that the white-noise-induced phase noise of ring oscillators trades primarily with the power consumption [2], [3] and is relatively independent of the number of stages. However, ring oscillators do present compelling advantages. 1) They occupy a smaller area and can be readily placed within a transceiver layout with less serious concerns regarding proximity effects. 2) They entail much less coupling to and from other circuits. 3) They achieve a wider tuning range and can be multiplexed to cover decades of frequencies. 4) They readily generate multiple phases.

That the phase noise of ring oscillators is difficult to improve at the circuit level forces us to higher levels of abstraction. For example, [4] processes the signals in an RF receiver (RX) so as to suppress the phase noise in reciprocal mixing. This approach, however, does not correct for the effect of phase noise on the received signal constellation and the error vector magnitude (EVM) (e.g., in the absence of a blocker), nor is it applicable to the transmitter (TX). It is interesting to note that 1) applications entailing significant reciprocal mixing, e.g., GSM, actually place tighter requirements on the TX phase noise, and 2) applications specifying the phase noise by the EVM, e.g., IEEE 802.11 a/b/g, impose equally stringent phase noise constraints on RX and TX. In other words, the TX phase noise is at least as critical as the RX phase noise in most systems. It is therefore desirable to seek a solution that can be applied to both.

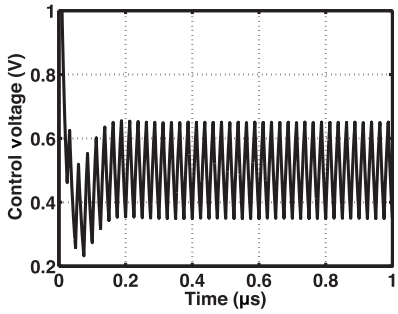
B. PLL Bandwidth Limitations

Another level of abstraction at which phase noise reduction can be considered is the synthesizer architecture. The loop bandwidth is generally constrained by three factors: 1) the PLL reference frequency, f_{REF}; for example, in a mobile phone environment, only a crystal oscillator around 20 MHz is available; 2) the PLL stability limit, often called "Gardner's Limit," and generally accepted to be around $f_{\mathrm{REF}}/10$ for type-II topologies; and 3) the ripple amplitude on the VCO control line and hence the output spur level. In the presence of charge pump (CP) nonidealities, the loop bandwidth is reduced to typically $f_{\mathrm{REF}}/20$ or less if spurs lower than −60 dBc are required [5]–[9].

It is helpful to briefly review the different bandwidths encountered in PLL analysis: 1) the input–output transfer function has a certain 3 dB bandwidth, which we call the "PLL bandwidth" f_{BW} in this paper; 2) the loop transmission has



(a)



(b)

Fig. 1. (a) Traditional type-I PLL architecture. (b) Settling behavior with bandwidth of 5.6 MHz.

a unity-gain bandwidth f_{UGB}; and 3) the VCO noise transfer function, a high-pass response, also has a 3 dB bandwidth $f_{n,\,VCO}$. For example, a type-II PLL with a charge pump current I_p, a loop filter capacitor C_1, a VCO gain K_{VCO}, a divide ratio N, and a unity damping factor provides $2\pi f_{BW} \approx 2.5\omega_n = 2.5\sqrt{I_p K_{VCO}/(2\pi\, NC_1)}$, $2\pi f_{UGB} \approx 2.1\omega_n$, and

$$2\pi f_{n,\,VCO} \approx 1.55\omega_n. \tag{1}$$

For example, if f_{UGB} is chosen in the range of $f_{REF}/20$ to $f_{REF}/10$, then

$$0.037 f_{REF} < f_{n,\,VCO} < 0.074 f_{REF}. \tag{2}$$

As mentioned above, [5]–[9] choose a loop bandwidth less than $f_{REF}/20$, thus falling on the low side of (2).

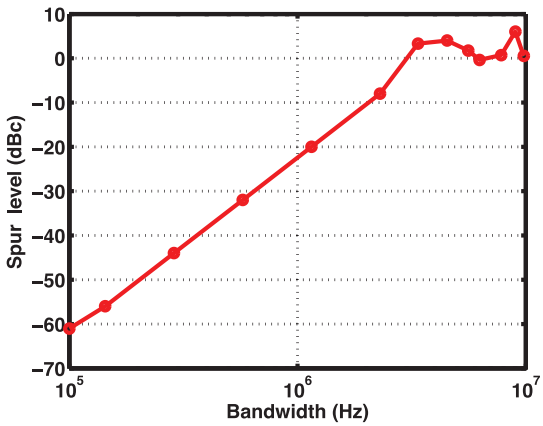


Fig. 2. Spur level versus bandwidth for type-I PLL.

III. Proposed Wideband PLL

Our approach to suppressing the VCO phase noise is to develop a PLL topology that avoids Gardner's limit and, if necessary, deal with the ripple on the control voltage by additional techniques. We assume $f_{REF} = 20$ MHz. Let us consider a type-I PLL architecture. Shown in Fig. 1(a), such a loop contains only one integrator and can, in principle, remain stable with a wide bandwidth. For example, Fig. 1(b) depicts the circuit's transient behavior with $(R_1C_1)^{-1} = 2\pi(40\text{ MHz})$, $K_{VCO} = 1500$ MHz/V, $N = 120$, and hence a loop bandwidth of 5.6 MHz. Of course, since the exclusive-OR (XOR) output swings from 0 to V_{DD}, the VCO experiences a large ripple. In fact, as R_1C_1 is reduced, the theoretical loop bandwidth can even exceed $f_{REF}/2$, but, as plotted in Fig. 2, the spurs eventually rise *above* the carrier, rendering the circuit meaningless. This PLL sustains a static phase error in proportion to the oscillator control voltage. For a V_{cont} ranging from 0 to V_{DD}, this error varies from 0 to about 180°.

The type-I PLL also suffers from a limited capture range. If the VCO begins with a frequency of f_1 and the XOR output at $|f_1/N - f_{REF}|$ is heavily attenuated by the filter, then the loop has no tendency to lock. In the foregoing example, $(R_1C_1)^{-1}$ must be lowered to $2\pi(0.47\text{ MHz})$ for the output spurs to fall to -35.5 dBc, yielding a simulated capture range of about 7.4%.

A. Type-I PLL with Sampling Filter

In a manner similar to charge-pump PLLs [10], [11], we can replace the continuous-time filter in Fig. 1(a) with a discrete-time implementation, aiming to isolate the VCO from the large XOR jumps. As depicted in Fig. 3(a), we wish to select the timing between the main input and V_F such that S_0 turns ON only during a "settled" level. Unfortunately, this is not possible because V_X still jumps between 0 and V_{DD}. Fig. 3(b) shows the loop's waveforms in the locked condition, indicating that V_X varies at $2f_{REF}$ if the input has a 50% duty cycle. When V_F goes high, V_{cont} attempts to track V_X, reaching a certain level V_1 that is necessary for the VCO to operate at Nf_{REF}.[1] That is, the loop adjusts the phase error $\Delta\phi$, until the V_{cont} transient yields a value of V_1 at the end of one T_{REF}.

The above technique does provide a constant voltage V_1, for the VCO while S_0 is off. We therefore wish to modify the circuit so that the VCO does not sense the transient from t_1 to t_2. This is accomplished by inserting one more sampling network in the VCO control path [Fig. 4(a)], with the two now operating in a master–slave manner. The divider output is converted to two nonoverlapping phases, preventing direct feedthrough from V_X to V_{cont}. We expect to observe a large ripple on C_1, similar to that in Fig. 3(b), but a small ripple on C_2. As an example, Fig. 4(b) shows the transient behavior with $C_1 = 16$ pF, $C_2 = 1$ pF, $K_{VCO} = 280$ MHz/V, and $N = 120$. The loop bandwidth is about 9 MHz and the loop settles in roughly 10 input cycles.

The PLL architecture employing the master–slave sampling filter (MSSF) displays several interesting and useful properties.

[1]This is true only if the ripple is small.

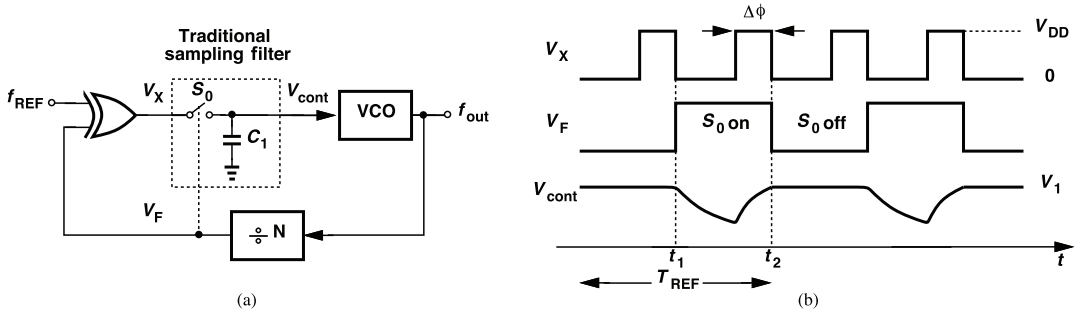


Fig. 3. (a) Type-I PLL with traditional sampling filter. (b) Time-domain operation.

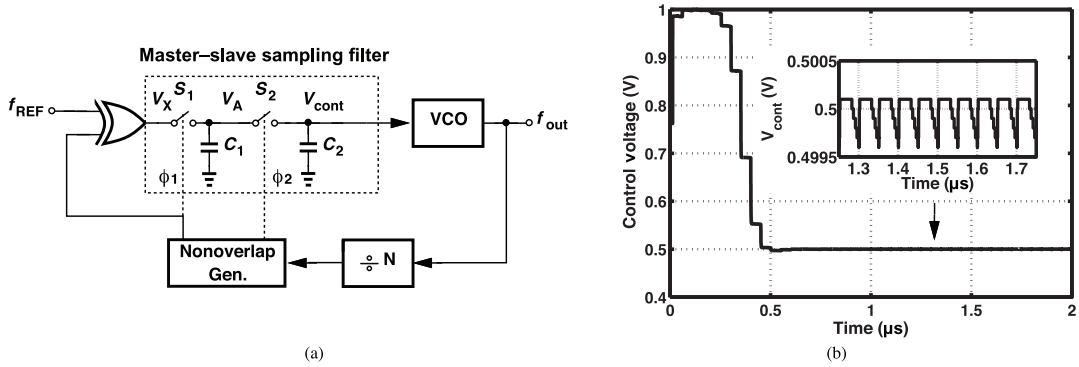


Fig. 4. Proposed PLL (a) architecture, and (b) settling behavior.

As explained below, compared to the traditional type-I PLL, its capture range is much wider, and, in comparison to type-II PLLs, it achieves a loop bandwidth close to $f_{\text{REF}}/2$, settles faster, and avoids the difficulties in low-voltage CP design.

B. MSSF Transfer Function

As explained above, the periodic voltage jumps at V_X in Fig. 4(a) do not reach V_{cont}, implying that the master–slave filter response has notches at the reference frequency and its harmonics. We examine this response in detail here.

As a continuous-time (CT) approximation, we can say that C_1 switches between V_X and V_{cont} periodically, thus acting as a series resistor R_{eq} equal to $1/(f_{\text{CK}}C_1)$, where f_{CK} denotes the sampling frequency and is equal to f_{REF} when the loop reaches the locked condition. In other words, the filter resembles a first-order section having a response given by

$$H(s) = \frac{1}{1 + R_{\text{eq}}C_2 s} = \frac{1}{1 + \dfrac{C_2}{C_1 f_{\text{CK}}} s}. \tag{3}$$

Note that this response accounts for charge sharing between C_1 and C_2, but fails to predict the harmonic notches. It is also a crude approximation if the PLL bandwidth approaches $f_{\text{REF}}/2$.

A more accurate transfer function is obtained if we consider the MSSF as a zero-order hold (ZOH) circuit. As illustrated in Fig. 5, the circuit converts a CT input to a discrete-time output. If $C_2 \ll C_1$ so that charge sharing between the two capacitors can be neglected, then the ZOH output can be expressed as [12]

$$Y(f) = e^{-j2\pi f T_{\text{CK}}/2} \frac{\sin \pi f T_{\text{CK}}}{\pi f T_{\text{CK}}} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_{\text{CK}}}\right). \tag{4}$$

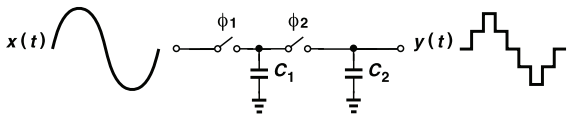


Fig. 5. Input and output waveforms of MSSF with zero switch resistance.

For the output component of interest, $n = 0$ and

$$Y_0(f) = e^{-j2\pi f T_{\text{CK}}/2} \frac{\sin \pi f T_{\text{CK}}}{\pi f T_{\text{CK}}} X(f). \tag{5}$$

This result, of course, predicts the notches at the harmonic of f_{CK} but disregards charge sharing.[2]

Even though operating as a master–slave storage circuit, the proposed filter exhibits a delay of $T_{\text{CK}}/2$, rather than T_{CK}, in the PLL environment. This is because the XOR produces the phase error information twice per cycle. Illustrated in Fig. 6, this effect can be seen by displacing the f_{REF} edges by a small amount ΔT and observing that V_X inherits this change from both the rising edge and the falling edge of V_{in}. Consequently, V_A changes in about $T_{\text{CK}}/2$ seconds and is frozen thereafter. If the MSSF delay were as long as T_{CK}, the PLL would become unstable for a unity-gain bandwidth of $f_{\text{REF}}/4$.

Equation (5) is a reasonable MSSF model for our analysis and design efforts described below, especially because we will select C_2 much less than C_1, thus minimizing charge sharing and improving the ZOH approximation. However, a more

[2]A z-domain model can also be constructed but yielding less intuition in terms of stability and closed-loop behavior (Sections III-C and III-D).

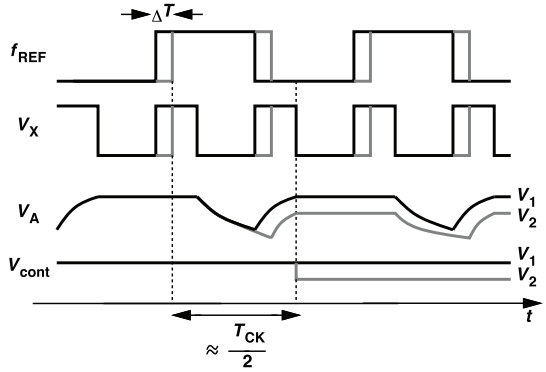


Fig. 6. XOR and MSSF time-domain waveforms.

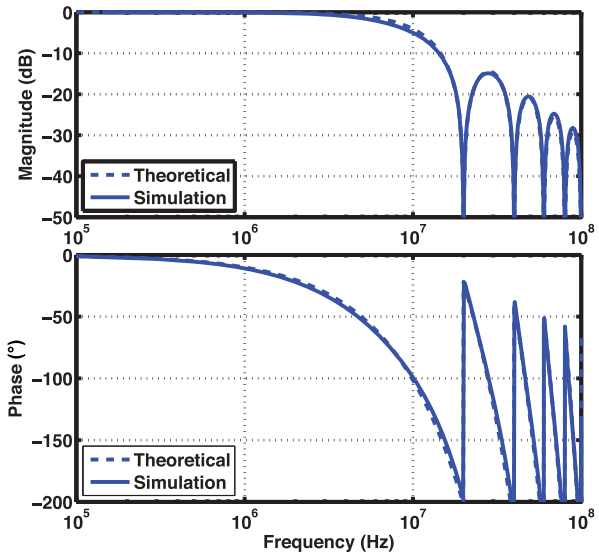


Fig. 7. Magnitude and phase responses of MSSF.

accurate model, obtained empirically, is as follows:

$$H_{\text{MSSF}}(j\omega) = \frac{1}{1+\dfrac{C_2}{C_1 f_{\text{CK}}}j\omega} e^{-j\pi f T_{\text{CK}}} \frac{\sin \pi f T_{\text{CK}}}{\pi f T_{\text{CK}}}. \quad (6)$$

Plotted in Fig. 7 are the magnitude and phase of the MSSF transfer function as predicted by (6) and as obtained from transient circuit simulations. Here, $C_1 = 16$ pF, $C_2 = 1$ pF, and $f_{\text{REF}} = 20$ MHz. We observe good agreement between the two. In this example, the filter has a 3 dB bandwidth of 7.4 MHz, at which the phase shift reaches $-75°$. To minimize this phase shift (which affects the loop stability), we typically choose $C_1 \gg C_2$ and reduce the contribution of the first fraction in (6).

The deep notches in Fig. 7 distinguish the MSSF from continuous-time filters. These notches suppress the harmonic components generated by the XOR gate in Fig. 4(a), thereby easing the trade-of between the loop bandwidth and the ripple amplitude. Nonetheless, second-order effects do create some ripple and are addressed in Section V.

C. Stability Considerations

While greatly suppressing the ripple, our proposed PLL is not unconditionally stable. In this section, we deal with this point.

From (6), the loop transmission of the topology shown in Fig. 4(a) can be expressed as

$$H(j\omega) = \frac{K_{\text{PD}}K_{\text{VCO}}}{N} \times \frac{1}{j\omega} \times \frac{1}{1+\dfrac{C_2}{C_1 f_{\text{REF}}}j\omega} e^{-j\pi f T_{\text{REF}}} \frac{\sin \pi f T_{\text{REF}}}{\pi f T_{\text{REF}}} \quad (7)$$

where K_{PD} is the phase detector (PD) gain (chosen approximately equal to 2.2 V/rad so as to provide the desired bandwidth). We have approximated the MSSF sampling rate by f_{REF}. To determine the phase margin, we must examine $\angle H(j\omega)$ at the unity-gain bandwidth f_{UGB}, i.e., the frequency at which $|H(j\omega)|$ drops to unity. To this end, we make two approximations. 1) As explained in Section III-B, $C_1 \gg C_2$ and hence the fraction $1/[1 + C_2 j\omega/(C_1 f_{\text{REF}})]$ contributes negligibly to $\angle H$ and $|H|$. 2) Predicting that $f_{\text{UGB}} < f_{\text{REF}}/2$, we also neglect the effect of the sinc on $|H|$. It follows that $|H(j\omega)| \approx K_{\text{PD}}K_{\text{VCO}}/(N\omega)$ and $2\pi f_{\text{UGB}} \approx K_{\text{PD}}K_{\text{VCO}}/N$. The phase contains a $-90°$ contribution by the VCO and $-\pi f T_{\text{REF}}$ by the MSSF, $\angle H(j\omega) \approx -\pi/2 - \pi f T_{\text{REF}}$. The phase margin $\pi + \angle H(j2\pi f_{\text{UGB}})$ is thus equal to

$$\text{PM} = \frac{\pi}{2} - \pi f_{\text{UGB}} T_{\text{REF}} = \frac{\pi}{2} - \frac{K_{\text{PD}}K_{\text{VCO}}}{2N} T_{\text{REF}}. \quad (8)$$

Equation (8) imposes an upper bound of $f_{\text{REF}}/2$ on f_{UGB}. The phase margin reaches about $45°$ for $f_{\text{UGB}} = f_{\text{REF}}/4$.

D. Closed-Loop Behavior

As mentioned in Section II, the closed-loop input–output bandwidth and the VCO noise transfer bandwidth are of interest. For the former, we have

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}}(j\omega) = \frac{NH(j\omega)}{1+H(j\omega)}. \quad (9)$$

With the approximation stipulated in Section III-C, $H(j\omega) \approx [K_{\text{PD}}K_{\text{VCO}}/(Nj\omega)] \exp(-j\pi f T_{\text{REF}})$. As shown in Appendix I, the 3 dB bandwidth is obtained as

$$2\pi f_{\text{BW}} \approx 2\sqrt{3} f_{\text{REF}} \sqrt{\frac{\alpha - 1 + \sqrt{(\alpha-1)^2 + \alpha^3/6}}{\alpha}} \quad (10)$$

where $\alpha = 2\pi f_{\text{UGB}}/f_{\text{REF}}$. Recall from (8) that $f_{\text{REF}}/4 < f_{\text{UGB}} < f_{\text{REF}}/2$ for $45° > PM > 0$, i.e., $\pi/2 < \alpha < \pi$. For this range of α, we have

$$0.55 f_{\text{REF}} < f_{\text{BW}} < 0.71 f_{\text{REF}}. \quad (11)$$

The key point here is that the closed-loop bandwidth can reach $f_{\text{REF}}/2$ with a reasonable phase margin.

The wide bandwidth of the proposed PLL naturally translates to a fast lock transient, e.g., about 10 input cycles as shown in Fig. 4(b).

For the VCO noise transfer, we have $\phi_{\text{out}}/\phi_{\text{VCO}} = (1+H)^{-1}$. The 3 dB bandwidth is obtained as

$$2\pi f_{n,\,\text{VCO}} \approx 2\sqrt{3} f_{\text{REF}} \sqrt{\frac{\alpha + 1 - \sqrt{(\alpha+1)^2 - \alpha^3/6}}{\alpha}} \quad (12)$$

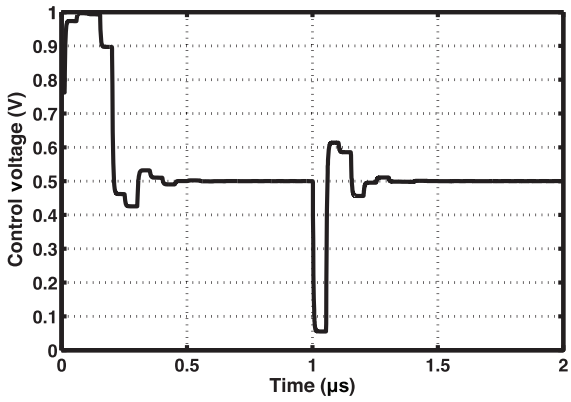


Fig. 8. Simulated control voltage with an input phase step at 1 μs.

which, for $\pi/2 < \alpha < \pi$, falls in the range of

$$0.16 f_{\text{REF}} < f_{n,\,\text{VCO}} < 0.26 f_{\text{REF}}. \tag{13}$$

For a fair comparison, we consider only the lower bound and note that, with respect to the two limits prescribed by (2), we have improved the VCO noise suppression bandwidth by about a factor of 2.2 to 4.3. In our synthesizer design, $f_{n,\,\text{VCO}} \approx 0.17 f_{\text{REF}}$ for a PM of around 42°. Fig. 8 shows the simulated settling behavior when PLL input experiences a phase step at 1 μs.

E. Acquisition Range

The MSSF-based PLL provides a much wider acquisition range than the traditional type-I architecture. Fundamentally, this is because the MSSF in Fig. 4(a) is clocked by the feedback signal, thus behaving differently from the continuous-time filter during the acquisition process. In order to formulate the acquisition range, we construct the open-loop configuration shown in Fig. 9(a), assuming that the VCO operates at a frequency of f_1. We follow the "beat" component generated by the XOR gate, $f_1/N - f_{\text{REF}}$, through the sampling filter and consider two cases. First, suppose the sampling process satisfies the Nyquist rate, i.e., $|f_1/N - f_{\text{REF}}| < f_1/(2N)$ and hence $(2/3)f_{\text{REF}} < f_1/N < 2f_{\text{REF}}$. In this case, the beat component passes through as a "baseband" signal, providing a nearly rail-to-rail voltage swing to the VCO. Fig. 9(b) plots the simulated control voltage in such a scenario; the VCO is heavily modulated at a rate of $f_1/N - f_{\text{REF}}$, producing a strong sideband at the divider output located at $f_1/N - (f_1/N - f_{\text{REF}}) = f_{\text{REF}}$.[3] In the closed-loop configuration, this sideband yields a dc component at the XOR output, leading to acquisition. The above inequality can be referred to the output as $(2/3)Nf_{\text{REF}} < f_1 < 2Nf_{\text{REF}}$. The loop therefore locks for an initial frequency between 2/3 and 2 times the final value. For example, if the VCO tuning range is from 1.6 to 4.8 GHz, then the loop can always lock to 2.4 GHz. The second case arises if the beat experiences aliasing, i.e., if f_1/N falls outside the acquisition range. The MSSF output now contains a component at $f_1/N - |f_1/N - f_{\text{REF}}|$, which does not lead to lock. Since the free-running VCO range lies well in the acquisition range, no frequency acquisition aid is necessary in our prototype. Circuit simulations confirm these predictions.

[3]MSSF sampling clock too carries sidebands, but they negligibly contribute to the MSSF output.

IV. Phase Noise Considerations

The phase noise of the proposed PLL arises from three building blocks, namely the VCO, the XOR gate, and the sampling filter. We wish to design the VCO according to the overall phase noise specification and reduce to negligible levels the XOR and filter contributions.

A. VCO Phase Noise

The VCO is designed as a three-stage inverter-based ring oscillator. Depicted in Fig. 10, the circuit employs MOS varactors for fine control and banks of switchable capacitors for coarse control. To achieve low flicker-noise-induced phase noise, we choose $W/L = 36\ \mu\text{m}/0.28\ \mu\text{m}$ for both PMOS and NMOS devices in each inverter. The varactors have a W/L of $26\ \mu\text{m}/0.2\ \mu\text{m}$,[4] providing a tuning range of about 200 MHz, and the capacitor banks consist of twelve 25 fF units, offering a range from 2 to 3 GHz. The circuit draws 3.1 mW from a 1 V supply at 2.4 GHz and exhibits a phase noise of -96 dBc/Hz at 1 MHz offset.

Three aspects of the VCO design merit remarks.

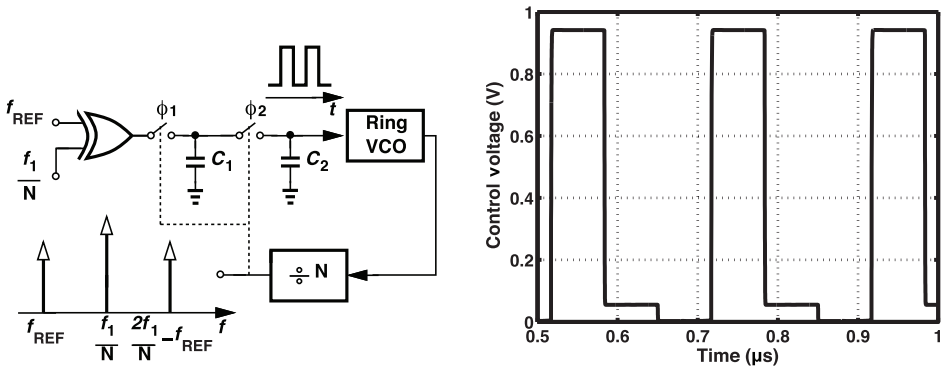
1) Simulations suggest that, among various ring oscillator tuning techniques, varactors cause the least degradation in phase noise as the frequency is varied for a given power consumption.[5] In a starved-inverter topology, e.g., the starving transistors themselves contribute significant phase noise as the frequency is decreased.
2) As with other inverter-based rings reported in prior work, the VCO suffers from supply sensitivity. In practice, such VCOs are fed from a low-dropout (LDO) regulator. In our prototype, we have used two separate supply pins for the analog and digital sections.
3) The three node waveforms within the ring can be combined to generate quadrature phases.[6] A full-size inverter sensing one node and a half-size inverter sensing another can merge their output nodes, generating $\pm 90°$ or $180°$ from $120°$ phases.

The shaping of the VCO phase noise deserves a note as well. Unlike type-II PLLs, a type-I PLL cannot force flicker-noise-induced phase noise to zero at zero frequency. To see this point, we choose a small ω in (16)in Appendix I and multiply the magnitude squared of the result by the VCO phase noise profile, e.g., η/ω^3, where η is a constant. The PLL output phase noise emerges as $N^2\omega^2(\eta/\omega^3) = N^2\eta/\omega$, rising as ω falls. Nevertheless, by virtue of its large bandwidth, the proposed PLL still displays a smaller integrated phase noise that a type-II architecture would. Fig. 11 plots the simulated free-running phase noise of the above VCO and the shaping that

[4]Varactor leakage has negligible effect on phase noise, and the variation of K_{VCO} affects the phase noise suppression by 1.5 dB.

[5]The varactors occupy 11% of the VCO area.

[6]For more precise quadrature generation, the single-ended ring oscillator in [13] can be used.



(a) (b)

Fig. 9. (a) Proposed PLL in open-loop configuration. (b) Simulated control voltage waveform.

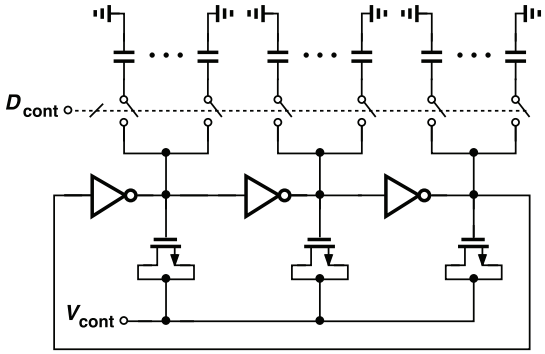


Fig. 10. VCO implementation.

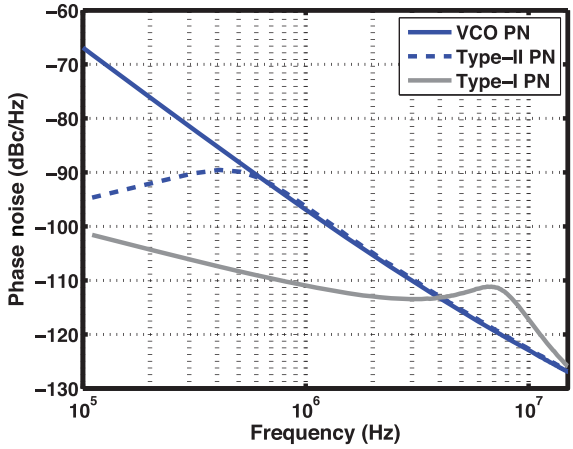


Fig. 11. VCO phase noise in free-running mode and in type-II and proposed PLLs.

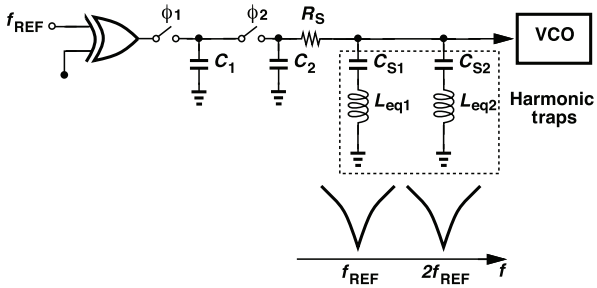


Fig. 12. Concept of harmonic traps.

it experiences in the two loops. (Here, the charge-pump PLL is assumed to have a loop bandwidth of $f_{REF}/20$,[7] while the type-I PLL is based on our architecture with a bandwidth of $f_{REF}/2$.) Our design leads to an integrated phase noise of 0.35° from 100 kHz to 15 MHz, and the type-II loop to 1.14° for the same range.[8] In practice, the charge pump flicker noise makes this comparison more favorable toward the proposed PLL.

B. PD and MSSF Phase Noise

In order to minimize the contribution of the PD/MSSF cascade in Fig. 4(a), we take several measures. First, the XOR incorporates PMOS and NMOS devices with $W/L = 32\ \mu m/80$ nm and $16\ \mu m/80$ nm, respectively, achieving a phase noise of -171 dBc/Hz at 5 MHz offset while consuming 86 μW at 20 MHz. This leads to an in-band phase noise at the PLL output equal to $-171\ \text{dBc/Hz} + 20\ \log N = -129$ dBc/Hz. Second, since S_1 carries large transient currents and can potentially generate high flicker noise, we choose $W/L = 20\ \mu m/100$ nm for this device. Third, the kT/C noise associated with S_2 and C_2 is reduced by selecting $C_2 = 1$ pF ($C_1 = 16$ pF contributes negligibly). This kT/C noise translates to in-band phase noise at the PLL output according to $S_{out,MSSF} \approx [kT/(2C_2)]\, f_{REF}^{-1} N^2/K_{PD}^2$, where the factor of 2 accounts for the fact that C_2 appears in parallel with C_1 ($\gg C_2$) for about half of the input period. With $C_2 = 1$ pF and $K_{PD} = 2.2\text{V/rad}$, we have $S_{out,MSSF} = -126$ dBc/Hz.

The foregoing study also prescribes a design procedure: we first pick the value of C_2 for negligible phase noise contribution and then choose C_1 to be 10–20 times larger. Finally, we size S_1 and the XOR devices for negligible noise as well.

V. Spur Reduction

Despite the transfer notches introduced by the sampling filter, we observe sidebands on the order of -50 to -55 dBc at the VCO output. This phenomenon arises from three mechanisms. 1) The large VCO varactors ($W/L = 26\ \mu m/0.2\ \mu m$) draw a

[7]For a reference spur level below -60dBc, reported type-II PLLs have a bandwidth of no more than $f_{REF}/20$; hence, this choice for a fair comparison with our architecture.

[8]The peaking in our phase noise can be reduced by choosing a smaller bandwidth. In general, some optimization is necessary at this stage.

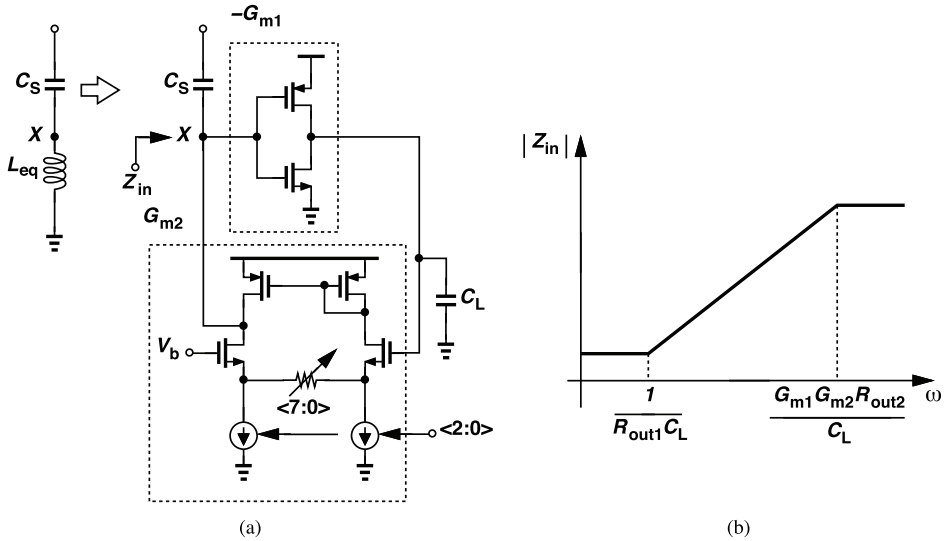


Fig. 13. (a) Harmonic trap implementation. (b) Magnitude of gyrator input impedance.

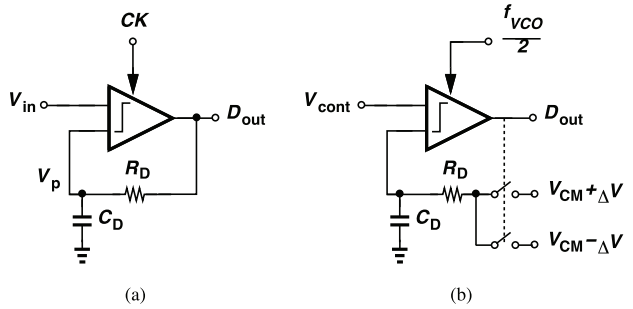


Fig. 14. (a) Traditional and (b) proposed Δ modulator architectures.

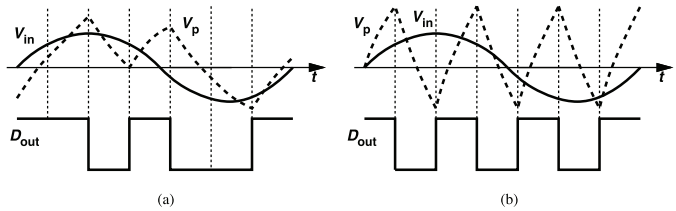


Fig. 15. Effect of R_DC_D on Δ modulator operation. (a) Long time constant. (b) Short time constant.

significant gate leakage current (∼ 80 nA) from C_2 in Fig. 4(a), causing a 2 mV droop in each cycle. 2) The leakage, charge injection, and clock feedthrough of S_2 produce another 1 mV_{pp} of ripple. 3) In the presence of ground bond wires, the bounce on the bottom plate of C_1 persists after S_2 turns ON, disturbing the control line periodically.

We propose the use of "harmonic" traps to suppress the ripple with little compromise in the bandwidth. Applicable to any PLL architecture and illustrated in Fig. 12, the idea is to add one or more series resonant branches in parallel with the control line, forming a low impedance to ground at f_{REF}, $2f_{REF}$, etc.

Harmonic traps entail three issues. 1) Active implementations ultimately present a tradeoff between the trap impedance and the power consumption, potentially unable to fight the MSSF output impedance. For this reason, R_S (≈ 2.5 kΩ) is inserted in Fig. 12. 2) The traps must have a sufficiently high Q so as to contribute negligible phase shift and noise for $f \leq f_{REF}/2$. 3) The traps' resonance frequencies must be calibrated with adequate resolution to deal with PVT variations.

A. Harmonic Trap Design

Each trap consists of a capacitor in series with an active inductor, obtained by gyrating another capacitor. As shown in Fig. 13(a), G_{m1} and G_{m2} constitute a gyrator, transforming C_L to $Z_{in} = L_{eq}s = C_Ls/(G_{m1}G_{m2})$ if their output impedances are assumed infinite. For example, the f_{REF} trap uses $G_{m1} =$ 0.92 mS, $G_{m2} = 54$ μS and $C_L = 3.5$ pF, creating $L_{eq} =$ 70 μH. The degeneration resistance and the bias currents within G_{m2} are programmable. The power dissipation is 170 μW.

For design purposes, we need a more accurate expression for Z_{in}. If the output impedances of G_{m1} and G_{m2} are denoted by R_{out1} and R_{out2}, respectively, then $Z_{in} = (R_{out1}C_Ls + 1)R_{out2}/(R_{out1}C_Ls + G_{m1}R_{out1}G_{m2}R_{out2} + 1)$. Plotted in Fig. 13(b), $|Z_{in}|$ reveals an inductive behavior for $(R_{out1}C_L)^{-1} < \omega < G_{m1}G_{m2}R_{out2}/C_L$. It is important that the trap resonance frequency, ω_{res}, lie well between the zero and pole frequencies so that Z_{in} approaches a pure inductor. We therefore view $(R_{out1}C_L)^{-1} \ll \omega_{res} \ll G_{m1}G_{m2}R_{out2}/C_L$ as a guideline for choosing C_L. If Z_{in} is rewritten as $\left[C_Ls/(G_{m1}G_{m2}) + (G_{m1}G_{m2}R_{out1})^{-1}\right] \| R_{out2}$, then we recognize that the inductance sees a series resistance equal to $(G_{m1}G_{m2}R_{out1})^{-1}$ and a parallel resistance equal to R_{out2}. Since R_{out2} is sufficiently large in our design, the quality factor is approximately equal to $R_{out1}C_L\omega$, about 15 at $f_{REF} =$ 20 MHz. With the large transistor dimensions chosen in this design, the gyrator input-referred offsets are less than 6 mV. To cover PVT variations, the trap frequency has a programmable range of ±30% around its nominal value with a resolution of 0.6 MHz. Circuit simulations indicate that the traps negligibly affect the loop settling time.

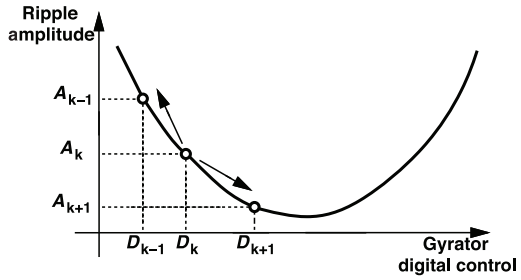


Fig. 16. Notch calibration algorithm.

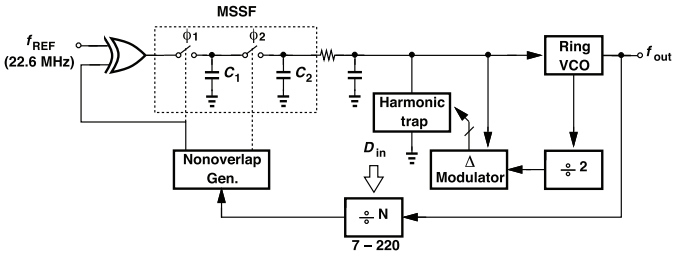


Fig. 17. Final proposed architecture of the synthesizer.

The noise contribution is formulated by modeling the gyrator noise by a current source and subjecting it to a (high-pass) transfer function to $V_{\rm cont}$ and another from $V_{\rm cont}$ to $\phi_{\rm out}$. Calculations and simulations predict a phase noise of -131 dBc/Hz at 5 MHz offset resulting from the traps.

B. Notch Calibration

To calibrate the traps, we must seek an error whose value reaches a minimum as the notch frequency reaches the desired value, e.g., $f_{\rm REF}$. The control ripple amplitude is one such error. But we must also measure this error with reasonable fidelity as, toward the end of calibration, it becomes very small. In our design, e.g., a spur level of -60 dBc at the output is equivalent to a ripple amplitude of about 0.28 $\rm mV_{pp}$.

We employ a Δ modulator as a compact, low-power ADC to measure the ripple waveform and reconstruct it in the digital domain. Shown in Fig. 14(a), a traditional Δ modulator consists of a comparator and a low-pass feedback network, forcing V_p to track $V_{\rm in}$. As a result, the running average of the pulsewidth-modulated output also tracks $V_{\rm in}$, provided that R_DC_D is sufficiently long [Fig. 15(a)]. Otherwise, the input peaks do not exceed the peaks of V_P, causing failure [Fig. 15(b)].

Similarly, the Δ modulator of Fig. 14(a) fails for small or slow input swings; it simply generates a periodic output at half of the clock frequency if the input peaks do not exceed the peaks of V_p. It can be proved that the sensitivity is given by $V_{\rm DD}\{1-\exp[-T_{\rm CK}/(2R_DC_D)]\}$, where the comparator output is assumed to swing between 0 and $V_{\rm DD}$. For example, a sensitivity of 0.28 $\rm mV_{pp}$ with $f_{\rm CK}\approx 1.2$ GHz translates to $R_DC_D = 3$ µs, demanding very large values for R_D and C_D. To resolve this issue, we modify the architecture as depicted in Fig. 14(b), where the comparator is clocked at $f_{\rm VCO}/2$ and its output drives a 1 bit DAC with a much smaller swing, $\pm\Delta V$. A ΔV of 25 mV, e.g., allows a 20 fold reduction in the R_DC_D product. In this design, we have $R_D = 50$ kΩ, $C_D = 4$ pF, and a StrongArm comparator consuming 80 µW.

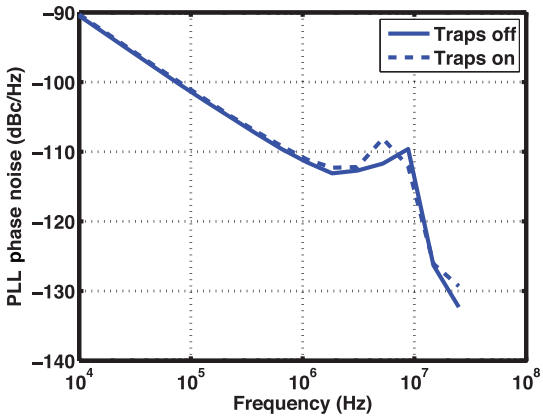


Fig. 18. Simulated PLL phase noise before and after harmonic traps are ON.

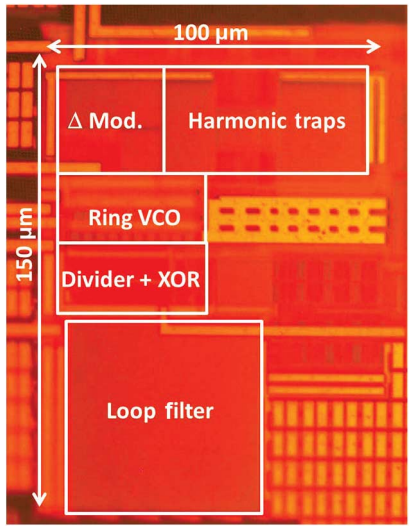


Fig. 19. Die micrograph.

Since the ripple amplitude is a convex function of the trap resonance frequency, we must somehow decide when the calibration has reached a minimum. As shown in Fig. 16, we measure the ripple for three consecutive gyrator codes D_{k-1}, D_k and D_{k+1} and consider three cases. 1) If $A_{k-1} > A_k > A_{k+1}$, we are on the descending slope and must increase the code. 2) If $A_{k-1} < A_k < A_{k+1}$, we are on the ascending slope and must decrease the code. 3) If $A_k < A_{k-1}$ and $A_k < A_{k+1}$, then D_k is the optimum value. The calibration runs in the background and compensates for temperature and supply drifts.

The overall synthesizer architecture is shown in Fig. 17. The feedback divider provides $N = 7-220$, but only the range from 120 to 124 is used for the 2.4 GHz band. Fig. 18 shows the simulated phase noise plot before and after harmonic traps are ON. As can be seen, the traps contribute negligible phase noise but increases the peaking by 1 dB due to their addtional phase shift.

VI. Experimental Results

The integer-N synthesizer has been fabricated in the TSMC 45 nm digital CMOS technology. As shown in Fig. 19, the die measures 100 µm ×150 µm. Tested with a 1 V supply, the

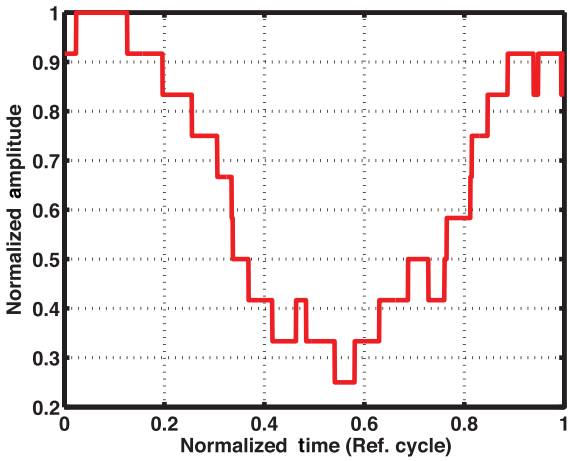


Fig. 20. Reconstructed ripple waveform sensed by Δ modulator.

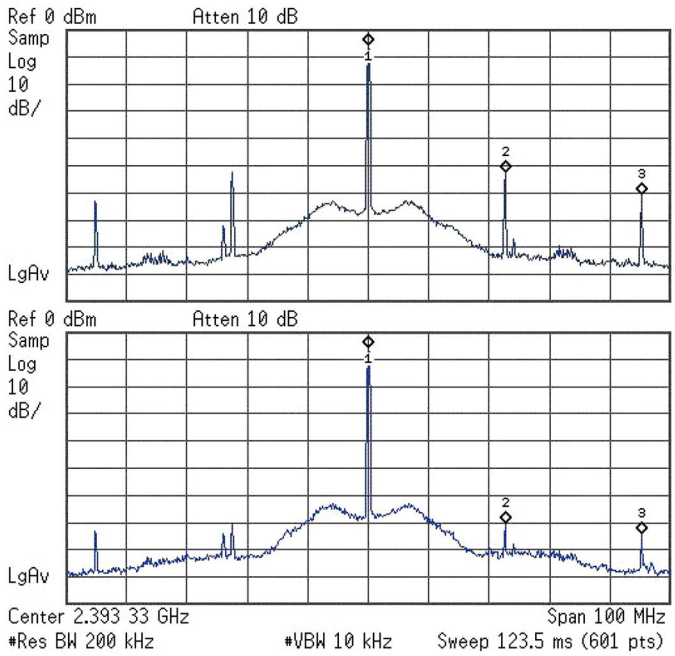


Fig. 21. Measured output spectrum with harmonic traps turned OFF (top) and turned ON (bottom).

synthesizer operates from 2 to 3 GHz and consumes 4 mW at 2.4 GHz. The 22.6 MHz input reference is produced by a low-noise crystal oscillator[9] (hence the departure from 20 MHz) and the output is measured by an Agilent spectrum analyzer. The Δ modulator output is sent off-chip and processed in Matlab, and the control codes are written back to the chip through a serial bus.

Upon power-up, the PLL locks with the harmonic traps OFF and then the traps are turned ON and calibrated. The initial calibration takes approximately 400 input cycles, but for subsequent frequency changes (initiated by a modulus change), the calibration settings remain constant because the notch frequencies do not depend on the output frequency. Fig. 20 shows the reconstructed control voltage ripple waveform as sensed by the Δ modulator. The output spectra of the

[9] The phase noise is around -170 dBc/Hz at 1 MHz offset.

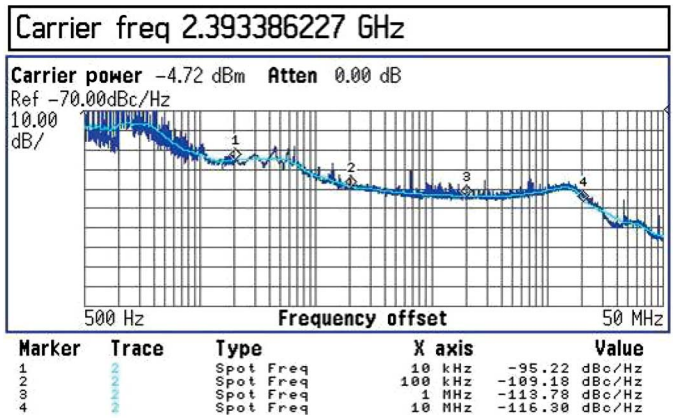


Fig. 22. Measured phase noise.

TABLE I
PERFORMANCE SUMMARY

	ISSCC'12 [14]	ISSCC'14 [15]	ISSCC'14 [16]	This work
Oscillator topology	Ring	Ring	LC	Ring
Reference freq. (MHz)	36	26	48	22.6
Output freq. (GHz)	3.1	2.4	2.3	2.4
Phase noise at 1 MHz offset (dBc/Hz)	–98	–94	–117	–113.8
RMS jitter (ps) Integ. range (MHz)	2.23 (N/A)	3.29 (0.01~40)	0.3 (0.01~30)	0.97 (0.001~200)
Ref. spur (dBc)	N/A	–75	–55	–65
Power (mW)	25.8	6.4	17.3	4
Area (mm^2)	0.32	0.013	0.75	0.015
Tech. (nm)	65	40	180	45
FoM_1 (dB)	–218.9	–221.6	–238	–234.1
FoM_2 (dB)	153.7	153.6	171.9	175.4

$$FoM_1 = 10\log_{10}\left[\left(\frac{\text{jitter}}{1\text{ s}}\right)^2\left(\frac{\text{power}}{1\text{ mW}}\right)\right] \quad FoM_2 = 10\log_{10}\left[\left(\frac{f_{OSC}}{\Delta f}\right)^2\left(\frac{1\text{ mW}}{\text{power}}\right)\right] - \text{Phase Noise}_{(\text{dBc/Hz})}$$

synthesizer with the harmonic traps OFF and ON are plotted in Fig. 21. The first-order spur falls from -47 to -65 dBc, and the second-order spur falls from -55 to -68.5 dBc. The measured phase noise is shown in Fig. 22. The in-band phase noise reaches -114 dBc/Hz. Integrated from 1 kHz to 200 MHz, the integrated jitter is equal to 0.97 ps_{rms}, which satisfies the IEEE 802.11 b/g standard. For all coarse VCO settings from 2 to 3 GHz, the loop is observed to lock.

The measurement is also done with different supply voltages (0.95V, 1.05V). After recalibration, the worst-case reference spur is -62 dBc while the worst-case jitter is 1.14 ps_{rms}. Among five measured chips, the phase noise plateau varies by about 1 dB. Table I summarizes the performance of our design and compares it to recently reported synthesizers in the range of 2.3 to 3.1 GHz. The proposed synthesizer achieves an FoM of -234.1 dB based on the integrated jitter and an FoM of 175.4 dB based on the phase noise.

VII. Conclusion

This paper presents an inductorless type-I synthesizer architecture for 2.4 GHz RF applications. A spur reduction approach based on harmonic traps is also introduced that measures the ripple on the control voltage by means of a Δ modulator and, using a three-point algorithm, forces the ripple to minimum.

ACKNOWLEDGMENT

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APPENDIX I

In this appendix, we use the approximation $[K_{\rm PD}K_{\rm VCO}/(Nj\omega)]\exp(-j\pi fT_{\rm REF})$ to determine the closed-loop bandwidth. From (9), we denote $K_{\rm PD}K_{\rm VCO}$ by K and write

$$\left|\frac{\phi_{\rm out}}{\phi_{\rm in}}(j\omega)\right| = \frac{K/\omega}{\left|1+\frac{K}{jN\omega}\exp(-j\pi fT_{\rm REF})\right|} = \frac{K/\omega}{\sqrt{N^2\omega^2-2KN\omega\sin\pi fT+K^2}}. \quad (14)$$

Equating the square of this quantity to $N^2/2$ yields the 3 dB bandwidth

$$N^2\omega_{\rm BW}^2 - 2KN\omega_{\rm BW}\sin\left(\frac{\omega_{\rm BW}T_{\rm REF}}{2}\right) - K^2 = 0. \quad (15)$$

Since $\sin\epsilon \approx \epsilon - \epsilon^3/6$ for $\epsilon \ll 1$ rad, $\left[(KNT_{\rm REF}^3)/24\right]\omega_{\rm BW}^4 + (N^2 - KNT_{\rm REF})\omega_{\rm BW}^2 - K^2 = 0$. We also denote $KT/N = K_{\rm PD}K_{\rm VCO}/(Nf_{\rm REF}) = 2\pi f_{\rm UGB}/f_{\rm REF}$ by α, obtaining (10).

We should mention that the VCO noise transfer function is obtained as

$$\frac{\phi_{\rm out}}{\phi_{\rm VCO}}(j\omega) = \frac{jN\omega}{j[N\omega - K\sin\pi fT_{\rm REF}] + K\cos\pi fT_{\rm REF}}. \quad (16)$$

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