Performance Bounds of ADC-Based Receivers Due to Clock Jitter

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***Abstract*—The maximum tolerable clock jitter for high-speed ADCs is pessimistically predicted by Nyquist-rate input sinusoidal tests. We prove that the jitter can be greatly relaxed in the presence of lossy channels in wireline systems. We derive compact expressions that allow PLL designers to decide how much jitter can be tolerated for a given channel loss and symbol rate.**

***Index Terms*—Analog-to-digital converter (ADC)-based receiver, clock jitter, jitter-induced noise, PAM4 signaling.**

I. Introduction

WIRELINE PAM4 receivers operating at tens of gigabits per second and targeting high-loss links typically employ an analog-to-digital converter (ADC) in their front end. The ADC resolution ranges from 6 to 7 bits [1], [2], [3], signifying a signal-to-noise ratio (SNR) of 38 to 44 dB in the ideal case. It is desirable that the Nyquist-rate ADC clock jitter minimally degrade the SNR, hence the need for low-noise phase-locked loops (PLLs).

In this brief, we first show that a common method of computing the jitter-induced noise (JIN) is far too pessimistic and demands excessively low clock jitter values. We then derive expressions for the SNR degradation in the presence of lossy channels. The objective is to provide system and circuit designers with simple equations that readily predict the tolerable clock jitter for a given SNR penalty. The analysis yields results that are generally applicable and specifically relevant to NRZ, PAM4, and PAM6 signaling.

Section II describes the results obtained in the prior art and their shortcomings. Section III presents our analysis framework and Section IV the general derivations. Comparisons with simulations are provided in Section V.

II. Prior Results

The most straightforward - and the most pessimistic - computation of jitter-induced noise assumes a full-scale sinusoidal input at the Nyquist rate in the form $V_R(t) = A_{in}\cos(2\pi f_{in}t)$ [4]. Since an ADC's sample-and-hold circuit and quantizer equivalently operate as an impulse sampler followed by a quantizer, we observe from Fig. 1 that each sample displaced by jitter can be viewed as one at the ideal sampling point but incurring an amplitude error. Assuming that the jitter has a variance of σ_j^2 and noting that the noise due to jitter is given by the power of dV_R/dt, one can show that the JIN power and the SNR are given by [4]

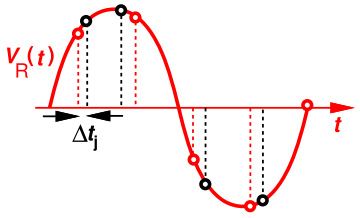

Fig. 1. Ideal samples (red dots) and jittery samples (black dots) of a sinusoid.

$$P_j = 2\pi^2 f_{in}^2 A_{in}^2 \sigma_j^2 \tag{1}$$

$$\text{SNR} = \frac{1}{4\pi^2 f_{in}^2 \sigma_j^2}. \tag{2}$$

This result is pessimistic because it condenses the entire input signal power in an impulse at the upper end of the input band. Nonetheless, this type of characterization is the most practical from the view point of ADC simulations and measurements.

We expect a more realistic JIN estimate if we assume a flat band-limited white-noise spectrum for the input signal [Fig. 2(a)]. As Eq. (1) suggests, components with lower frequencies experience less corruption. To obtain the total JIN power, we draw upon Rice's method of approximating the spectrum by n equally-spaced impulses [5] [Fig. 2(b)], and recognize that each carries a power of $\beta f_{in}/n$ and hence corresponds to a sinusoid whose peak amplitude is given by $A^2/2 = \beta f_{in}/n$. The sinusoids incur noise according to (1), yielding a total power of

$$P_j = \lim_{n\to\infty} 4\pi^2\sigma_j^2 \frac{\beta f_{in}}{n} \times \left[(\frac{f_{in}}{n})^2 + (\frac{2f_{in}}{n})^2 + \cdots + (\frac{nf_{in}}{n})^2 \right]$$

$$= \lim_{n\to\infty} 4\pi^2\sigma_j^2 \frac{\beta}{n^3} f_{in}^3 \frac{n(n+1)(2n+1)}{6} = \frac{4\pi^2\sigma_j^2\beta f_{in}^3}{3}. \tag{3}$$

Hence,

$$\text{SNR} = \frac{\beta f_{in}}{P_j} = \frac{3}{4\pi^2 f_{in}^2 \sigma_j^2}. \tag{4}$$

This expression agrees with the alternate derivation in [6] and reveals a threefold increase in the SNR compared to Eq. (2).

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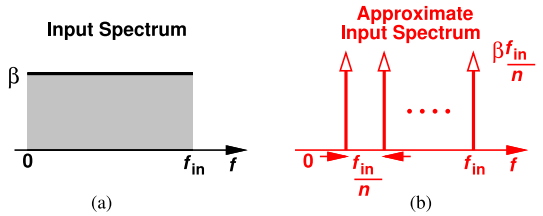

Fig. 2. (a) Input with band-limited, white spectrum, and (b) approximation of the spectrum with n equally-spaced impulses.

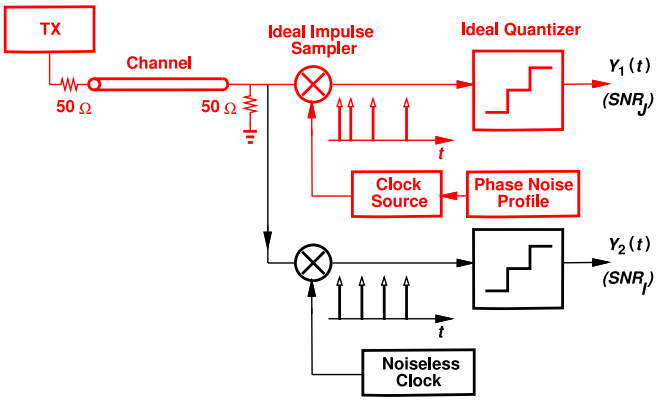

Fig. 3. Analysis framework.

While more realistic, this result still poses a pessimistic upper bound on jitter for links with lossy channels.

III. Analysis Framework

Figure 3 depicts the framework for our analysis. A transmitter (TX) generates PRBS-9 PAM data, which then travels through a channel having a certain frequency response. The receiver (RX) performs sampling at the symbol rate by impulses such that their position can be modulated according to a given phase noise profile. The result is then digitized by a 6- or 7-bit quantizer. In addition, we subject the received data to jitterless sampling and quantization (as shown in the lower part of Fig. 3). The channel is represented by a scalable RLC model [7] whose loss can be adjusted by cascading more or fewer stages (the model incorporates both the skin-effect and the dielectric loss). We wish to determine the SNR degradation for a given amount of jitter.

We should make two remarks. First, denoting the ADC's analog LSB by Δ, we express the "jittery" SNR in Fig. 3 as $\text{SNR}_\text{J} = P_{sig}/(\Delta^2/12 + P_j)$, where P_{sig} is the total received signal power. The "ideal" SNR, on the other hand, is equal to $\text{SNR}_\text{I} = P_{sig}/(\Delta^2/12)$. The ratio of these two quantities can be viewed as the SNR penalty.

Second, the transmitted data exhibits a sinc^2 spectrum of the form [8]

$$S_{TX}(f) = \frac{k}{f_R}\left(\frac{\sin(\pi f/f_R)}{\pi f/f_R}\right)^2, \tag{5}$$

where f_R is the symbol rate, and k is a constant whose value depends on the signaling levels. We have assumed the following levels for the three formats: $\{-1, +1\}$ for NRZ, $\{-1, -1/3, +1/3, +1\}$ for PAM4, and $\{-1, -3/5, -1/5, +1/5, +3/5, +1\}$ for PAM6. Also, $k = 1, 5/9$, and $7/15$, respectively.

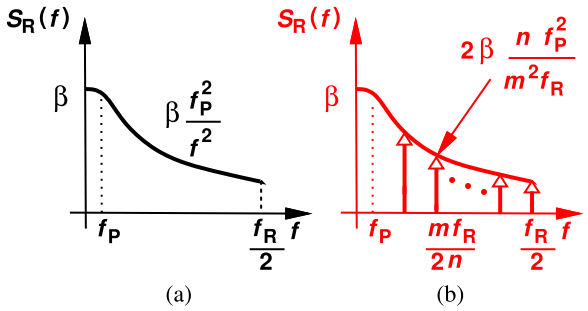

Fig. 4. (a) Spectrum of channel output, and (b) approximation of the spectrum with n equally-spaced impulses.

IV. Proposed Analysis

A. High-Loss Channels

For losses greater than roughly 20 dB at the Nyquist frequency, it is possible to approximate the TX/channel cascade by a white-noise generator followed by a first-order low-pass filter (LPF). The received signal spectrum is then viewed as shown in Fig. 4(a), where the power beyond $f_{Nyq} = f_R/2$ is neglected. Note that the filter 3-dB bandwidth is uniquely specified by the loss at f_{Nyq}. We have

$$S_R(f) = \frac{\beta}{1 + (f/f_P)^2}, \tag{6}$$

where f_P is the 3-dB bandwidth. The total signal power is approximately equal to $(\pi/2)\beta f_P$ if $f_{Nyq} \gg f_P$. Following the impulse approximations of Section II, we construct the spectrum depicted in Fig. 4(b), and neglect the JIN for frequency components below f_P. We decompose the spectrum from f_P to f_{Nyq} into n impulses and express the power of the m-th one as

$$\frac{A_m^2}{2} = 2\beta\frac{n}{m^2}\frac{f_P^2}{f_R}. \tag{7}$$

With the aid of (1), the total corresponding JIN power is now given by

$$\begin{aligned} P_{J,2} &= 4\pi^2\sigma_j^2\frac{m^2 f_R^2}{4n^2}\frac{2\beta n f_P^2}{m^2 f_R} \times n \\ &= 2\pi^2\sigma_j^2\beta f_P^2 f_R. \end{aligned} \tag{8}$$

The SNR for high-loss channels thus emerges as

$$\text{SNR}_\text{H} = \frac{(\pi/2)\beta f_P}{2\pi^2\beta f_P^2 f_R\sigma_j^2} = \frac{1}{4\pi f_P f_R\sigma_j^2}. \tag{9}$$

The remarkable point here is that, in comparison to the SNR in Eq. (2), this result replaces f_{in}^2 with $f_P f_R$: the greater the channel loss is, the lower f_P is and hence the higher the SNR will be. The difference between the two SNRs (in dB) can be written as

$$\Delta\text{SNR}_\text{H} = 10\log\frac{\pi f_R}{4f_P}. \tag{10}$$

This is the amount by which the jitter can be relaxed, $\Delta\sigma_j$. To arrive at a simple rule of thumb, we assume a channel loss of γ dB at f_{Nyq}, and use $\gamma \approx -20\log(2f_P/f_R)$ to obtain

$$\Delta\text{SNR}_\text{H} = \Delta\sigma_j = \frac{\gamma + 3.92}{2}\ \text{dB}. \tag{11}$$

This result allows us to still characterize RX ADCs by Nyquist-rate sinusoids and then simply apply a correction factor to ease the PLL jitter. For example, a loss of $\gamma = 30$ dB allows a 17-dB (sevenfold) increase in the rms jitter.

B. Low-Loss Channels

For channel losses below roughly 20 dB, two of our previous approximations begin to fail. First, f_P is no longer much less than f_{Nyq}. Second, our previous computation of the received signal power and noise loses it accuracy because the signal amplitude and slope at the ideal sampling points differ markedly from the overall average of these quantities (calculated using the spectrum).

As shown in the Appendix, the high-loss SNR can be revised for low-loss channels as follows:

$$\text{SNR}_\text{L} = \left(\frac{f_R}{2\pi f_P}e^{4\pi f_P/f_R}\right)\text{SNR}_\text{H} \tag{12}$$

$$= \frac{1}{8\pi^2 f_P^2 \sigma_j^2}e^{4\pi f_P/f_R}. \tag{13}$$

The term in parentheses in Eq. (12) serves as a simple yet accurate correction factor. In this case, Eq. (11) is rewritten as

$$\Delta\text{SNR}_\text{L} = \Delta\sigma_j = 10\log_{10}\frac{f_R^2 \times e^{4\pi f_P/f_R}}{8f_P^2}. \tag{14}$$

For example, a loss of 10 dB yields $\Delta\sigma_j = 15.6$ dB, suggesting that the PLL rms jitter can be relaxed by a factor of 6 compared to the bound dictated by (2).

C. General Channel

The compact and intuitive results expressed by (11) and (14) prove sufficient in most cases. Nonetheless, we can also develop more complete (and, inevitably, less intuitive) SNR equations. Denoting the received voltage by $V_R(t)$, we recognize that the jitter-induced noise power is given by

$$P_j = \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}\sigma_j^2\left[\frac{dV_R(t)}{dt}\right]^2, \tag{15}$$

which, from Parseval's theorem, reduces to

$$P_j = 4\pi^2\sigma_j^2\int_{-\infty}^{+\infty} f^2 S_R(f)df. \tag{16}$$

The received signal spectrum, $S_R(f)$, can be obtained by subjecting Eq. (5) to the channel's transfer function, $H(f)$, leading to

$$P_j = \frac{4k\pi^2\sigma_j^2}{f_R}\int_{-\infty}^{+\infty} f^2|H(f)|^2\left[\frac{\sin(\pi f/f_R)}{\pi f/f_R}\right]^2 df. \tag{17}$$

Similarly, the received signal power is written as

$$P_{sig} = \frac{k}{f_R}\int_{-\infty}^{+\infty}|H(f)|^2\left[\frac{\sin(\pi f/f_R)}{\pi f/f_R}\right]^2 df. \tag{18}$$

For a given $H(f)$, these integrals can be evaluated numerically. For the high-loss approximation described in Section IV-A, this general result reduces to that in Eq. (9). Note that σ_j^2 appears outside the integrals, implying that P_j does not depend on the shape of the clock's phase noise profile. This has been confirmed by simulations and also by [6].[1]

A key point arising from our work is that the jitter-induced noise is independent of the modulation scheme, and it should be compared only to the ADC's quantization noise. The results therefore apply to NRZ, PAM4, and PAM6 signaling.

D. Effect of CTLE

Since the RX ADC is often preceded by a CTLE, we wish to revise our previous results accordingly. Suppose the CTLE provides a boost factor of B at f_{Nyq}. We surmise that the lower overall loss translates to a proportionally greater f_P in the RX input spectrum. That is, we can simply scale f_P in (10) and (14) by a factor of B, arriving at

$$\Delta\text{SNR}_\text{H} = \Delta\sigma_j = 10\log\left(\frac{\pi f_R}{4f_P}\right) - \frac{B}{2} \tag{19}$$

$$\Delta\text{SNR}_\text{L} = \Delta\sigma_j = 10\log_{10}\left(\frac{f_R^2 \times e^{4\pi f_P/f_R}}{8f_P^2}\right) - \frac{B}{2}, \tag{20}$$

where B is expressed in dB. Even though the channel/CTLE cascade response may not behave as a first-order system and exhibit ripple, these approximations provide a reasonable accuracy (Section V-C).

V. Simulation Results

The framework of Fig. 3 serves as our simulation environment as well. The physical channel model is realized in Cadence and the RX processing in Python. The difference between $Y_1(t)$ and $Y_2(t)$ yields the jitter-induced noise and hence the SNR.

A. Maximum Tolerable Jitter

Circuit and system designers are primarily interested in the maximum tolerable clock jitter, $\sigma_{j,max}$, for a given ADC SNR penalty. Assuming an N-bit ADC and a 2-dB penalty, we use (8) to derive

$$\sigma_{j,max} = \frac{0.248 \times 10^{(\gamma/40)}}{2^N f_R}. \tag{21}$$

We assume $N = 7$ and compare the $\sigma_{j,max}$ values thus obtained with simulations. Figure 5 plots the results vs the symbol rate for PAM4 signals. The sine-wave plot assumes a frequency equal to the Nyquist rate.

Two key points emerge here. First, for a symbol rate of, e.g., 56 Gbaud (112 Gb/s), $\sigma_{j,max}$ must be as low as 28 fs according to the sine-wave model whereas it can be relaxed to 194 fs for a loss of 30-dB. Second, our model and simulation results display a discrepancy of at most 2-3 dB.

[1]Further, P_j does not depend upon the phase response of the channel transfer function.

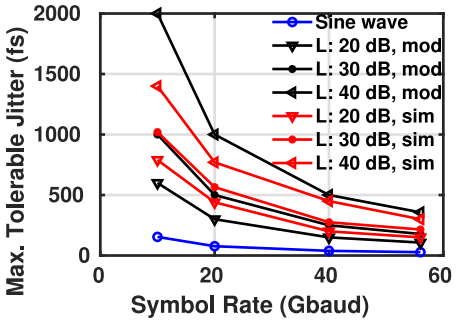

Fig. 5. Maximum tolerable jitter vs symbol rate estimated from our model, simulations, and the generic sinusoidal model.

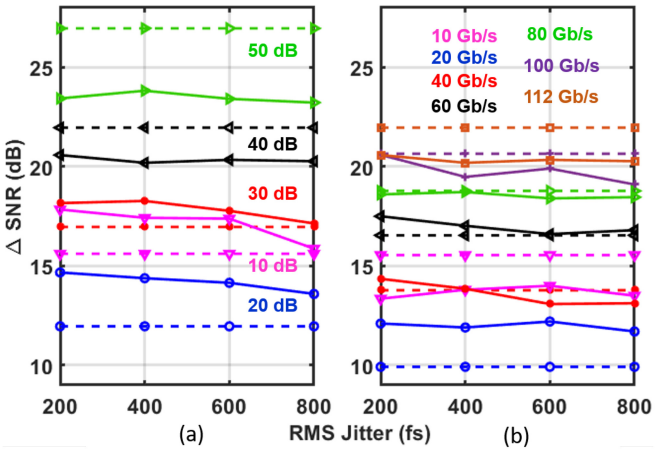

Fig. 6. ΔSNR vs jitter for (a) different channel losses for 112-Gb/s PAM4 data, (b) different data rates for PAM4 data and a loss of 40 dB at 28 GHz. (dashed lines: proposed models, solid lines: simulations).

B. General Results

We wish to examine the accuracy of our models in several other scenarios. To this end, we compare the ΔSNR values predicted by (11) and (14) to those observed in simulations. We use these two equations for channel losses greater or less than 20 dB, respectively.

Three sets of simulations are performed with different losses, data rates, and modulation schemes. Figure 6(a) plots the first set vs the clock jitter for a PAM4 data rate of 112 Gb/s and losses ranging from 10 dB to 50 dB. We observe that our equations incur a maximum error of 3.7 dB. Figure 6(b) repeats the results for data rates ranging from 10 Gb/s to 112 Gb/s and a loss of 40 dB at 28 GHz, revealing a maximum error of about 2 dB. Figure 7 presents the results for NRZ, PAM4, and PAM6 signaling for a loss of 30 dB and 56 Gbaud symbol rate. As expected, the effect of jitter on the SNR is fairly independent of the modulation scheme.

C. Effect of Notches and CTLE

The notches in the channel's frequency response arise from impedance mismatches and translate to reflections. From our simulations, we find that the $\Delta\sigma_j$ predictions of (11) and (14) are relatively accurate for notches with a depth up to about 4 dB. For deeper notches, Eq. (17) can be used.

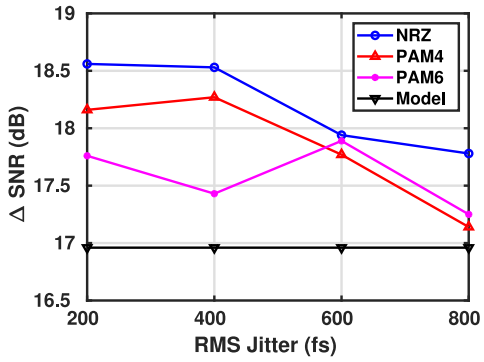

Fig. 7. ΔSNR vs jitter with a symbol rate of 56 Gbaud and channel loss of 30 dB.

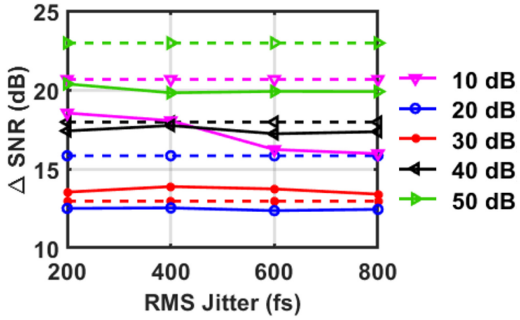

Fig. 8. ΔSNR vs jitter with a CTLE preceding the ADC for 112-Gb/s PAM4 data. (dashed lines: proposed models, solid lines: simulations).

Figure 8 plots ΔSNR for a CTLE boost of 8 dB and a PAM4 data rate of 112 Gb/s. It is noted that the estimates provided by (19) and (20) are fairly accurate.

VI. Conclusion

This brief analyzes the effect of ADC clock jitter on wireline receivers in the presence of lossy channels. Compact, intuitive equations are derived that prescribe the SNR and its penalty for a given loss, demonstrating that the ADC can tolerate a significantly higher jitter than previous models suggest.

Appendix
Case of Low-Loss Channel

Approximating the channel by a one-pole system and denoting the symbol period by T_S, we examine the pulse response, $y(t)$, and express it as $[1-e^{-t/\tau}]$ for $0 \le t \le T_S$ and as $(1-e^{-T_S/\tau})e^{-(t-T_S)/\tau}$ for $t \ge T_S$. If $y(t)$ is sampled at $t = T_S$, its average power is given by $E[|y(nT_S)|^2] = (1-e^{-T_S/\tau})^2$. This value is about unity if $\tau \ll T_S$. On the other hand, the entire (continuous-time) power of $y(t)$ between $T_S/2$ and $3T_S/2$ (the effect of ISI is neglected in this time window) is approximately half of this value.

To compute the jitter-induced noise power, we first write

$$E\left[\left(\frac{dy}{dt}|_{nT_S}\right)^2\right] = \frac{1}{\tau^2}e^{-2T_S/\tau} \tag{22}$$

for the sampled signal and

$$E\left[\left(\frac{dy}{dt}\right)^2\right] = \frac{1}{2\tau T_S} \tag{23}$$

for the continuous-time counterpart. The high-loss SNR is now corrected by the two factors found above, namely, the factor of 2 for the signal power and the factor of $[1/(2\tau T_S)]e^{2T_S/\tau}$ for the slope. It follows that

$$\mathrm{SNR_L} = \left(\frac{f_R}{2\pi f_P} e^{2\pi f_P/f_R}\right)\mathrm{SNR_H}, \tag{24}$$

where τ is replaced with $1/(2\pi f_P)$.

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