A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology

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***Abstract*—This paper describes the design of a CMOS frequency synthesizer targeting wireless local-area network applications in the 5-GHz range. Based on an integer-N architecture, the synthesizer produces a 5.2-GHz output as well as the quadrature phases of a 2.6-GHz carrier. Fabricated in a 0.4-μm digital CMOS technology, the circuit provides a channel spacing of 23.5 MHz at 5.2 GHz while exhibiting a phase noise of −115 dBc/Hz at 2.6 GHz and −100 dBc/Hz at 5.2 GHz (both at 10-MHz offset). The reference sidebands are at −53 dBc at 2.6 GHz, and the power dissipation from a 2.6-V supply is 47 mW.**

***Index Terms*—Frequency dividers, oscillators, phase-locked loops, RF circuits, synthesizers, wireless transceivers.**

I. Introduction

WIRELESS local area networks (WLAN's) provide great flexibility in the communication infrastructure of environments such as hospitals, factories, and large office buildings. While WLAN standards in the 2.4-GHz range have recently emerged in the market, the data rates supported by such systems are limited to a few megabits per second. By contrast, a number of standards have been defined in the 5-GHz range that allow data rates greater than 20 Mb/s, offering attractive solutions for real-time imaging, multimedia, and high-speed video applications. One of these standards is high-performance radio LAN (HIPERLAN) [1].

HIPERLAN operates across 5.15–5.30 GHz and provides a channel bandwidth of 23.5 MHz with Gaussian minimum shift keying (GMSK) modulation. The receiver sensitivity must exceed −70 dBm.

This paper presents the design of a frequency synthesizer for 5-GHz WLAN applications. To target realistic specifications, HIPERLAN is chosen as the framework. Employing an integer-N architecture, the circuit generates a 5.2-GHz output for the transmit path and the quadrature phases of a 2.6-GHz carrier for the receive path. Realized in a 0.4-μm CMOS technology, the synthesizer provides a channel spacing of 23.5 MHz while dissipating 47 mW from a 2.6-V supply. The phase noise at 10-MHz offset is equal to −115 dBc/Hz at 2.6 GHz and −100 dBc/Hz at 5.2 GHz.

Section II of this paper describes the synthesizer environment and general issues, and Section III introduces the synthesizer architecture. Section IV presents the design of each building block, and Section V summarizes the experimental results.

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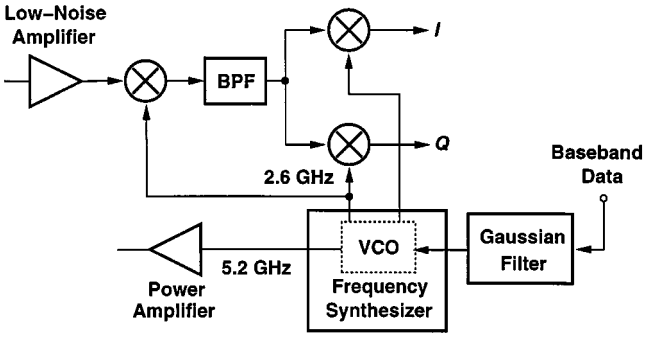

Fig. 1. Transceiver architecture.

II. Synthesizer Environment

The design of a 5-GHz synthesizer in a 0.4-μm CMOS technology presents many difficulties at both the architecture and the circuit levels. The high center frequency of the voltage-controlled oscillator (VCO), the poor quality of inductors due to skin effect and substrate loss, the limited tuning range, the nonlinearity of the VCO input/output characteristic, the high speed required of the feedback divider, the mismatches in the charge pump, and the implementation of the loop filter are among the issues encountered in this design.

A 0.4-μm-long NMOS transistor in this technology achieves an f_T of less than 15 GHz with a gate–source overdrive voltage $(V_{\rm GS} - V_{\rm TH})$ of about 400 mV, a typical value in this design. Also, a 5-nH inductor exhibits a self-resonance frequency of 6.5 GHz and a Q of 5 at this frequency, indicating that skin effect and substrate loss are much more significant at 5.2 GHz than at 2.6 GHz. The technology offers no high-density linear capacitors, creating difficulty in the design of the loop filter.

The foregoing limitations make it necessary that the transceiver and the synthesizer be designed concurrently so as to relax some of the synthesizer requirements. Fig. 1 shows the transceiver architecture and its interface with the synthesizer. The receive path consists of two downconversion stages, each using a local oscillator (LO) frequency of 2.6 GHz, and the transmit path modulates the VCO by the Gaussian-filtered baseband data, producing a GMSK output.

An important feature of this architecture is that the synthesizer is shared between the transmitter and the receiver, reducing the system complexity substantially. This is possible because HIPERLAN incorporates time-division duplexing (TDD). Also, the transceiver requires the generation of the quadrature phases of the 2.6-GHz carrier rather than the 5.2-GHz output, a task readily accomplished by the synthesizer itself.

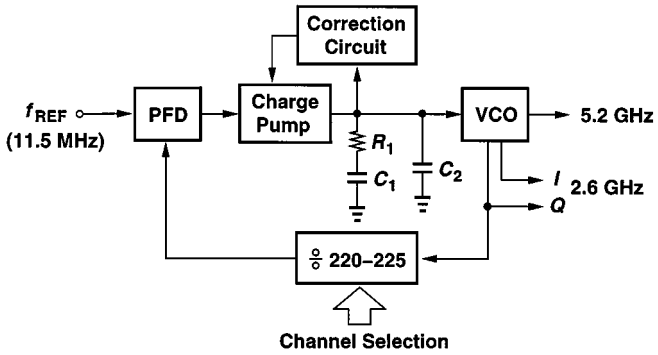

Fig. 2. Synthesizer architecture.

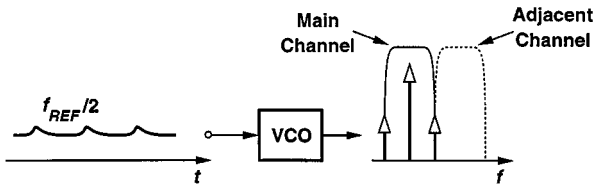

Fig. 3. Position of reference sidebands.

III. Synthesizer Architecture

The synthesizer is based on an integer-N phase-locked loop architecture (Fig. 2). The feedback divider senses the 2.6-GHz output because it is not possible to design a dual-modulus divider in 0.4-μm CMOS technology that operates at 5.2 GHz reliably. Controlled by the digital channel-select input, the ÷220–225 circuit generates frequency steps of $f_{\rm REF} = 11.75$ MHz in the 2.6-GHz band and 23.5 MHz in the 5.2-GHz band.

A critical issue in the architecture of Fig. 2 is the nonlinearity of the VCO characteristic, i.e., the variation of the VCO gain, $K_{\rm VCO}$, with the control voltage $V_{\rm cont}$. This effect manifests itself in the loop settling behavior as well as the magnitude of the phase noise and reference sidebands at the output. The problem is partially resolved through the use of a correction circuit that adjusts the charge-pump current according to the value of $V_{\rm cont}$ [2].

An interesting property of the architecture of Fig. 2 is the position of the reference spurs with respect to the main carrier. Since the reference frequency is half the channel spacing, such spurs fall at the *edge* of the channel rather than at the center of the adjacent channel for both 2.6- and 5.2-GHz outputs (Fig. 3). Since the interference energy received by the antenna is small at the edge, the maximum allowable magnitude of the spurs can be quite higher than if the reference frequency were equal to 23.5 MHz.

IV. Building Blocks

A. VCO

The VCO core is based on two 2.6-GHz coupled oscillators operating in quadrature, as shown in Fig. 4(a) [3], [4]. The fully differential topology of each oscillator raises the possibility of sensing the common-source nodes A, B, C, or D as the 5.2-GHz output. In fact, since the 2.6-GHz oscillators operate in quadrature, the waveforms at A and B (or C and D) are 180° out of phase, thereby serving as a differential output at 5.2 GHz. With proper choice of device dimensions and bias current, a differential swing of 0.5 V can be achieved at this port. Note that if a frequency doubler were used, the output would be single-ended and difficult to convert to differential form at such a high frequency.

The tuning of the oscillator poses several difficulties: the varactor diode must exhibit a small series resistance and remain reverse-biased even with large swings in the oscillator, and the varactor capacitance must be large enough to yield the required tuning range, but at the cost of increasing the power dissipation or the phase noise. This design incorporates a p^+-n^+ diode inside an n-well and strapped with metal to reduce the n-well series resistance [4]. Such a structure suffers from a large parasitic n-well/substrate capacitance, making it desirable to connect the anode of the diode to the oscillator. This is accomplished as illustrated in Fig. 4(b), where only one of the two oscillators is shown for clarity. Here, the control voltage varies the dc potential at nodes X and Y by varying the on-resistance of M_3.

However, the sharp variation of the on-resistance of M_3 leads to significant change in the gain of the VCO. To make the transition smoother, another transistor, M_4, in series with a resistor is added as shown in Fig. 4(c). Transistor M_5 serves as a clamp, keeping the tail current source in saturation. Otherwise, the oscillator may turn off during synthesizer loop transients.

Since the minimum voltage at node A is only a few hundred millivolts above ground, an NMOS differential pair cannot directly sense the 5.2-GHz signal at this node. Instead, a common-gate stage is used [Fig. 4(d)]. But if V_b is constant, then M_6 turns off for low values of $V_{\rm cont}$. Modifying the circuit as shown in Fig. 4(e) ensures that the common-gate stage carries a constant bias current across the full tuning range.

The choice of the inductors and capacitance of the varactors entails a compromise between the phase noise and the tuning range. In this design, 7-nH inductors are used, each contributing a parasitic capacitance of 120 fF. The cross-coupled transistors are relatively wide to ensure startup, yielding approximately 175 fF of gate-source capacitance. The differential pairs coupling the oscillators also load the tank. As a result, the varactor capacitance for 2.6-GHz operation must not exceed 160 fF.

The inductors are realized as stacked spirals [5] made of metal 4 and metal 3 with a width of 6 μm. Since the tuning range is inevitably narrow, it is critical to predict the oscillation frequency accurately. A distributed model is used for each inductor, yielding an error of only a few percent in the measured frequency of oscillation.

B. Frequency Divider

The design of a 2.6-GHz programmable divider with a reasonable power dissipation in 0.4-μm CMOS technology is quite difficult. A number of circuit techniques are introduced in this work to ameliorate the power–speed tradeoff.

The divider is based on a pulse-swallow topology. Shown in Fig. 5(a) is a conventional implementation, consisting of a dual-modulus prescaler, a fixed-ratio program counter, and a programmable swallow counter. The RS latch is typically included in the swallow counter and is drawn explicitly here for clarity. The prescaler begins the operation by dividing by $N+1$ until the swallow counter is full. The RS latch is then set, changing

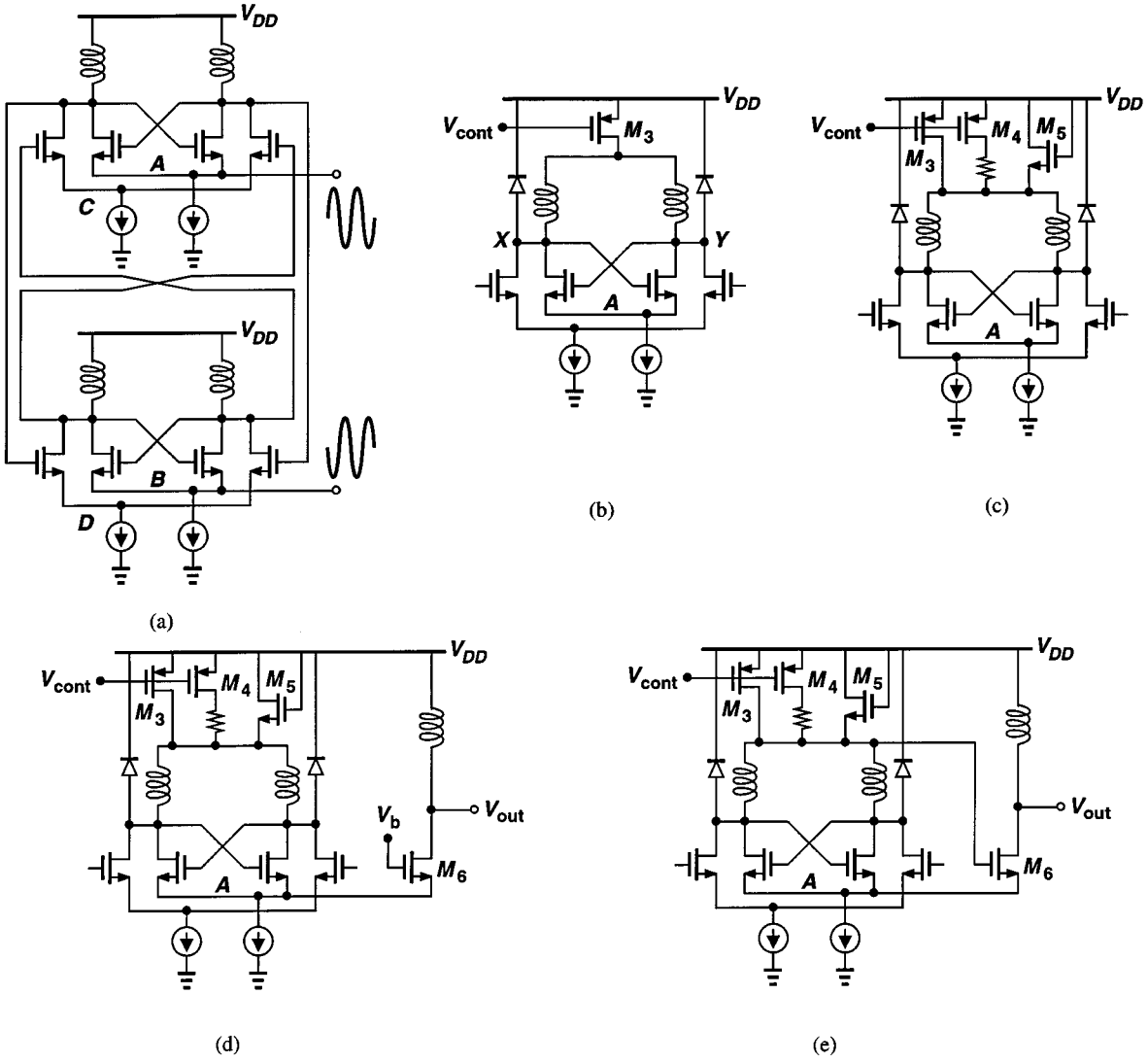

Fig. 4. Evolution of the VCO topology.

the prescaler modulus to N and disabling the swallow counter. The division continues until the program counter is full and the RS latch is reset. The overall divide ratio is therefore equal to $NP + S$.

The pulse-swallow divider used in this work is shown in Fig. 5(b). Here, the RS latch is followed by a D flip-flop to allow pipelining of the prescaler modulus control signal. This modification is justified below. The overall divide ratio is now equal to $NP + S$+1. A critical decision in the design of the divider is the choice between low-swing current-steering logic and rail-to-rail CMOS logic. Simulations of the circuit with various values of N, P, and S indicate that the minimum power dissipation occurs if the prescaler incorporates current steering, its output is converted to rail-to-rail swings, and the remainder of the circuit incorporates standard dynamic and static CMOS logic. The use of current steering in the prescaler also obviates the need for large oscillator swings, saving power in the VCO buffer.

The design of the 8/9 prescaler for 2.6-GHz operation presents a great challenge. Shown in Fig. 6, the prescaler consists of a synchronous ÷2/3 circuit and two asynchronous ÷2 circuits. In a conventional ÷2/3 realization [Fig. 7(a)], flip-flop FF_1 is loaded by an OR gate, whereas FF_2 is loaded by FF_1, an AND gate, and an output buffer. Since FF_2 limits the speed, the fanout of three inherent to this topology translates to substantial power dissipation. Furthermore, if the divider is implemented by current-steering circuits, the AND gate requires stacked logic and hence level-shift source followers. Both of these issues intensify the power–speed tradeoff.

The ÷2/3 circuit used in this work is shown in Fig. 7(b). Here, FF_2 is loaded by a NOR gate and FF_1 by a NOR gate and a buffer. Simulations indicate that the reduction of the load capacitance of FF_2 increases the maximum operating speed by approximately 40%.

The NOR/flip-flop combination is realized as depicted in Fig. 8. The resistors are made of n-well, and the bias voltage V_b is generated to fall midway between the high and low levels of inputs A and B. The output of the prescaler drives a differential to single-ended converter, producing rail-to-rail swings for the remainder of the divider.

The divider of Fig. 5 incorporates pipelining for the prescaler modulus control, thereby relaxing the minimum delay require-

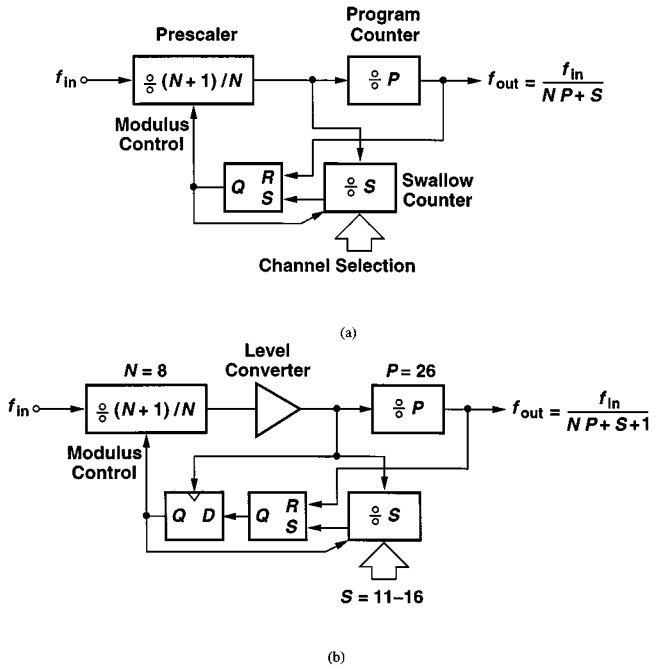

Fig. 5. Pulse swallow divider. (a) Conventional topology. (b) Addition of pipelining in the prescaler modulus control path.

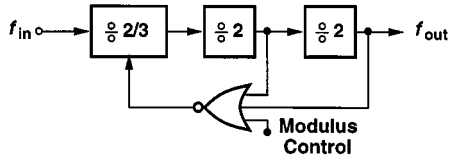

Fig. 6. Prescaler.

ment in this path. Fig. 9 illustrates the issue. When the $\div 9$ operation of the prescaler is finished, the circuit would have at most seven cycles of $V_{\rm in}$ to change the modulus to eight. In this particular prescaler, the timing budget is actually about five input cycles—approximately 1.9 ns. Thus, with no pipelining, the last pulse generated by the prescaler in the $\div 9$ mode must propagate through the level converter, the first $\div 2$ stage in the swallow counter, the subsequent logic, the RS latch, and the three-input NOR gate in less than 1.9 ns. Such a delay constraint necessitates the use of current steering in this path, raising the power dissipation and complicating the design. With pipelining, on the other hand, the maximum tolerable delay increases to about eight input cycles—approximately 3.1 ns.

C. Charge Pump and Loop Filter

Fig. 10 shows the charge pump [6] and the loop filter. Here, M_3 and M_4—rather than M_1 and M_2—operate as switches. Thus, the problem of transistor charge injection and clock feedthrough to the output is somewhat alleviated. In addition to these errors, up and down currents produced by the charge pump may also create ripple on the control voltage. Since in locked condition, M_3 and M_4 turn on at every phase comparison instant, any mismatch between their magnitudes, duration, or absolute timing results in a net current that is drawn from the loop filter.

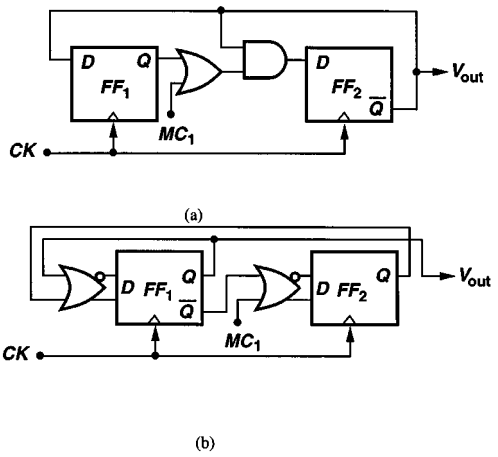

Fig. 7. Divide-by-2/3 circuit: (a) conventional topology and (b) circuit used in this work.

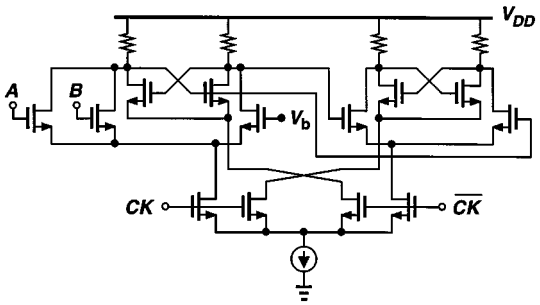

Fig. 8. Implementation of NOR/flip-flop combination.

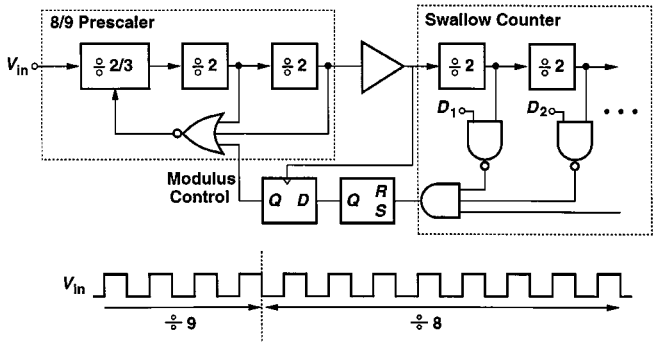

Fig. 9. Pipelining in the prescaler modulus control path.

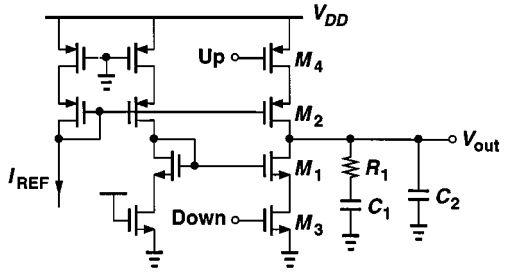

Fig. 10. Charge pump and loop filter.

To appreciate the significance of these effects, let us consider some typical values in this design. If the reference sidebands are to be 50 dB below the carrier, then with $K_{\rm VCO,max} \approx 1$ GHz/V and $f_{\rm REF} = 11.75$ MHz, the ripple amplitude must not exceed

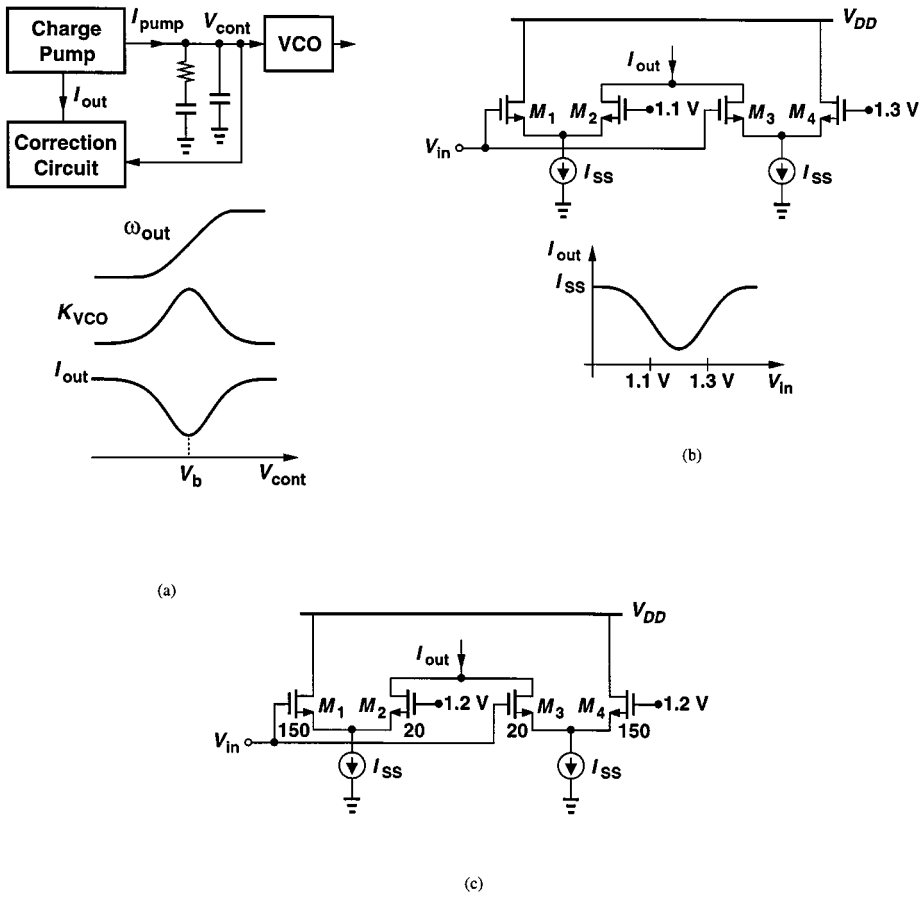

Fig. 11. (a) Addition of correction circuit to charge pump. (b) Simple folding circuit. (c) Folding circuit with one reference voltage.

75 μV.[1] This indicates that great attention must be paid to the design of the phase/frequency, the charge pump, and the loop filter so as to minimize the above errors.

Another source of ripple in the control voltage is the low output impedance of M_1 and M_2 in Fig. 10, especially as $V_{\rm cont}$ reaches within a few hundred millivolts of the rails. This effect creates additional mismatch between the up and down currents as a function of $V_{\rm cont}$, potentially leading to larger reference sidebands near the ends of the tuning range. Transistors M_3 and M_4 degenerate M_1 and M_2, respectively, alleviating this issue (another advantage of this topology over the standard charge-pump configuration).

The addition of C_2 in the circuit of Fig. 10 to suppress the ripple potentially degrades the stability of the loop. Simulations suggest that for $C_2 \leq 0.2C_1$, the settling time increases negligibly. In this design, $C_1 = 5$ pF, $C_2 = 1$ pF, and $R_1 = 86\ \text{k}\Omega$. The two capacitors can be realized by either MOSFET's or poly-metal sandwiches, a choice determined by the control voltage range. To achieve the maximum tuning range, $V_{\rm cont}$ must approach the supply and ground rails, demanding a reasonable capacitor linearity across this range. MOS capacitors, however, exhibit substantial change as their gate-source voltage falls below the threshold. Even a parallel combination of an NMOS capacitor (connected to ground) and a PMOS capacitor (connected to $V_{\rm DD}$) suffers from a two-fold variation as $V_{\rm cont}$ goes from zero to $V_{\rm DD}$. For this reason, C_1 and C_2 are formed as poly-metal sandwiches (albeit with much less density than MOS capacitors).

Another issue in the design of the loop filter of Fig. 10 relates to the thermal noise produced by R_1. Low-pass filtered by C_1 and C_2, this noise modulates the VCO, raising the output phase noise. The thermal noise on the control voltage per unit bandwidth is given by

$$V_{n,\rm cont}^2 = \left(\frac{C_1}{C_1+C_2}\right)^2 \frac{1}{1+\left(R_1\dfrac{C_1C_2}{C_1+C_2}\omega\right)^2} V_{n,R1}^2 \quad (1)$$

where $V_{n,R1}^2$ denotes the noise density of R_1. From the narrow-band frequency modulation theory [8], we know that if a sinusoid with a peak amplitude A_m and frequency ω_m modulates a VCO, the output sidebands fall at ω_m rad/s below and above the carrier frequency and exhibit a peak amplitude of $A_m K_{\rm VCO}/(2\omega_m)$. Approximating the noise per unit bandwidth in (1) by a sinusoid, we obtain the output relative phase noise per unit bandwidth at an offset frequency $\Delta\omega$ as

$$\frac{P_n}{P_{\rm carrier}} = \left(\frac{C_1}{C_1+C_2}\right)^2 \frac{2kTR_1}{1+\left(R_1\dfrac{C_1C_2}{C_1+C_2}\Delta\omega\right)^2} \times \left(\frac{K_{\rm VCO}}{2\Delta\omega}\right)^2. \quad (2)$$

[1]The ripple is approximated by a sinusoid here. In a more rigorous method, the ripple can be expressed as a Fourier series [7].

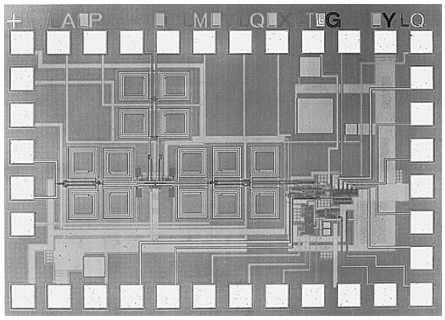

Fig. 12. Die photograph.

With the values chosen in this design, the output phase noise reaches -138 dBc/Hz at 10-MHz offset for $K_{\mathrm{VCO,max}} = 1$ GHz/V. While it is desirable to reduce the value of R_1, the required increase in C_1 leads to a severe area penalty because of the low density of the poly-metal capacitors. Note that since the stability factor $\zeta = (1/2)R_1\sqrt{C_1 K_{\mathrm{VCO}} I_{\mathrm{pump}}/(2\pi)}$, if R_1 is, say, halved, then C_1 must be quadrupled to maintain ζ constant (for a given charge-pump current).

D. Correction Circuit

The gain of the VCO varies substantially across the tuning range, resulting in considerable change in the settling behavior. As depicted in Fig. 11(a), it is desirable to vary the charge-pump current, I_{pump}, such that the product ofK_{VCO} and I_{pump} and hence ζ remain relatively constant. Rather than use piecewise linearization [2], this work incorporates an analog folding technique. Fig. 11(b) shows a possible solution. Here M_1 and M_3 are off if V_{in} is well below 1.1 V and hence $I_{\mathrm{out}} = I_{\mathrm{SS}}$. As V_{in} approaches 1.1 V, M_1 turns on while M_3 is off. Thus, I_{out} drops, reaching a low value as M_1 carries most of I_{SS} and M_3 a negligible current. As V_{in} approaches and exceeds 1.3 V, M_3 turns on and I_{out} eventually returns to I_{SS}. This design actually utilizes the topology shown in Fig. 11(c), where only one reference voltage is required and each differential pair provides a built-in offset by virtue of skewed device dimensions. The characteristic is similar to that shown for Fig. 11(b), with I_{out} driving the current mirrors in the charge pump.

The reference voltage of 1.2 V in Fig. 11(c) assumes that the gain of the VCO reaches its maximum at $V_{\mathrm{cont}} = 1.2$ V. This value is somewhat process- and temperature-dependent, limiting (according to simulations) the suppression of the VCO nonlinearity to about one order of magnitude.

V. Experimental Results

The frequency synthesizer has been fabricated in a 0.4-μm digital CMOS technology. All of the inductors and capacitors are included on the chip. Fig. 12 is a photograph of the die, which measures 1.75×1.15 mm^2. The circuit has been tested with a 2.6-V supply.

Figs. 13(a) and (b) depict the output spectra in the locked condition. The phase noise at 10-MHz offset is equal to -115 dBc/Hz at 2.5 GHz and -100 dBc/Hz at 5.2 GHz. A significant part of the phase noise at 5.2 GHz is attributed to the considerable loss of the output 50-Ω buffer. Fig. 14 shows the 2.6-GHz output along with the reference sidebands. The sidebands are approximately 53 dB below the carrier. For the 5.2-GHz output, the sidebands are buried under the noise floor.

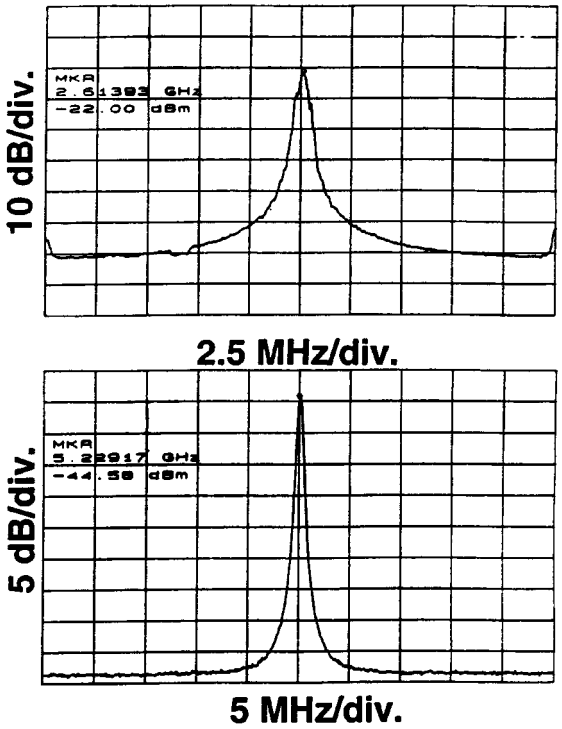

Fig. 13. Measured spectra at 2.6 and 5.2 GHz in locked condition.

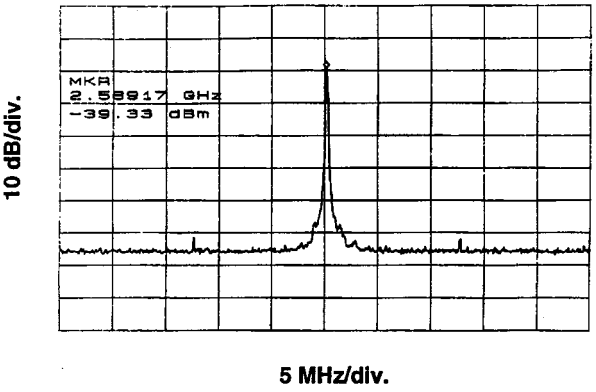

Fig. 14. Measured spectrum at 2.6 GHz.

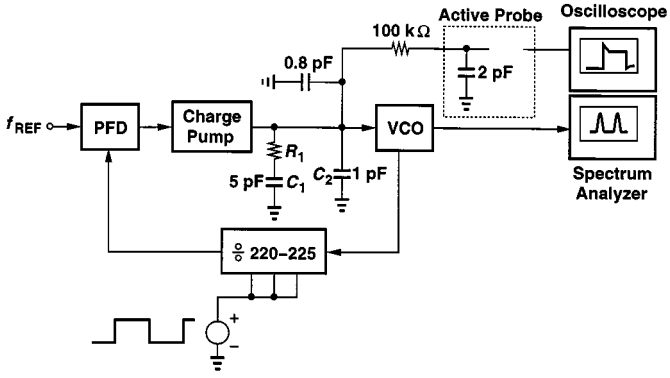

Fig. 15. Setup for settling time measurement.

The settling behavior of the synthesizer has also been studied. Fig. 15 illustrates the setup, where the modulus of the feedback

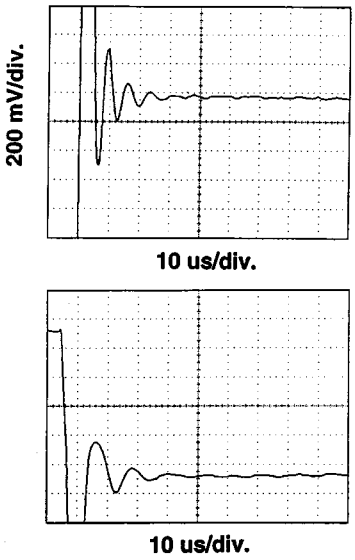

Fig. 16. Control voltage during loop settling.

TABLE I
SYNTHESIZER PERFORMANCE

Output Frequency	**2.6 GHz/5.2 GHz**
Phase Noise @ 10–MHz Offset	**–110 dBc/Hz @ 2.6 GHz –100 dBc/Hz @ 5.2 GHz**
Sidebands	**–55 dBc**
Power Dissipation	
VCO	**30 mW**
Divider, etc.	**17 mW**
Total	**47 mW**
Supply Voltage	**2.6 V**
Area	**1.75 mm x 1.15 mm**
Technology	**0.4– μm CMOS**

divider is switched periodically and the control voltage is monitored. The 0.8-pF capacitor results from the trace on the printed circuit board, and the active probe presents an input capacitance of 2 pF. Since $C_1 = 5$ pF and $C_2 = 1$ pF, the addition of these parasitics markedly degrades the stability. Therefore, a 100-kΩ resistor is placed in series with the active probe to mimic the role of R_1 and C_1. The low-pass filter thus formed has a corner frequency comparable to the loop bandwidth, and the 0.8-pF capacitor still produces ringing in the time response. Fig. 16 shows the measured control voltage, indicating a settling time on the order of 40 μs.

Table I summarizes the measured performance of the synthesizer.

VI. CONCLUSION

The speed and quality of the devices available in an IC technology directly affect the choice of transceiver architectures, synthesizer topologies, and circuit configurations. In order to optimize the overall system performance, the transceiver and the synthesizer must be designed concurrently, with particular attention to the frequency planning.

Designing a multigigahertz synthesizer in 0.4-μm CMOS technology necessitates circuit techniques such as: 1) a quadrature VCO with inherent frequency doubling, 2) a dual-modulus divider with equalized fanout, 3) pipelining in pulse-swallow counters, and 4) use of folding stages to compensate for nonlinearity in the VCO characteristic.

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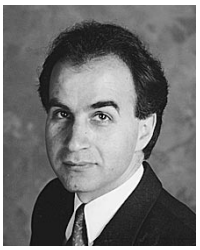

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