A New Transceiver Architecture for the 60-GHz Band

Ali Parsa, *Member, IEEE*, and Behzad Razavi, *Fellow, IEEE*

***Abstract*—A new "half-RF" architecture incorporates a polyphase filter in the signal path to allow the use of a local oscillator frequency equal to half the input frequency. The receiver performs 90° phase shift and two downconversion steps to produce quadrature baseband outputs. The transmitter upconverts the quadrature baseband signals in two steps, applies the results to a polyphase filter, and sums its outputs. Each path employs a dedicated 30-GHz oscillator and is fabricated in 90-nm CMOS technology. The receiver achieves a noise figure of 5.7–7.1 dB and gain/phase mismatch of 1.1 dB/2.1° while consuming 36 mW. The transmitter produces a maximum output level of −7.2 dBm and an image rejection of 20 dB while drawing 78 mW.**

***Index Terms*—Half-RF architecture, low-noise amplifier, mm-wave transceiver, polyphase filter, quadrature LO, synthesizer, mixer, transceiver architecture.**

I. Introduction

RECENT developments in millimeter-wave CMOS systems have begun to address the integration of building blocks to form transceivers [1]–[4]. In addition to generic challenges such as high-frequency operation and low-noise design, the implementation of transceivers at these frequencies must deal with three critical issues related to the local oscillator (LO): generation, division, and distribution [3]. It is therefore important to develop "synthesizer-friendly" transceivers so as to alleviate these issues.

This paper introduces a 60-GHz transceiver architecture that employs a 30-GHz LO without quadrature phases or frequency multiplication, greatly simplifying the three tasks mentioned above [4]. Specifically, the proposed concept leads to the lowest reported power for a 60-GHz receiver including an LO and generating quadrature baseband outputs and also a 60-GHz transmitter including an LO and upconverting quadrature baseband inputs.

Section II of the paper compares a number of transceiver architectures and describes their drawbacks. Section III introduces the proposed receiver architecture and the design of its building blocks. Section IV deals with the transmit path, and Section V presents the experimental results.

II. Comparison of Architectures

The LO-related challenges prove so severe at millimeter-wave frequencies that the choice of the receive (RX) and transmit (TX) topologies becomes closely intertwined with the synthesizer design. For example, the direct-conversion receiver shown in Fig. 1(a) requires generation of quadrature LO phases at 60 GHz, a difficult task because inductor Q's begin to saturate and varactor Q's are likely to fall to low levels at these frequencies. For example, [5] reports a Q of 12 for 180-pH inductors at 60 GHz and [6] a Q of 17 for 400-pH inductors at 50 GHz. The division and distribution of the 60-GHz LO also pose critical challenges [3].

To ameliorate these difficulties, a direct-conversion receiver can employ a 30-GHz LO and a frequency doubler [Fig. 1(b)]. While simplifying the task of division, this approach suffers from other drawbacks: 1) CMOS doublers tend to be quite lossy at these frequencies, raising the LO noise floor, necessitating post-amplification to achieve sufficient swings, and consuming additional inductors; 2) typical doubler topologies do not produce quadrature outputs, calling for additional (lossy) quadrature separation stages; and 3) the distribution of the 60-GHz quadrature phases around large layout geometries such as inductors still proves difficult.

The generation and distribution of quadrature phases can be eased by opting for a heterodyne architecture. Fig. 1(c) illustrates a general case employing Nf_{osc} for the first downconversion and f_{osc}/M for the second, thus requiring $f_{osc} = f_{in}M/(MN+1)$. This architecture must deal with the loss of the frequency multiplier and the problem of image rejection. For example, the receiver in [7] incorporates $N = 3$ and $M = 2$, placing the image at $5f_{in}/7$. Thus, for $f_{in} = 64$ GHz, the image lies at 45.7 GHz, experiencing only some attenuation if the front end must accommodate frequencies as low as 57 GHz. As another example, the receiver in [2] uses $f_{osc} = 29$ GHz and $N = 2$, thereby suffering from an *in-band* image. Consequently, the image thermal noise produced by the antenna, the LNA, and the mixer is downconverted to the intermediate frequency (IF), raising the receiver noise figure by about 3 dB. For the receiver in [3], $N = 1$, $M = 2$, and hence $f_{\rm LO} = 2f_{in}/3$. Located at $f_{in}/3$, the image is suppressed by the selectivity of the antenna and the RF front end. Nevertheless, $f_{\rm LO}$ is still relatively high.

The foregoing observations apply to transmitters as well. Direct upconversion entails similar issues with respect to I/Q generation (from a 60-GHz LO or a multiplier), division, and distribution. Two-step upconversion must deal with the problem of image (if the second upconversion does not employ a single-sideband mixer), which can corrupt the transmitted signal constellation, thus raising the error vector magnitude.

Fig. 2(a) shows a transceiver architecture that relaxes the LO-related issues while avoiding frequency multiplication [8]. Placing the image around zero, this approach incorporates the lowest possible LO frequency and provides a "clean" frequency

Manuscript received May 28, 2008; revised November 13, 2008. Current version published February 25, 2009.

A. Parsa was with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA. He is now with Broadcom Corporation, San Diego, CA 92128 USA.

B. Razavi is with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA (e-mail: razavi@ee.ucla.edu).

Digital Object Identifier 10.1109/JSSC.2008.2012368

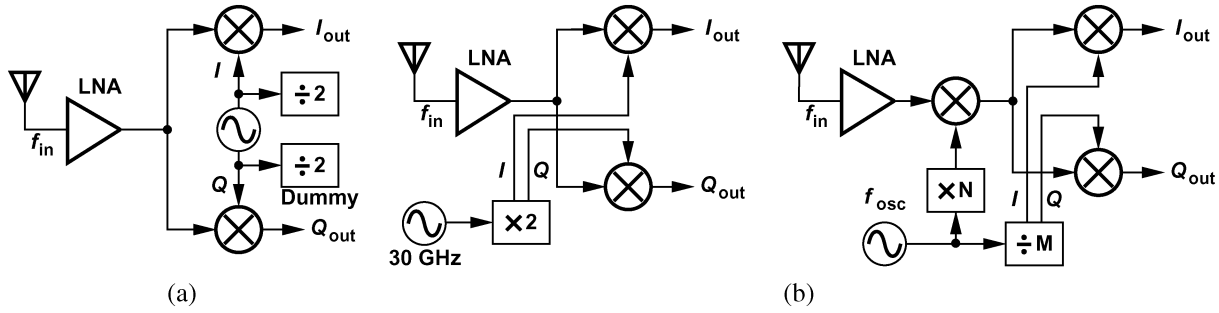


Fig. 1. (a) Generic direct-conversion receiver, (b) direct-conversion receiver with frequency doubler, (c) heterodyne receiver with frequency multiplier and divider.

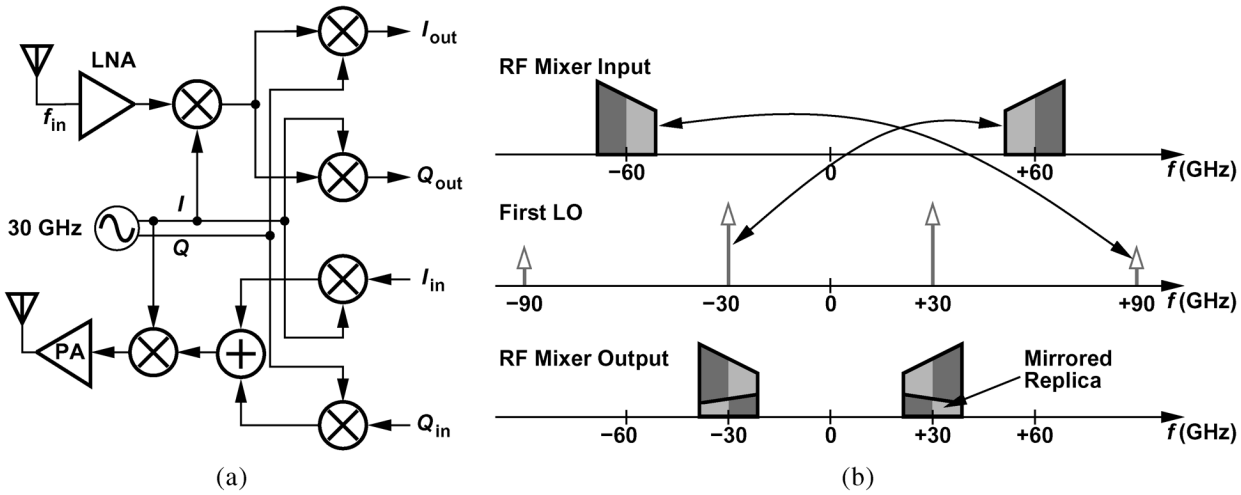


Fig. 2. (a) Half-RF heterodyne transceiver architecture, and (b) receiver spectra.

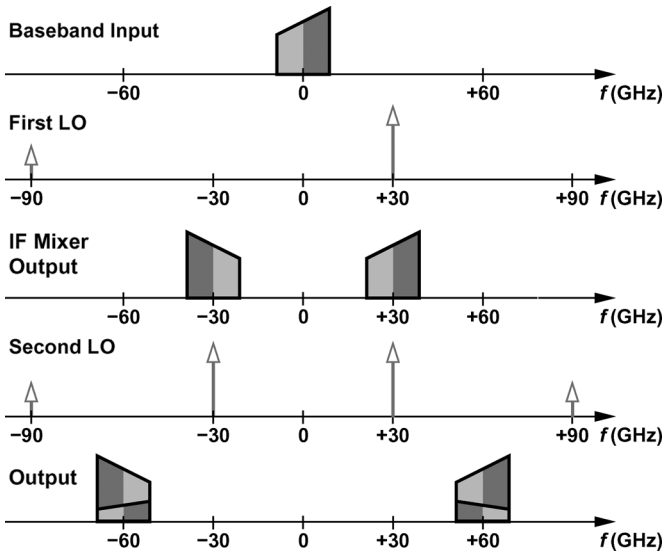


Fig. 3. Half-RF transmitter spectra.

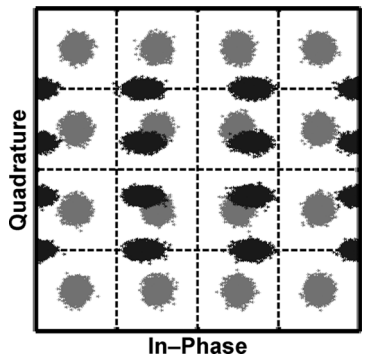


Fig. 4. 16-QAM constellations of ideal and half-RF receivers.

plan and a compact design. This "half-RF" architecture, however, exhibits a number of drawbacks.

The first drawback relates to the third harmonic of the LO. Illustrated in Fig. 2(b) for the receive path, this effect manifests itself if an asymmetrically-modulated input is mixed with $f_{\rm LO} = 30$ GHz and $3f_{\rm LO} = 90$ GHz. The latter also down-converts the signal to $f_{IF} = 30$ GHz but superimposes on the desired channel its "mirrored replica," a corruption that cannot be undone by subsequent stages. Similarly, as shown in Fig. 3 for the transmit path, a 30-GHz IF signal is mixed with $f_{\rm LO}$ and $3f_{\rm LO}$, thereby experiencing a mirrored replica as it appears at 60 GHz. Since hard switching in the mixers inevitably yields a third harmonic for the LO, and since most modulation schemes exhibit asymmetric spectra, this phenomenon proves serious.

The effect of the third harmonic can also be expressed analytically. Writing a general bandpass signal as $x_{RF}(t) = \mathrm{Re}\{x_{BB}(t)\exp(+j\omega_{RF}t)\}$, where $x_{BB}(t)$ denotes the baseband signal, and multiplying it by an LO waveform

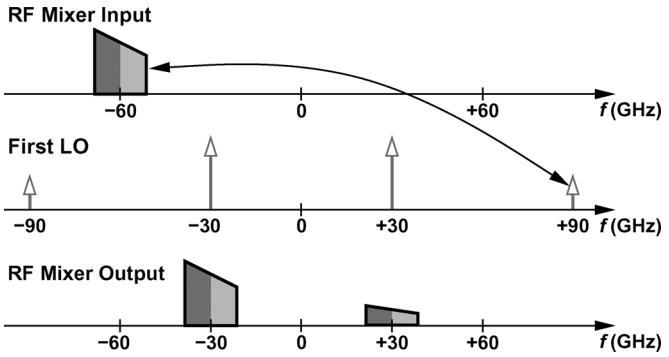


Fig. 5. Elimination of the positive frequency at RF.

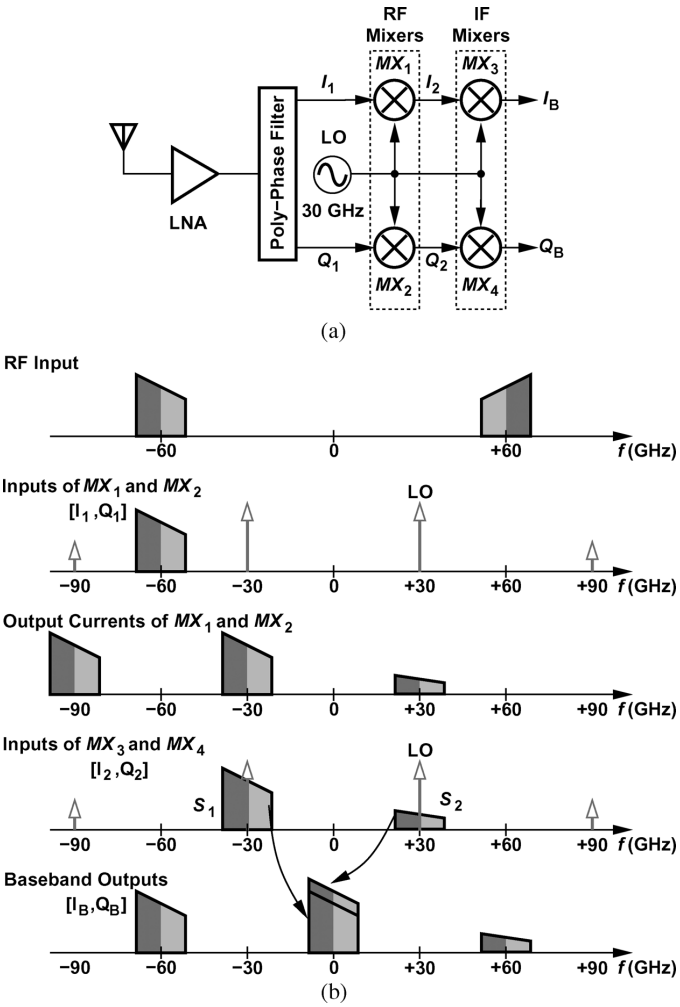


Fig. 6. (a) Proposed half-RF receiver architecture and (b) its spectra.

approximated by $\cos\omega_{\rm LO}t + \alpha\cos 3\omega_{\rm LO}t$, we obtain the first IF signal as

$$x_{IF}(t) = \mathrm{Re}\left\{x_{BB}(t)e^{+j\omega_{IF}t}\right\} + \mathrm{Re}\left\{\alpha x^*_{BB}(t)e^{+j\omega_{IF}t}\right\}. \tag{1}$$

The second term reveals that the mirrored replica is, in fact, the complex conjugate of the signal scaled by a factor of α. For

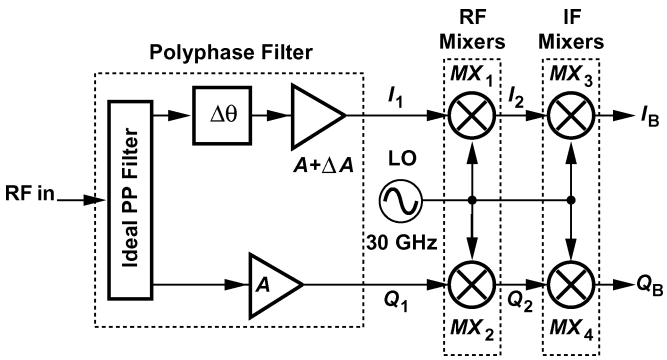


Fig. 7. Gain and phase mismatch in the receiver.

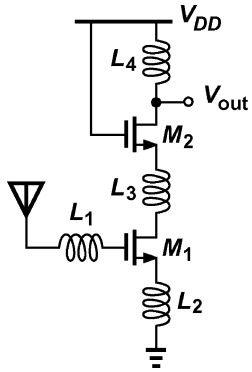


Fig. 8. LNA topology.

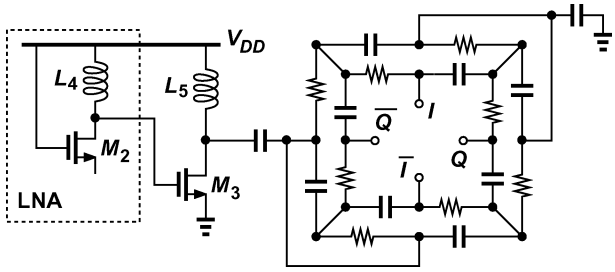


Fig. 9. Schematic of LNA and polyphase filter.

hard-switching mixers, $\alpha \approx 1/3$.[1] The downconversion of the IF signal to baseband yields

$$\begin{aligned} x_{BB,I}(t) &= \mathrm{Re}\left\{x_{BB}(t) + \alpha x^*_{BB}(t)\right\} \\ &= (1+\alpha)\mathrm{Re}\left\{x_{BB}(t)\right\} \end{aligned} \tag{2}$$

$$\begin{aligned} x_{BB,Q}(t) &= \mathrm{Im}\left\{x_{BB}(t) + \alpha x^*_{BB}(t)\right\} \\ &= (1-\alpha)\mathrm{Im}\left\{x_{BB}(t)\right\}. \end{aligned} \tag{3}$$

As an example, Fig. 4 shows the constellation of a 16-QAM signal downconverted by such a receiver (an SNR of 25 dB is assumed). As predicted by (2) and (3), the constellation is expanded in the I direction and compressed in the Q direction. The factors $1+\alpha$ and $1-\alpha$ can be viewed as an I/Q gain mismatch of $(1+\alpha)/(1-\alpha) = 2$. This 6-dB mismatch proves difficult to correct in the analog domain (due to nonlinearity

[1]It is important to note that $3f_{\rm LO}$ does not appear as a voltage quantity anywhere in the circuit and is therefore not suppressed. With the LO amplitude and switching pair design used here, simulations indicate an α of 0.22.

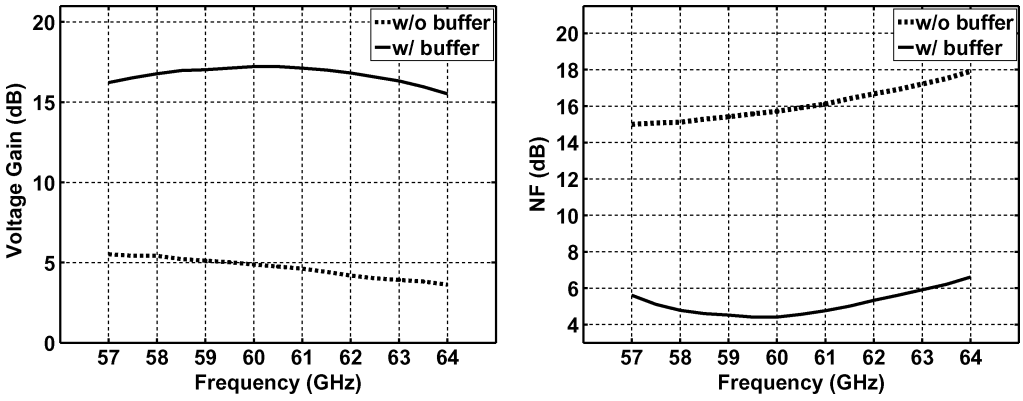


Fig. 10. Simulated (a) gain and (b) noise figure of the LNA/PPF/mixer cascade.

and noise issues) or in the digital domain (due to the additional dynamic range required of the baseband analog-to-digital converters). Similar observations apply to the transmit path as well.

Another drawback of the half-RF receiver shown in Fig. 2(a) stems from the inevitable result that the first IF is equal to $f_{\rm LO}$. Thus, the LO-IF feedthrough of the RF mixer cannot be filtered, potentially desensitizing the IF mixers. This issue makes it difficult to utilize a single-balanced RF mixer, which is the preferred choice if the LNA is single-ended.

III. Receiver Design

A. Proposed Architecture

In order to avoid the mirrored replica in Fig. 2(b), one can eliminate the third harmonic of the LO by linearizing the corresponding port of the mixer, but at the cost of drastic degradation of the conversion gain and the noise figure. Alternatively, as depicted in Fig. 5, one can eliminate the positive or negative part of the RF signal spectrum. Here, the mixing of the RF signal with $3f_{\rm LO}$ does produce a 30-GHz replica at IF, but the replica is not mirrored with respect to the desired IF signal.

Fig. 6(a) shows the proposed half-RF receiver architecture, which employs this concept. The input is applied to an LNA and subsequently a polyphase filter (PPF) so as to create a complex signal having negative (or positive) frequency content. The one-sided spectrum is then downconverted twice using mixers that are driven by a real (rather than quadrature) 30-GHz LO.

Fig. 6(b) illustrates the signal spectra at different points along the receiver. The one-sided spectrum at the inputs of MX_1 and MX_2 is mixed with $f_{\rm LO}$ and $3f_{\rm LO}$, generating replicas at -30 GHz, -90 GHz, and $+30$ GHz in the output currents of the two mixers. The bandpass loads of MX_1 and MX_2 suppress the -90-GHz component, applying only S_1 and S_2 to the IF mixers. Upon downconversion to baseband, S_2 constructively adds to S_1.

The behavior of the architecture can also be formulated by assuming an RF signal with an envelope $A(t)$ and a phase $\phi(t)$. The quadrature outputs of the polyphase filter in Fig. 6(a) are therefore given by

$$I_1 = A(t)\cos\left[\omega_{RF}t + \phi(t)\right] \tag{4}$$

$$Q_1 = A(t)\sin\left[\omega_{RF}t + \phi(t)\right]. \tag{5}$$

Multiplying these signals by an LO waveform expressed as $\cos\omega_{\rm LO}t + \alpha\cos 3\omega_{\rm LO}t$ and neglecting the high-frequency terms, we have

$$I_2 = A(t)\cos\left[\omega_{IF}t + \phi(t)\right] + \alpha A(t)\cos\left[\omega_{IF}t - \phi(t)\right] \tag{6}$$

$$Q_2 = A(t)\sin\left[\omega_{IF}t + \phi(t)\right] - \alpha A(t)\sin\left[\omega_{IF}t - \phi(t)\right]. \tag{7}$$

Upon mixing with the LO, I_2 and Q_2 result in the following baseband signals:

$$I_B = (1+\alpha)A(t)\cos\left[\phi(t)\right] \tag{8}$$

$$Q_B = (1+\alpha)A(t)\sin\left[\phi(t)\right]. \tag{9}$$

Simulation of the receiver with a 16-QAM RF input confirms that the signal constellation is restored.

Effect of Mismatches: The one-sided spectrum assumed for the RF signal in the above analysis occurs only in the absence of mismatches. To determine the efficacy of the architecture with a realistic implementation, we lump all of the mismatches as a gain imbalance ΔA and a phase imbalance $\Delta\theta$ in the polyphase filter (Fig. 7). This is justified in Appendix A. Repeating the above analysis yields the complex baseband signal as

$$I_B + jQ_B = (1+\alpha)A\left\{\left[\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}+1\right]x_{BB}(t) + \left[\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}-1\right]x_{BB}^*(t)\right\}. \tag{10}$$

The ratio of the mirrored replica to the desired signal is thus given by

$$\left|\frac{x_{BB}^*}{x_{BB}}\right| = \left|\frac{\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}-1}{\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}+1}\right| \tag{11}$$

which is identical to the image-rejection ratio (IRR) of image-reject receivers [9]. In other words, the proposed architecture attenuates the mirrored replica by a factor equal to IRR.

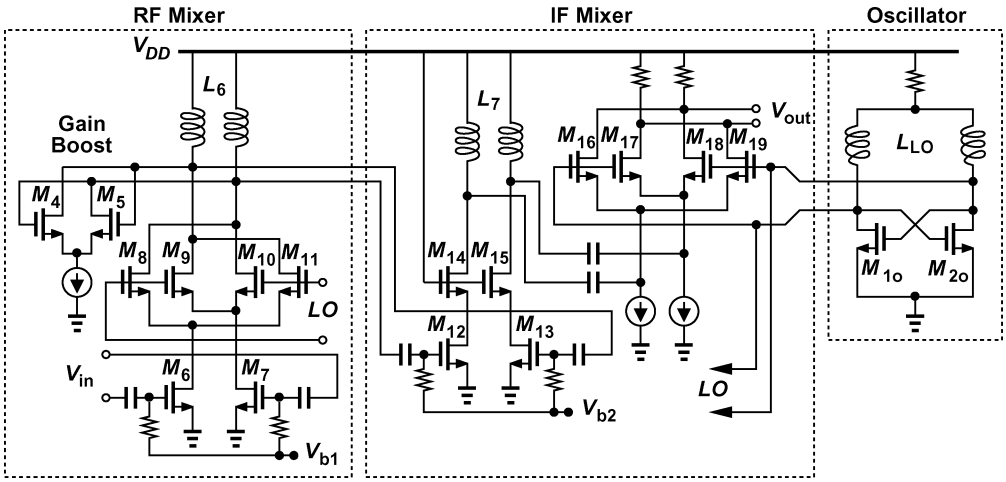


Fig. 11. RF and IF mixers and the oscillator.

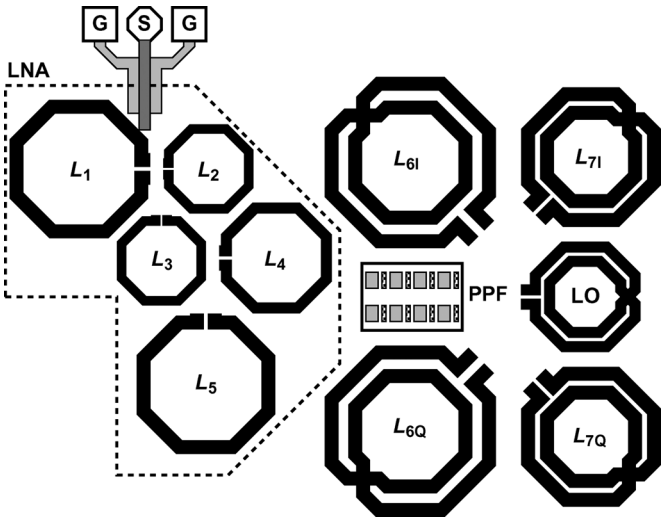


Fig. 12. Receiver floor plan.

TABLE I
DEVICE PARAMETERS IN THE RECEIVER BLOCKS

		$W(\mu\text{m})$	I_D (mA)
LNA	$M_{1,2}$	20	3
	M_3	7	4.5
RF Mixer	$M_{4,5}$	1.2	0.05
	$M_{6,7}$	3	0.6
	$M_{8\text{-}11}$	6	0.3
IF Mixer	$M_{12\text{-}15}$	45	3
	$M_{16\text{-}19}$	6	0.25
Oscillator	$M_{1o,2o}$	5	1.65

Transceivers operating at 60 GHz are likely to employ I/Q calibration if they must accommodate dense modulation schemes such as 16-QAM [10]. Fortunately, such calibration also lowers the mirrored replica proportionally. This can be proved by writing the baseband signals as

$$I_B = (1+\alpha)(A+\Delta A)e^{j\Delta\theta}(x_{BB}+x_{BB}^*) \quad (12)$$

$$Q_B = -j(1+\alpha)A(x_{BB}-x_{BB}^*) \quad (13)$$

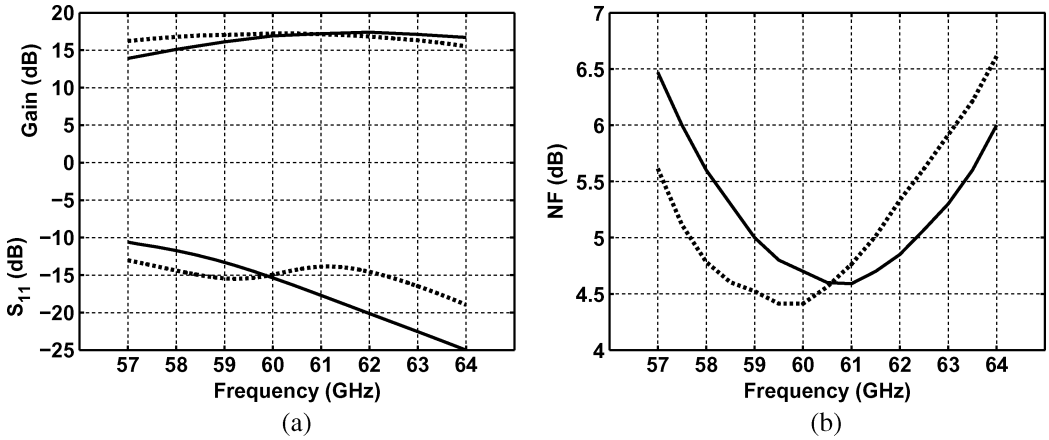
and noting that, to compensate for the gain and phase error of the desired signal (x_{BB}), a gain correction of $A/(A+\Delta A)$ and a phase correction of $\exp(-j\Delta\theta)$ are required. This gain and phase adjustment would also drive the coefficient of $x_{BB}^*(t)$ in (10) to zero, consequently suppressing the mirrored replica.

B. Building Blocks

The low-noise amplifier is realized as a cascode topology with inductive degeneration (Fig. 8). Since the pole at the cascode node falls around $f_T/2$, inductor L_3 is inserted to create series peaking [11]. In contrast to placing an inductor in parallel with this node [3], series peaking avoids the use of a large, high-quality bypass capacitor and obviates the need for a low-inductance ground connection to that capacitor. Also, series peaking provides a greater bandwidth. Nevertheless, L_3 along with the gate-drain overlap capacitance of M_1 tends to lower the real part of the input impedance. These effects are formulated in Appendix B.

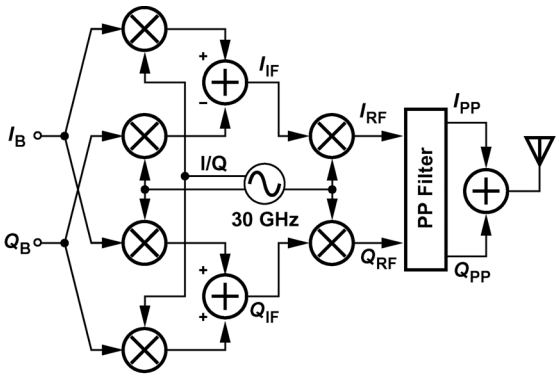
The quadrature separation following the LNA can be realized in different forms, each introducing its own trad-offs. For example, the microwave hybrid structure in [12] occupies a large area and fails to produce differential outputs from a single-ended input. The current-domain technique in [3] requires small component values at 60 GHz and also fails to perform single-ended to differential conversion. Thus, an *RC* polyphase filter is chosen.

To accommodate a wide bandwidth, this design employs a two-stage polyphase filter (Fig. 9). The unit resistor and capacitor are respectively equal to 120 Ω and 20 fF in the first stage and 130 Ω and 20 fF in the second. In addition to quadrature separation, the PPF also provides differential outputs, thereby allowing the use of a double-balanced RF mixer. This property proves critical in reducing the LO-to-RF feedthrough, which would otherwise desensitize the IF mixers considerably. Even



(a) (b)

Fig. 13. Simulation of the gain, S_{11} and NF of the LNA/PPF/mixer cascade with coupling (solid lines) and without (dashed lines).



(a)

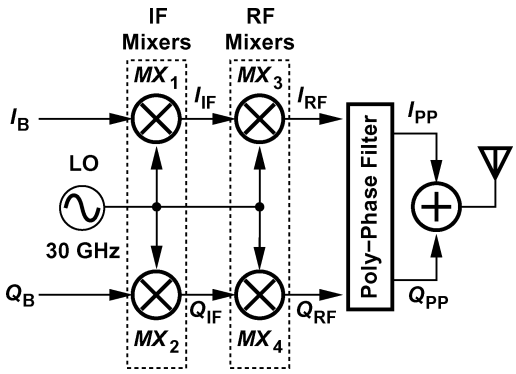
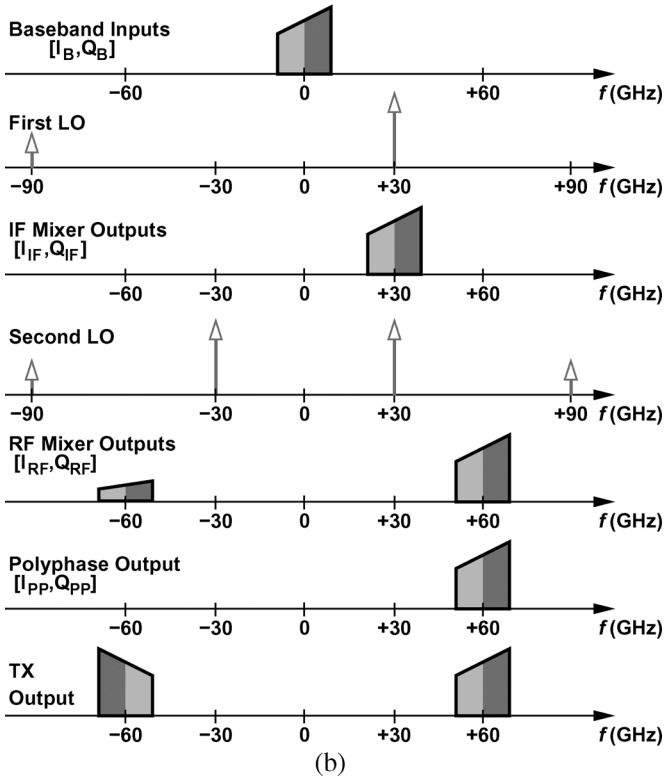


Fig. 15. Architecture of the proposed transmitter.



(b)

Fig. 14. (a) Transmitter with complex signals. (b) TX spectra.

with two stages, the polyphase filter may not provide sufficient balance between I and Q outputs near the edges of the band. Nonetheless, as explained in Section III-A, per-channel I/Q calibration can alleviate this issue. At midband, the filter exhibits an input impedance of 140 Ω, a loss of 11 dB, and an input-referred noise voltage of 1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, drastically degrading the performance of the LNA/mixer cascade. For this reason, a buffer stage consisting of M_3 and L_5 is interposed between the LNA and the PPF. Figs. 10(a) and 10(b) plot the simulated gain and noise figure of the LNA/PPF/mixer cascade with and without the buffer as a function of frequency, respectively. The 1-dB compression point falls from −10.5 dBm to −22.3 dBm with the addition of the buffer. Transistor M_3 in Fig. 9 benefits from a large overdrive voltage while suffering from a poorly-defined bias current. Simulations indicate that the drain current varies from 3.7 mA in the slow corner to 5.3 mA in the fast corner. Alternatively, a current source can be inserted in series with the source of M_3 and bypassed to ground (or V_{DD}) by a capacitor [13], but it is difficult to provide a low-impedance return path for the capacitor at these frequencies.

The RF and IF mixer circuits are shown in Fig. 11. The gain of the RF mixer is raised by 3 dB by the cross-coupled pair tied to its output nodes without risking instability. According to simulations, this pair contributes negligible noise but it lowers the 1-dB compression point by 3 dB. The IF mixer incorporates capacitive coupling between its input transconductance stage and its mixing quad, thus allowing a high current (2 mA) in the former to achieve high linearity and low noise, and a low current (0.4 mA) in the latter to ensure abrupt switching and

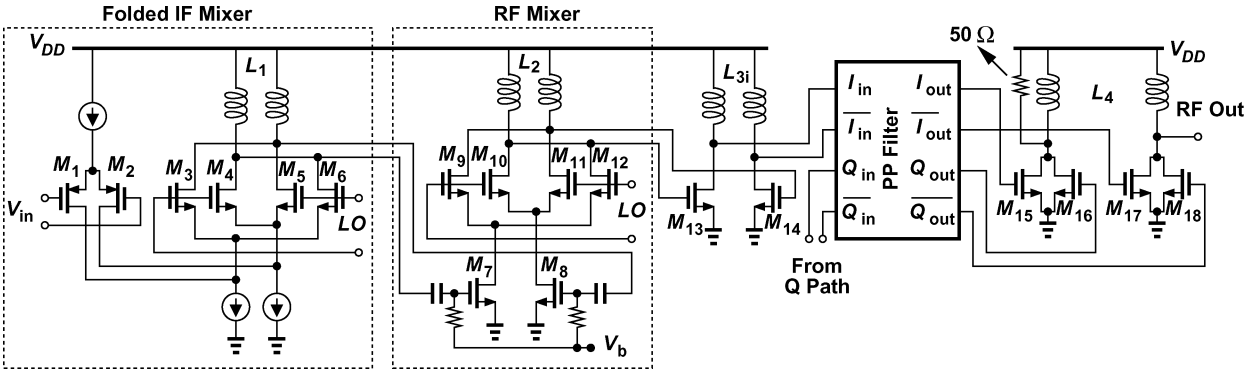


Fig. 16. Schematic of the proposed transmitter.

accommodate larger load resistors and hence a higher conversion gain. With L_6 and L_7 connected to the input and output of the transconductance stage, respectively, the circuit can potentially become unstable. The parallel resistance introduced by the switching quad lowers the Q of L_7; nonetheless, the cascode devices are added to guarantee stability and reduce the LO leakage, which would otherwise result in a large DC offset in the baseband. Table I summarizes the device parameters in various blocks of the receiver.

C. Floor Plan

The ten inductors used in the LNA, the RF and IF mixers, and the LO dictate the structure of the receiver floor plan. As shown in Fig. 12, the five inductors in the LNA are placed in close proximity to minimize the length of the 60-GHz lines. The circuit still contains one long 60-GHz interconnect (85 μm) between the top of L_5 and the polyphase filter. The LO is placed farthest from the LNA input so that its leakage does not desensitize the receiver. In this design, $L_1 = L_5 = 197$ pH, $L_2 = L_3 = 100$ pH, $L_4 = 173$ pH, $L_6 = 700$ pH and $L_7 = 560$ pH.

The proximity of $L_1 - L_5$ raises concern with respect to couplings among them. In order to rigorously account for these couplings, the layout of $L_1 - L_5$ is imported to Ansoft HFSS, simulated as a 10-port network, and returned to circuit simulations as an S-parameter model. The overall LNA/PPF/mixer cascade is then simulated to obtain various characteristics. Fig. 13 plots the simulated input return loss, voltage gain, and NF as a function of frequency with couplings and without couplings (obtained from circuit simulations with isolated inductor models).

The LO is realized as a standard negative-G_m *LC* topology with a bias current of 4 mA, providing a peak differential voltage of around 700 mV to the mixers. To avoid additional inductors, no buffer is placed between the LO and the mixers.

TABLE II
DEVICE PARAMETERS IN THE TRANSMITTER BLOCKS

		$W(\mu\text{m})$	I_D(mA)
IF Mixer	$M_{1,2}$	100 ($L = 0.5$ μm)	2
	$M_{3\text{-}6}$	6	0.25
RF Mixer	$M_{7,8}$	30	0.5
	$M_{9\text{-}12}$	10	0.25
	$M_{13,14}$	8	3.5
Output Driver	$M_{15\text{-}18}$	20	7.5
Oscillator	$M_{1o,2o}$	5	1.5

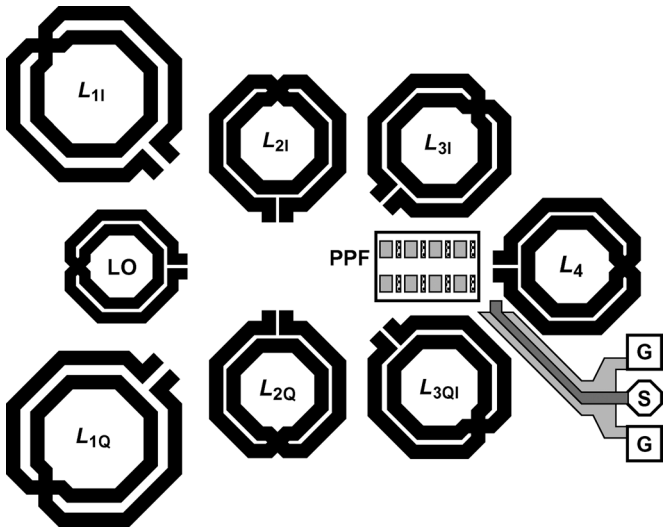
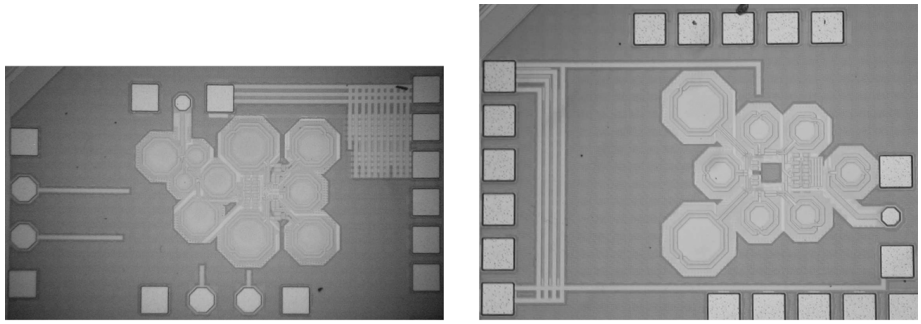


Fig. 17. Transmitter floor plan.

IV. TRANSMITTER

A. Proposed Architecture

As mentioned in Section III, most of the issues identified in various receiver architectures apply to transmitters as well. Also, two-step upconversion with a 30-GHz LO suffers from a mirrored replica resulting from $3f_{\text{LO}}$. As with the receiver, this effect can be suppressed if the signal is processed in complex form. Shown in Fig. 14(a) is an example, where the baseband I and Q signals are mixed with the quadrature phases of the LO so as to produce quadrature IF signals [14]. The IF components are then upconverted to 60 GHz and applied to a PPF, whose outputs are summed. The transmitter spectra are illustrated in Fig. 14(b), suggesting that the mixing of the one-sided IF signal with the second LO produces the desired channel at +60 GHz and the



(a) (b)

Fig. 18. Die photographs of the receiver and the transmitter.

mirrored replica at −60 GHz. The PPF removes the latter, and the summation of its outputs yields a real TX signal.

The presence of a polyphase filter in the upconverted signal path suggests that perhaps the first upconversion need not use the quadrature phases of the LO. Indeed, since the baseband signal is available in complex form, it can simply be mixed with a real LO so as to generate complex IF components. The architecture is thus simplified to that shown in Fig. 15, where a differential LO drives all four mixers. Simulations with a 16-QAM signal confirm that this architecture suppresses the mirrored replica.

The duality between the receiver architecture of Fig. 6(a) and the transmitter architecture of Fig. 15 implies that mismatches have similar effects in both. Specifically, 1) mismatches can be lumped in the polyphase filter, and 2) I/Q calibration also attenuates the mirrored replica proportionally.

B. Building Blocks

Fig. 16 shows the realization of the transmit path. Unlike the RF mixer, the IF mixer employs a folded input so as to allow DC coupling of the baseband signal while maintaining a well-defined bias current. Common-source buffers are inserted between the RF mixers and the polyphase filter, which consist of two stages similar to those in the receiver. The output stage sums the PPF outputs in the current domain and directly drives 50-Ω instrumentation in single-ended form. Though not included here, a balun can raise the output power and, more importantly, suppress the 60-GHz carrier feedthrough. Table II summarizes the device parameters in various blocks of the transmitter.

C. Floor Plan

The symmetry of the architecture and the circuits in Fig. 16 leads to the symmetric floor plan shown in Fig. 17. The eight differential inductors are positioned so as to favor the 60-GHz sections of the design and the 30-GHz LO. The load inductors of the IF mixers ($L_{1\mathrm{I}}$ and $L_{1\mathrm{Q}}$) therefore connect to the core through relatively long interconnects (80 μm). In this design, $L_1 = 720$ pH and $L_2 = L_3 = L_4 = 310$ pH. The LO design is the same as that in the RX.

V. Experimental Results

The receiver and the transmitter are fabricated in 90-nm CMOS technology, each employing its own LO. Due to loading and routing difficulties, it appears necessary that millimeter-wave RX and TX paths use dedicated LOs and synthesizers rather than share them. Fig. 18 shows the die photographs. The active areas are 500 μm × 370 μm and 495 μm × 425 μm for the RX and TX, respectively. The 60-GHz input and output lines are realized as microstrips that connect to a ground-signal-ground pad arrangement for

TABLE III
Comparison of Different Receivers

	[2]	[3]	[15]	This Work
Frequency Range (GHz)	57-63	49-53	57-63	57-61
Noise Figure (dB)	10.4-11	6.9-8.3	6.1-6.35	5.7-7.1
Gain (dB)	9.5-12	26-31.5	−8.5-55	19.8-22
P_{1dB} (dBm)	−15.8	−25.5	−26	−27.5
LO Leakage to Input (dBm)	N/A	−47	< -77	−65
I/Q Mismatch	N/A	6.5°/1.5dB	N/A	2.1°/1.1dB
LO Phase Noise (dBc/Hz @ 1-MHz offset)	−86	−95	off-chip	−90
Power Dissipation (mW)	77	80	24	36
LNA				9
Mixers				23
Oscillator				4
Supply Voltage (V)	1.2	1.8	1.0	1.2
Chip Area (mm^2)	3.8	0.15	1.55	0.19
CMOS Technology	0.13-μm	90-nm	90-nm	90-nm

TABLE IV
Comparison of Different Transmitters

	[12]	[16]	This Work
Frequency Range (GHz)	57-67	60-64	59-63
Max Output Power (dBm)	−3	11	−7.2
Output P_{1dB} (dBm)	N/A	10	−8.6
I/Q Mismatch (dB)	N/A	N/A	−20
LO Phase Noise (dBc/Hz @ 1-MHz offset)	off-chip	off-chip	−90
Power Consumption (mW)	98	133*	78*
Supply Voltage (V)	1.2	0.7	1.5
Chip Area (mm^2)	1.15	1.0	0.2
CMOS Technology	0.13-μm	90-nm	90-nm

* Excludes the power amplifier.

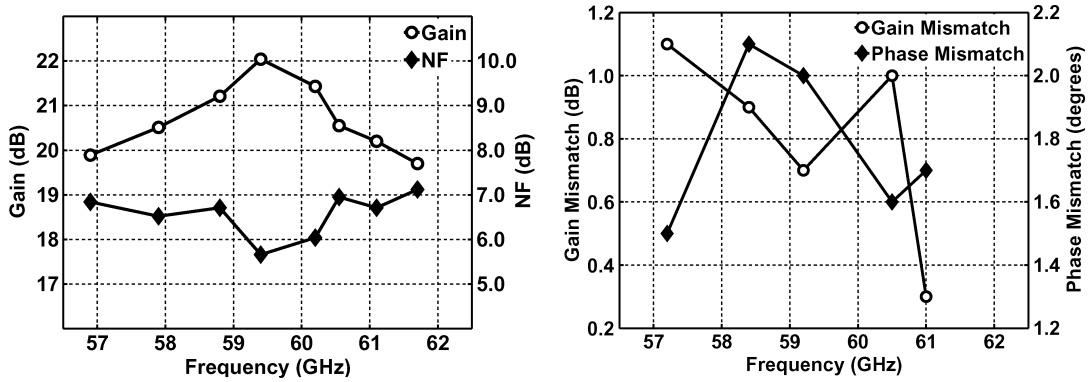


Fig. 19. Measured (a) gain and noise figure, and (b) gain/phase mismatch of the receiver.

probing. The low-frequency pads are bonded to a printed circuit board on which each die is mounted. The LO frequency is varied by lowering a narrow metal plate on top of the LO inductor and adjusting its distance from the chip [3].

Fig. 19 plots the measured receiver gain, noise figure, and baseband I/Q mismatches as a function of frequency. The gain varies from 19.8 dB to 22 dB and the noise figure from 5.7 dB to 7.1 dB. The gain and phase mismatches reach a maximum of 1.1 dB and 2.1°, respectively.[2] Such values translate to an uncalibrated rejection of 22 dB for the mirrored replica. Fig. 20 shows the measured compression behavior of the receiver, indicating a 1-dB compression point of −27.5 dBm. The measured DC offset at the output of the receiver varies between 10.1–15.3 mV.

In order to characterize the transmitter's suppression of the mirrored replica, an asymmetrically-modulated signal is emulated by two complex tones of different frequencies in the baseband [Fig. 21(a)]. As a result, the IF spectrum exhibits asymmetry with respect to the carrier frequency of 30 GHz, leading to a finite mirrored replica at 60 GHz. The relative levels at the output readily yield the amount of suppression. Fig. 21(b) shows the measured output in this case. Here, f_c denotes the 60-GHz carrier feedthrough,[3] f_1 and f_2 the original tones, and f_3 and f_4 the mirrored replicas. We observe an uncalibrated suppression of approximately 20 dB.

Figs. 22(a) and (b) plot the measured output power and sideband rejection (mirrored replica suppression) of the transmitter as a function of frequency. Fig. 23 shows the LO spectrum as measured at the baseband ports of the TX. The phase noise is about −90 dBc/Hz at 1-MHz offset.[4] Tables III and IV compare the performance of the proposed RX and TX designs with that of other reported work.

VI. Conclusion

The half-RF architecture can considerably relax the LO-related issues and yield a compact, low-power design. The effect of the LO's third harmonic can be suppressed by the proposed architecture. It is envisioned that baseband I/Q calibration can deal with the limited bandwidth of the polyphase filter, allowing coverage of the entire unlicensed band around 60 GHz.

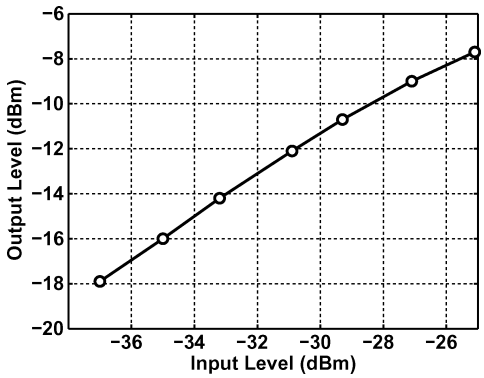


Fig. 20. Measured compression behavior of the receiver.

Appendix A

Consider the mixer blocks of the receiver in Fig. 24 where the gain and phase mismatch of the RF and IF mixers are inserted. Assuming the first and third harmonic for the LO and perfect quadrature separation in the polyphase filter, we can derive the output expression for a generic RF input signal $x_i + jx_q = x_{BB}\exp(+j\omega_{RF}t)$ as

$$I_B = (1+\alpha)(G_0+\Delta G_0)(G_1+\Delta G_1)e^{j(\Delta\phi_0+\Delta\phi_1)} \times (x_{BB}+x_{BB}^*) \quad (14)$$

$$Q_B = (1+\alpha)G_0G_1\,(x_{BB}-x_{BB}^*)\,, \quad (15)$$

where α is the relative amplitude of the third harmonic of the LO. For small gain and phase errors, (14) and (15) can be written as

$$I_B = (1+\alpha)(G+\Delta G)e^{j(\Delta\phi_0+\Delta\phi_1)}\,(x_{BB}+x_{BB}^*) \quad (16)$$

$$Q_B = (1+\alpha)G\,(x_{BB}-x_{BB}^*) \quad (17)$$

where $G = G_0G_1$ and $\Delta G = G_0\Delta G_1 + G_1\Delta G_0$. Comparing (16) and (17) with (10), we conclude that the gain and phase mismatch of the RF and IF mixers can be lumped along with

[2]The sharp changes across the frequency band are attributed to measurement inaccuracies rather than the response of the circuit.

[3]The feedthrough is relatively large because a 30-GHz LO driving a double-balanced mixer produces a significant 60-GHz component in each single-ended output. A balun can reduce this considerably.

[4]The LO at the TX output is attenuated even more, failing to display the phase noise.

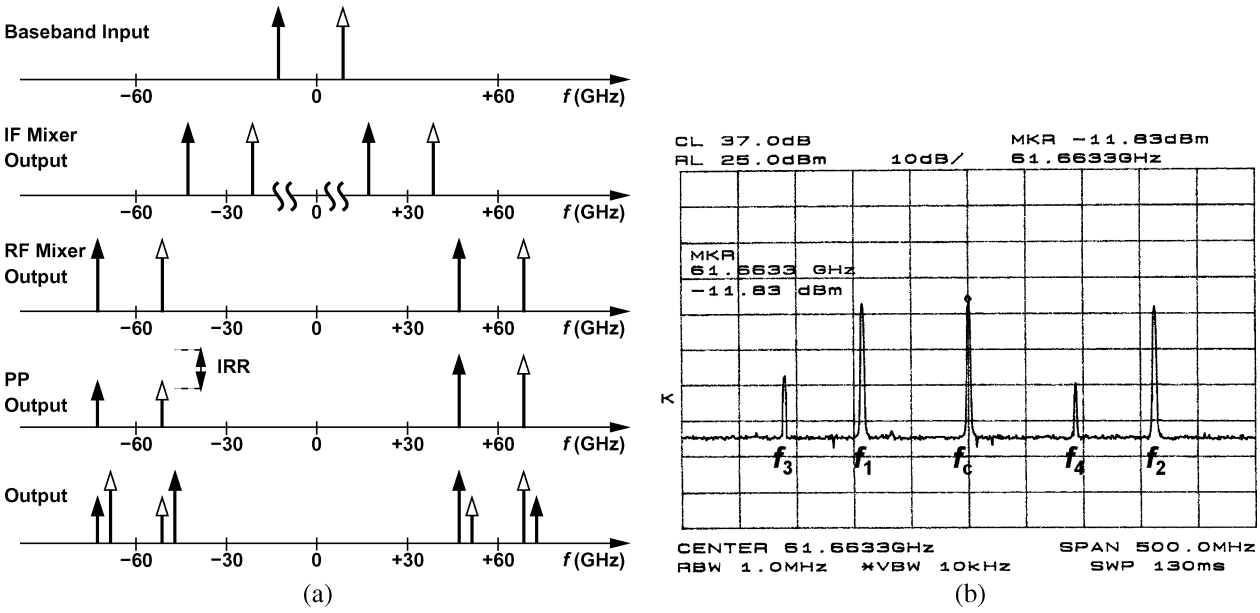


Fig. 21. (a) Asymmetric modulation emulated by two complex tones, (b) measured TX output.

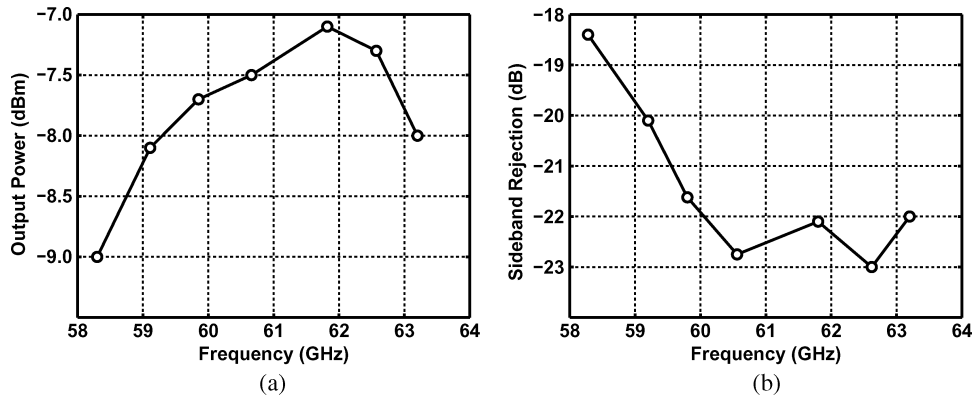


Fig. 22. Measured (a) output level and (b) sideband rejection of the transmitter.

the mismatches of the polyphase filter even in the presence of the LO's third harmonic.

APPENDIX B

Consider the LNA of Fig. 25, where the gate-source and gate-drain capacitances of transistor M_1 are included. The input impedance of this structure can be written as shown in (18) at the bottom of the page. The numerator of $\mathrm{Re}(Z_{in})$ assumes the form of $A + B\omega^2 + C\omega^4$, with the coefficients given by

$$A = g_{m1}\left(\frac{C_{gd}}{g_{m1}g_{m2}} + \frac{C_{gd}}{g_{m2}^2} + \frac{C_{gs}}{C_{gd}}L_2 + \frac{g_{m1}}{g_{m2}}L_2 - L_3\right) \quad (19)$$

$$B = g_{m1}L_3(L_3C_{gd} - L_2C_{gs}) + \frac{C_{gd}L_2}{g_{m2}}\left(g_{m1}^2L_2 - 2C_{gs}\right) \quad (20)$$

$$C = \frac{C_{gs}^2C_{gd}L_2^2}{g_{m2}}. \quad (21)$$

It is seen from these equations that some values of L_3 can potentially make $\mathrm{Re}(Z_{in})$ negative. For the special case of $L_2 = 0$, $\mathrm{Re}(Z_{in})$ reduces to a quadratic and remains positive if

$$L_3 < \frac{C_{gd}}{g_{m2}}\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right). \quad (22)$$

$$Z_{in}(s) = L_1 s + \frac{1}{C_{gd}s}\frac{\left(1 + \frac{C_{gd}}{g_{m2}}s + L_3C_{gd}s^2\right)\left(1 + g_{m1}L_2s + L_2C_{gs}s^2\right)}{\left(1 + \frac{C_{gs}}{C_{gd}} + \frac{g_{m1}}{g_{m2}}\right) + \left[g_{m1}(L_2 + L_3) + \frac{C_{gs}}{g_{m2}}\right]s + C_{gs}(L_2 + L_3)s^2}. \quad (18)$$

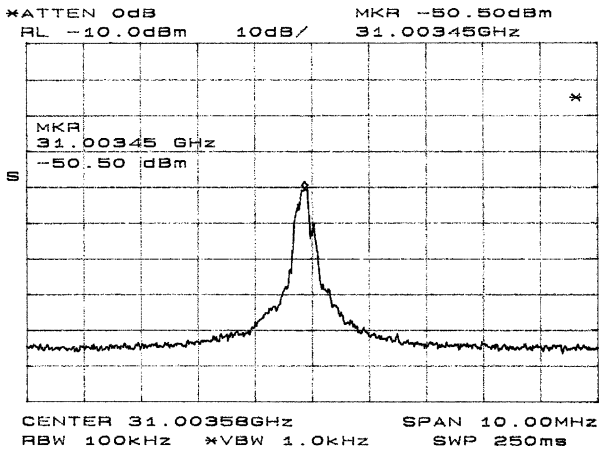


Fig. 23. Measured LO spectrum at TX baseband input.

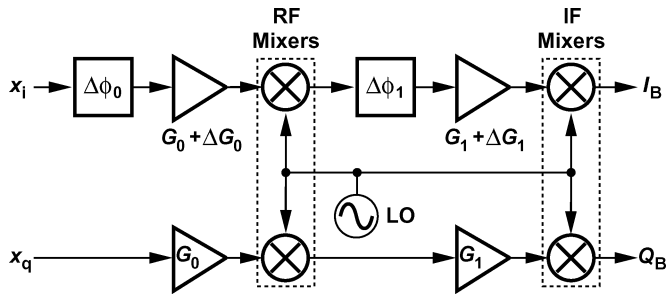


Fig. 24. I/Q mismatch in the receiver.

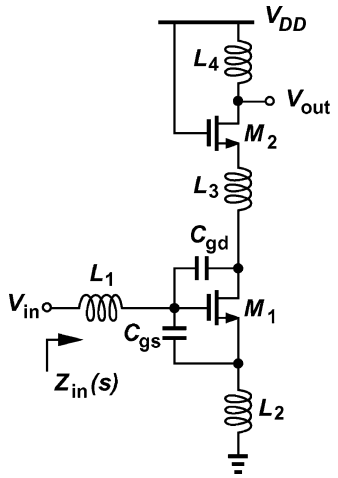


Fig. 25. Input impedance of the LNA.

With $L_2 \neq 0$, we assume that $g_{m1} = g_{m2} = g_m$, $L_2 \approx L_3 = L$, $C_{gs} \gg C_{gd}$, and $g_m L/C_{gs}$ is on the order of $1/g_m$. It follows that

$$A \approx g_m \frac{C_{gs}}{C_{gd}} L \tag{23}$$

$$B \approx -g_m L^2 C_{gs} \tag{24}$$

$$C = \frac{C_{gs}^2 C_{gd} L^2}{g_m}. \tag{25}$$

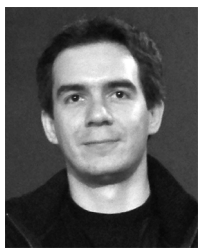
For $A+B\omega^2+C\omega^4$ to remain positive at all frequencies, $4AC > B^2$, and hence

$$L < 4\frac{C_{gs}}{g_m^2}. \tag{26}$$

With the values used in this design, this upper limit is about 280 pH. Chosen for $\mathrm{Re}(Z_{in}) = 50\,\Omega$, the value of $L_2 = 100$ pH ensures a high margin to instability.

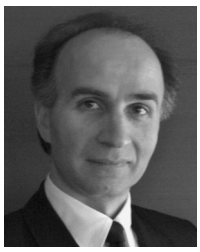
REFERENCES

[1] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.
[2] S. Emami *et al.*, "A highly integrated 60 GHz CMOS front-end receiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 190–191.
[3] B. Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 477–485, Feb. 2008.
[4] A. Parsa and B. Razavi, "A 60 GHz CMOS receiver using a 30 GHz LO," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 190–191.
[5] K. Scheir *et al.*, "Design and analysis of inductors for 60 GHz applications in a digital CMOS technology," presented at the 69th ARFTG Microwave Measurement Conf., Honolulu, HI, Jun. 2007.
[6] T. O. Dickson *et al.*, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
[7] S. K. Reynolds *et al.*, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.
[8] B. Razavi, "A 5.2-GHz CMOS receiver with 62-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 810–815, May 2001.
[9] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
[10] I. Vassiliou, "A single-chip digitally calibrated 5.15-5.825-GHz 0.18-μm CMOS transceiver for 802.11a wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2221–2231, Dec. 2003.
[11] T. Yao *et al.*, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.
[12] C.-H. Wang *et al.*, "A 60 GHz low-power six-port transceiver for gigabit software-defined transceiver applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 192–596.
[13] B. Razavi, "Architectures and circuits for RF CMOS receivers," in *Proc. IEEE Custom Integrated Circuits Conf.*, Santa Clara, CA, May 1998, pp. 393–400.
[14] B. Razavi, "A 900-MHz/1.8-GHz CMOS transmitter for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 573–579, May 1999.
[15] B. Afshar, Y. Wang, and A. M. Niknejad, "A Robust 24 mW 60 GHz receiver in 90 nm standard CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 182–183.
[16] M. Tanomura *et al.*, "TX and RX front-ends for the 60 GHz band in 90 nm standard bulk CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 558–559.



Ali Parsa (S'03–M'08) received the B.S. and M.S. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively. In 1998, he joined Unistar-Micro Technology where he was involved in research and design of high-speed analog ICs for wireless communications both in Bipolar and CMOS technologies. In 2008, he received the Ph.D. degree in electrical engineering from the University of California, Los Angeles.

He is currently a Senior Staff Scientist at Broadcom Corporation, San Diego, CA. His major research interests are design of high-speed integrated circuits for wireless communications.



Behzad Razavi (F'03) received the B.S.E.E. degree from Sharif University of Technology, Tehran, Iran, in 1985, and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of electrical engineering at University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. He was an Adjunct Professor at Princeton University from 1992 to 1994, and at Stanford University in 1995. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998, translated into Korean, Japanese, and Chinese), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001, translated into Chinese and Japanese), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003), and *Fundamentals of Microelectronics* (Wiley 2006), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996), and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003).

Prof. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the best paper award at the IEEE Custom Integrated Circuits Conference in 1998. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006 and the UCLA Faculty Senate Teaching Award in 1997. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He served on the Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and *International Journal of High Speed Electronics*. He is an IEEE Distinguished Lecturer.