Design Techniques for High-Speed, High-Resolution Comparators

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Abstract—**This paper describes precision techniques for the design of comparators used in high-performance analog-to-digital converters employing parallel conversion stages. Following a review of conventional offset cancellation techniques, circuit designs achieving 12-b resolution in both BiCMOS and CMOS 5-V technologies are presented. The BiCMOS comparator consists of a preamplifier followed by two regenerative stages and achieves an offset of 200 μV at a 10-MHz clock rate while dissipating 1.7 mW. In the CMOS comparator offset cancellation is used in both a single-stage preamplifier and a subsequent latch to achieve an offset of less than 300 μV at comparison rates as high as 10 MHz, with a power dissipation of 1.8 mW.**

I. Introduction

In high-speed analog-to-digital converters, comparator design has a crucial influence on the overall performance that can be achieved. Converter architectures that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraints on the delay, resolution, power dissipation, input voltage range, input impedance, and area of those circuits. Moreover, the relatively large device mismatch and limited voltage range that accompany the integration of comparator circuits in low-voltage scaled VLSI technologies severely compromise the precision that can be obtained.

This paper introduces a number of comparator design techniques for use in parallel A/D converters that are implemented in BiCMOS and CMOS VLSI technologies. The suggested methods are intended to provide improved resolution and speed while maintaining low power dissipation, a small input capacitance, and low complexity. The techniques are presented within the context of practical designs for both a BiCMOS and a CMOS comparator with 12-b resolution at 10-MHz comparison rates. The BiCMOS comparator employs a low-gain preamplifier followed by two regenerative amplifiers to achieve an offset of 200 μV at clock rates as high as 10 MHz. In the CMOS comparator, offset cancellation is used in both the preamplifier and the subsequent latch to achieve an offset of less than 300 μV at 10 MHz.

Manuscript received March 4, 1992; revised July 13, 1992. This work was supported by the Army Research Office under Contract DAAL03-91-G-0088.

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IEEE Log Number 9204135.

The next section of this paper reviews some of the conventional approaches to offset cancellation and identifies their fundamental trade-offs and limitations. The BiCMOS comparator is then described in Section III, and the design of the CMOS comparator is presented in Section IV. The experimental results obtained for both circuits are summarized in Section V.

II. Offset Cancellation Techniques

A. Circuit Topologies

The analog sampling capability inherent in CMOS and BiCMOS technologies provides a means whereby offsets can be periodically sensed, stored, and then subtracted from the input [1]. Of the various offset cancellation methods, two of the most common approaches, based on input offset storage (IOS) and output offset storage (OOS), are considered herein. Fig. 1(a) and (b) illustrates these two approaches as applied to a fully differential comparator. Each of these topologies comprises a preamplifier, offset storage capacitors, and a latch. With IOS, the cancellation is performed by closing a unity-gain loop around the preamplifier and storing the offset on the input coupling capacitors. With OOS, the offset is cancelled by shorting the preamplifier inputs and storing the amplified offset on the output coupling capacitors. A comparison of these two approaches reveals their respective merits and drawbacks.

In the comparator with IOS, the residual input-referred offset (i.e., the offset after calibration) is

$$V_{OS} = \frac{V_{OS1}}{1 + A_0} + \frac{\Delta Q}{C} + \frac{V_{OSL}}{A_0} \tag{1}$$

where V_{OS1} and A_0 are the input offset and gain of the preamplifier, respectively, ΔQ is the mismatch in charge injection from switches $S5$ and $S6$ onto capacitors $C1$ and $C2$, and V_{OSL} is the latch offset. In the comparator employing OOS, the residual offset is

$$V_{OS} = \frac{\Delta Q}{A_0 C} + \frac{V_{OSL}}{A_0}. \tag{2}$$

Equations (1) and (2) show that, for similar preamplifiers, the residual offset obtainable using OOS can be smaller than that for IOS. In fact, unless sufficient statistical data for V_{OS1}, ΔQ, and V_{OSL} are available, IOS requires the use of quite large values for A_0 and C to guarantee a low V_{OS}.

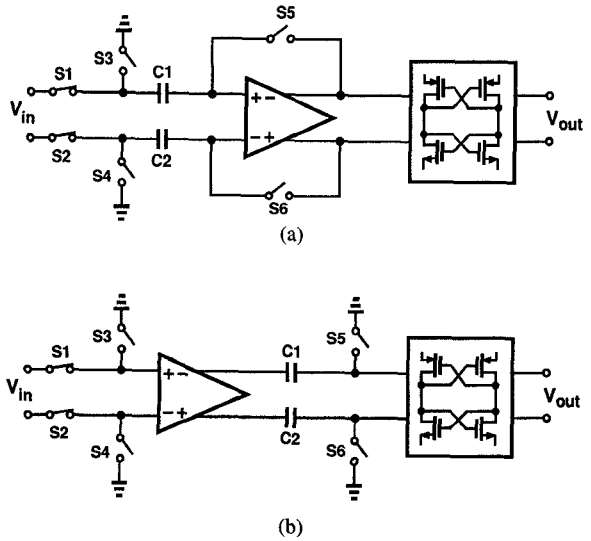

Fig. 1. Comparator offset cancellation techniques: (a) input offset storage, and (b) output offset storage.

Since the value of the input coupling capacitors with IOS is governed by charge injection, kT/C noise, and attenuation considerations, the input capacitance of this topology is usually higher than that of the OOS configuration. During offset cancellation, the input capacitance of the IOS circuit is equal to the offset storage capacitor, while in the comparison mode it is approximately the sum of the input capacitance of the preamplifier and the parasitic capacitances of the offset storage capacitor. These parasitic capacitances are typically as large as 0.1 to 0.2 pF for input storage capacitors in the range of 0.5 to 1 pF, whereas the preamplifier input capacitance can be maintained below 30 fF. For this reason OOS is generally preferable in flash stages, where many comparators are connected in parallel. Of course, the dc coupling at the input of an OOS comparator limits the common-mode range. Also, in applications where a large differential reference voltage must be stored in the comparator [2], the preamplifier of the OOS topology must be designed for a low gain so that it does not saturate at its output.

While IOS is accomplished by means of a closed feedback loop, which forces the preamplifier into its active region, OOS is normally an open-loop operation that requires tight control of the amplifier gain. Therefore, OOS is typically implemented using a single-stage amplifier with a gain of less than 10 to ensure operation in the active region under extreme variations in device matching and supply voltage.

In conventional CMOS comparator designs, the preamplifier is typically followed by a standard dynamic CMOS latch. As shown in the following subsection, this latch has a potentially large input offset and therefore requires the use of a high-gain preamplifier in order to achieve a low offset. Consequently, in high-resolution applications a single stage of OOS cannot be used, while a single-stage high-gain preamplifier with IOS suffers from a long delay.

The above considerations have led to the use of multistage calibration techniques in high-resolution applications. Fig. 2 illustrates a typical multistage comparator topology that, in effect, utilizes both IOS and OOS when it is clocked sequentially [2], [3]. The overall gain of the circuit is chosen so that an input of 0.5 LSB overcomes the offset of the latch (50 to 100 mV), and the number of stages is then selected to provide the smallest delay [2].

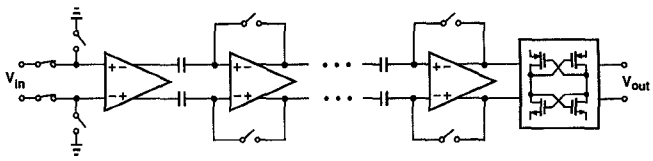

Fig. 2. Multistage offset cancellation.

In the configuration of Fig. 2 a large latch offset is accommodated through the use of multiple preamplifier stages, each with offset cancellation. Alternatively, the offset of the latch can be reduced so as to relax the gain required of the preamplifier. This can be accomplished through the use of either devices with inherently low offsets or offset cancellation in the latch.

B. Design Constraints in a Dynamic CMOS Latch

In order to synchronize the operation of a comparator with other parts of a system, as well as provide the gain needed to generate logic levels at the output, a regenerative amplifier is normally used as the final comparator stage. Fig. 3 shows a dynamic CMOS latch similar to that used in [4] to amplify small differences to CMOS levels. In this circuit, when Φ is low, $M5$ is off, $S1$ and $S2$ are on, and the latch senses the inputs V_{in1} and V_{in2}. When Φ goes high, $S1$ and $S2$ turn off to isolate nodes X and Y from input terminals and $M5$ turns on to initiate regeneration.

In order to simplify calculations and estimate a lower bound for the offset of the latch in Fig. 3, only the mismatches between $M1$ and $M2$ and between $S1$ and $S2$ are considered here. In practice, other errors such as mismatches between $M3$ and $M4$ further increase the offset. Considering only the $M1$, $M2$ and $S1$, $S2$ mismatches, the input offset of the latch can be expressed as

$$V_{OSM} = \Delta V_{TH} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)(V_{GS} - V_{TH}) + \frac{\Delta Q}{C_D} \tag{3}$$

where ΔV_{TH} and V_{TH} are the standard deviation and mean of the threshold voltage, $\Delta W/W$ and $\Delta L/L$ are relative dimension mismatches, $V_{GS} - V_{TH}$ represents the initial gate–source overdrive, ΔQ is the charge injection mismatch between $S1$ and $S2$, and C_D is the total capacitance at X or Y (assumed equal on both sides). For optimistic values of $\Delta V_{TH} = 5$ mV, $\Delta W/W = \Delta L/L = 0.05$, $V_{GS} - V_{TH} = 1$ V, $\Delta Q = 0.5$ fC, and $C_D = 100$ fF, the latch offset voltage is approximately 60 mV, with its major component arising from the second term in (3). This term can be reduced by increasing W and L and/or decreasing $V_{GS} - V_{TH}$, i.e., decreasing the initial drain current of $M1$ and $M2$. However, these remedies can degrade the speed

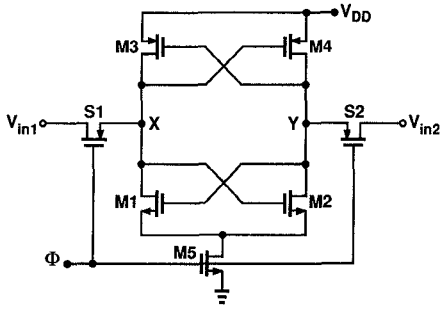

Fig. 3. Dynamic CMOS latch.

of the latch by increasing the regeneration time constant τ_R. Since

$$\tau_R = \frac{C_D}{g_m} \tag{4}$$

where g_m is the initial transconductance of $M1$ and $M2$, the delay–offset product of this latch assumes the following form:

$$\tau_R V_{OSM} = \Delta V_{TH} \frac{C_D}{g_m} + \frac{1}{2}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right) \cdot (V_{GS} - V_{TH}) \frac{C_D}{g_m} + \frac{\Delta Q}{g_m}. \tag{5}$$

This relationship reduces to a simpler form if C_D is assumed to only include the gate–source capacitance of $M1$ or $M2$, i.e., if $C_D = (2/3)WLC_{ox}$. Then, substituting for C_D and g_m gives

$$\tau_R V_{OSM} = \sqrt{\frac{WC_{ox}}{6\mu_n I_D}}\, L^{3/2}\Delta V_{TH} + \frac{1}{3}\left(\frac{\Delta W}{W} - \frac{\Delta L}{L}\right)\frac{L_2}{\mu_n} + \frac{\Delta Q}{g_m} \tag{6}$$

where I_D is the initial drain current of $M1$ and $M2$, which is determined by the dimensions of $M5$ and the high level of Φ. Note from (6) that although increasing L decreases $\Delta L/L$, its overall impact is to increase all of the three terms, thus raising the delay–offset product. Increasing W diminishes the last two terms but slowly raises the first term; since the second term contributes most, a W of 5 to 10 times minimum size should be used. From (6) it also follows that increasing I_D only slightly improves the trade-off. These observations indicate that, unless mismatch effects in a process are well characterized, a simple CMOS latch design will not reliably attain offsets less than several tens of millivolts.

In addition to a large input offset, the latch in Fig. 3 generates a great deal of kickback noise at its inputs when it is reset. This noise is largely differential because the two sides of the latch begin from different supply rails and swing in opposite directions toward their input common-mode voltage. As a result, the input levels are severely disturbed and may take a long time to recover if the preceding circuit does not have a low output impedance.

III. A Self-Calibrating BiCMOS Comparator

As discussed in Section II, the fundamental limitations of CMOS comparators stem from the large offset of their latch, and the consequent gain required of the preamplifier. The BiCMOS comparator described in this section employs a latch that consists of devices with inherently low offset to ease the performance required of the preamplifier. This is accomplished through the use of a bipolar latch interposed between a preamplifier and a CMOS output latch.

A. Architecture

Fig. 4 shows the architecture and timing of the BiCMOS comparator. The circuit comprises a preamplifier, offset storage capacitors, a bipolar latch, and a CMOS latch. Controlled by clocks Φ_1 and Φ_2, the circuit operates as follows. In the calibration mode, $S1$ and $S2$ are off, $S3$–$S6$ are on, and the inputs of the preamplifier and the bipolar latch are grounded. The preamplifier offset is thus amplified and stored on $C1$ and $C2$. In this mode, the two latches are also reset. In the comparison mode, first $S3$–$S6$ turn off while $S1$ and $S2$ turn on; the input voltage V_i is thereby sensed and amplified, generating a differential voltage at the bipolar latch input. Next, the two latches are strobed sequentially to produce CMOS levels at the output. The residual input-referred offset of this configuration is determined by the bipolar latch offset divided by the preamplifier gain. For an emitter-coupled bipolar latch, the latch offset voltage can be approximated as

$$V_{OSB} \approx \frac{kT}{q}\left(\frac{\Delta W}{W} + \frac{\Delta L}{L}\right) \tag{7}$$

where $\Delta W/W$ and $\Delta L/L$ represent relative dimension mismatches between the emitters of the two devices. Comparison of (3) and (7) indicates that, assuming equal dimension mismatches for bipolar and MOS transistors, V_{OSB} can be substantially less than V_{OSM} because $kT/q \approx$ 26 mV (at room temperature) whereas $V_{GS} - V_{TH} \approx$ 0.5–1 V. The lower offset of the bipolar latch permits a smaller gain in the preamplifier, resulting in a correspondingly faster response.

In order to generate 5-V CMOS levels at the output from a 200-μV input, the comparator must provide an equivalent gain of 25 000, a constraint that demands careful gain allocation among the three stages. In this design, the preamplifier has a gain of 20, while each of the two latches exhibits an equivalent gain of several thousand. As described in following subsections, these latches have a finite maximum gain because they steer a finite amount of charge.

B. BiCMOS Preamplifier

The preamplifier circuit is shown in Fig. 5. It comprises source followers $M1$ and $M2$, the differential pair $Q1$ and $Q2$, and emitter followers $Q3$ and $Q4$. The preamplifier gain is stabilized against variations in temperature by using bias currents proportional to absolute

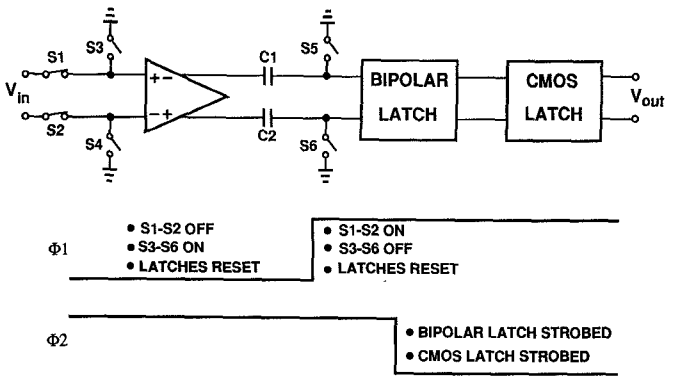

Fig. 4. BiCMOS comparator block diagram and timing.

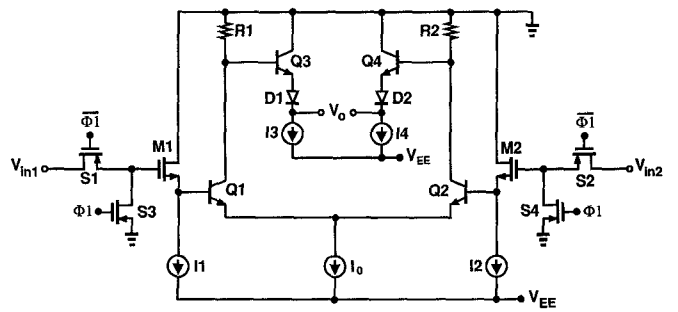

Fig. 5. BiCMOS preamplifier.

temperature. By virtue of the large transconductance of the bipolar transistors, the differential amplifier achieves a bandwidth of more than 100 MHz with a power dissipation of only 0.5 mW.

An important issue in the design of the preamplifier is the input noise. The flicker noise of MOS devices is quite substantial; as a consequence, large transistors must be used at the input unless this noise is reduced by offset cancellation. If the comparator offset is cancelled on every cycle, the time interval between offset cancellation and comparison does not exceed a few tens of nanoseconds. Hence, only those flicker noise components that change appreciably in this time interval will be significant. Due to the $1/f$ dependence of flicker noise, these components have very small magnitudes and thus are negligible. As a result, the source-follower dimensions are dictated only by thermal noise requirements.

Neglecting flicker noise, the preamplifier input-referred noise power density is [5]

$$\frac{\overline{v_n^2}}{\Delta f} = 4kT\left(\frac{1}{g_{m\mathrm{BJT}}}\right) + 4kT\left(2r_b + 2R_{SW} + \frac{2}{g_{m\mathrm{MOS}}}\right) \quad (8)$$

where $g_{m\mathrm{BJT}}$ and r_b are the transconductance and base resistance of $Q1$ and $Q2$, R_{SW} is the channel resistance of input switches, and $g_{m\mathrm{MOS}}$ is the transconductance of $M1$ and $M2$. In this equation the first term represents shot noise in the bipolar pair, while the second term embodies the various sources of thermal noise. For this design $\sqrt{\overline{v_n^2}} \approx 130\ \mu\mathrm{V}$ for a bandwidth of 100 MHz.

Emitter followers $Q3$ and $Q4$ buffer the outputs and, together with $D1$ and $D2$, shift the output voltage down to establish a bias across capacitors $C1$ and $C2$ in Fig. 4, which are simply large NMOS transistors in this implementation.

C. Bipolar Latch

A combined circuit diagram of the bipolar and CMOS latches is shown in Fig. 6. The bipolar latch consists of cross-coupled transistors $Q5$ and $Q6$ and a charge-pumping circuit, $M11$, $M12$, and $C3$. The coupling capacitors $C1$ and $C2$ act both as offset-storage elements and load devices for the bipolar latch. During calibration, Φ_1 is low, grounding the nodes $X1$ and $Y1$, and Φ_2 is high, discharging $C3$ to V_{EE}. During comparison, Φ_1 goes high and, after the preamplifier has sensed the input and a differential voltage is developed at $X1$ and $Y1$, Φ_2 goes low, turning $M12$ on and transferring charge through the bipolar pair. In a fashion similar to that described in [6], the voltage difference between nodes $X1$ and $Y1$ is regeneratively amplified until $C3$ charges up and the tail current of the pair falls to zero. This operation, which can be viewed as charge sharing between $C3$ and the combination of $C1$ and $C2$, occurs quickly because of the positive feedback around $Q5$ and $Q6$ and the large transconductance of these devices. With an initial voltage difference of 1 mV between nodes $X1$ and $Y1$, the latch produces a differential voltage of several hundred millivolts in less than 5 ns.

Since the bipolar latch steers charge, rather than current, it has two advantages over conventional current-steering bipolar latches: 1) it draws no input current during calibration and can therefore be directly coupled to $C1$ and $C2$ without input bias current cancellation, and 2) it has zero static power dissipation. Also, in this application the preamplifier need only attenuate the input offset resulting from the V_{BE} mismatch of the two bipolar transistors $Q5$ and $Q6$, rather than the larger V_{GS} mismatch of two MOS devices as would be necessary if a CMOS latch were used.

The charge-sharing nature of the bipolar latch introduces a relationship between gain and delay that differs from that for current-steering circuits. In the latter the gain can approach infinity if sufficient time is permitted for regeneration, while the former has a finite gain because of the limited charge available for regeneration. The Appendix presents an analysis of transient response of the charge-steering latch to better illustrate this behavior.

D. CMOS Latch

The last stage of the comparator is a CMOS latch, included in Fig. 6, that is used to generate CMOS levels from the output of the bipolar latch. It consists of sense transistors $M3$ and $M4$, cross-coupled devices $M5$–$M8$, reset transistors $M9$ and $M10$, and a CMOS clock delay inverter $G1$. The operation of this latch is based on charge sharing between $C1$ and the capacitance at the node $X2$, and between $C2$ and the capacitance at the node $Y2$. However, $C1$ and $C2$ are not significantly discharged by activation of the latch because they are much larger than

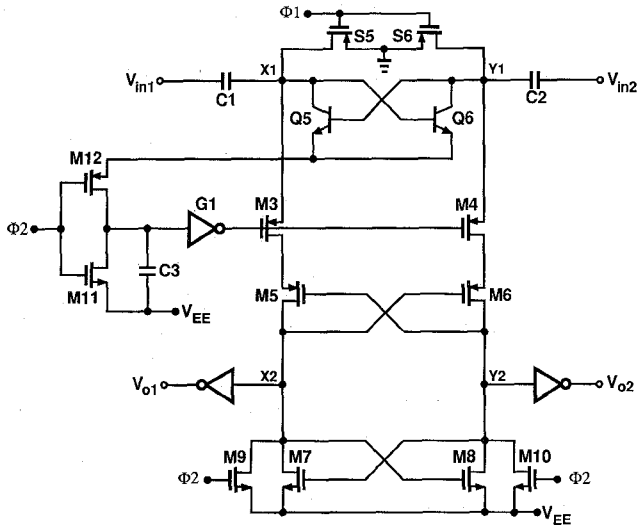

Fig. 6. Combined circuit of bipolar and CMOS latches.

the parasitics at $X2$ and $Y2$. As a result, the voltages at $X2$ and $Y2$ closely approach the supply rails.

The CMOS latch operates as follows. In the calibration mode, when Φ_2 is high, $M3$ and $M4$ are off, and $M9$ and $M10$ discharge $X2$ and $Y2$ to V_{EE}. In the comparison mode, Φ_2 goes low to strobe the bipolar latch and turn off $M9$ and $M10$. Then, following a delay controlled by $C3$, transistors $M3$ and $M4$ turn on, coupling the voltage difference between $X1$ and $Y1$ to the sources of $M5$ and $M6$ and initiating regeneration at nodes $X2$ and $Y2$. The regeneration continues until either $X2$ or $Y2$ reach the voltage at $X1$ or $Y1$, while the other returns to V_{EE}. Designed with short-channel devices for a fast response, this latch may have an input offset as high as 50 mV and thus must be strobed only after the bipolar latch has generated a sufficient voltage difference between $X1$ and $Y1$. This is ensured by setting the switching point of $G1$ above -3 V, so that its output does not go low until $C3$ has charged up by at least 2 V. Because $C3$ is approximately one-fifth the size of $C1$ and $C2$, a 2-V change in its voltage corresponds to a potential difference of at least 200 mV between $X1$ and $Y1$.

Another issue in the design of the CMOS latch is the disturbance it may cause at the sensitive nodes $X1$ and $Y1$ before the bipolar latch is strobed. In this circuit, the only disturbance arises from the clock and charge feedthrough of $M9$ and $M10$ as they turn off, and this is negligible because of the weak capacitive path from $X2$ and $Y2$ to $X1$ and $Y1$.

In order to prevent degradation of the $X1$ and $Y1$ common-mode voltage, $M3$ and $M4$, which remain on as long as Φ_2 is low, are followed by cross-coupled devices $M5$ and $M6$. For example, when $X2$ is low and $Y2$ is high $M5$ turns off, isolating $X1$ from $M7$, which would otherwise discharge $X1$ to one PMOS threshold voltage above V_{EE}.

E. Simulation Results

Figs. 7 and 8 show the simulated waveforms for the two latches. For clarity, the amplitudes of Φ_1 and Φ_2 (= 5 V) are reduced in these figures. Fig. 7 depicts the waveforms at nodes $X1$ and $Y1$. When Φ_1 goes high at $t = 2$ ns, the preamplifier senses the analog inputs (V_{in1} and V_{in2} in Fig. 5) and amplifies their difference, thus generating a differential voltage at $X1$ and $Y1$. At $t = 22$ ns, Φ_2 goes low to strobe the bipolar latch, thereby regeneratively amplifying the difference between V_{X1} and V_{Y1}.

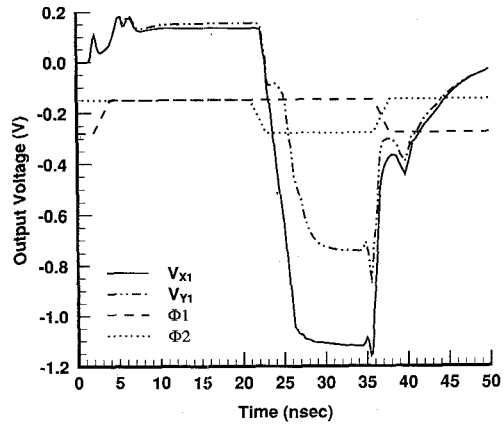

Fig. 7. Bipolar latch output waveforms (Φ_1 and Φ_2 amplitudes not to scale).

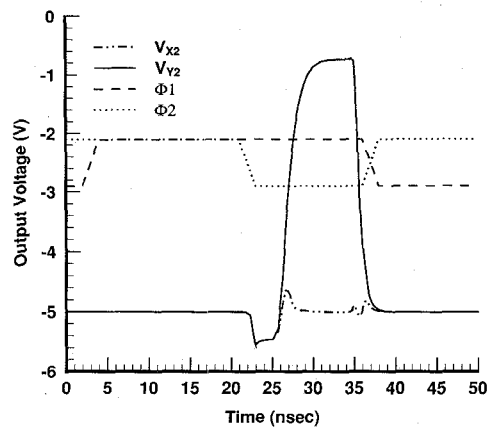

Fig. 8. CMOS latch output waveforms (Φ_1 and Φ_2 amplitudes not to scale).

Fig. 8 shows the waveforms at the outputs of the CMOS latch. As explained previously, the CMOS latch is activated by a delayed version of Φ_2. The output nodes $X2$ and $Y2$ are initially discharged to V_{EE}. Shortly after Φ_2 goes low, charge is transferred from nodes $X1$ and $Y1$ to nodes $X2$ and $Y2$. If, for example, $V_{X1} < V_{Y1}$, then more charge is transferred to $Y2$ than $X2$, and $Y2$ goes high while $X2$ is regeneratively pulled back to V_{EE}.

The degradation in the high level at $X1$ and $Y1$, which also appears as the high level of nodes $X2$ and $Y2$, is proportional to the ratio of the parasitics at $X2$ and $Y2$ to the coupling capacitors $C1$ and $C2$. For the minimum geometry devices used in the latch, this degradation is approximately 0.8 V.

IV. A Self-Calibrating CMOS Comparator

While BiCMOS technologies offer the potential of superior performance in both digital and analog circuits, many such technologies lack the passive components that

are essential for analog design. On the other hand, the prevalence of CMOS technology in system design has supported the incorporation of such components in many CMOS processes.

To improve the performance obtainable in a fully CMOS comparator, offset cancellation can be applied to both the preamplifier and the latch. The CMOS comparator described in this section employs a topology that achieves complete offset cancellation for both its preamplifier and latch, thereby making it possible to achieve 12-b precision at comparison rates as high as 10 MHz when implemented in a 1-μm technology.

A. Architecture

Fig. 9 is a simplified block diagram of the CMOS comparator. It consists of two transconductance amplifiers, G_{m1} and G_{m2}, sharing the same output nodes, load resistors R_{L1} and R_{L2}, and capacitors $C1$ and $C2$ in a positive feedback loop around G_{m2}. In the offset-cancellation mode, the inputs of G_{m1} and G_{m2} are grounded and their offsets are amplified and stored on $C1$ and $C2$. In the comparison mode, the inputs are released from ground and the input voltage is sensed. This voltage is amplified by G_{m1} to establish an imbalance at the output nodes A and B, and hence at the inputs of G_{m2}, initiating regeneration around G_{m2}.

The calibration of this comparator can be viewed as output offset storage applied to both G_{m1} and G_{m2}, resulting in complete cancellation of their offsets. This topology utilizes the offset-cancelled amplifier G_{m2} for regeneration, whereas a conventional OOS configuration incorporates an explicit latch that can suffer from large input offsets. Thus, neglecting second-order effects such as mismatch in charge injection from $S5$ and $S6$, the proposed topology achieves zero residual offset while retaining the advantages of OOS.

Owing to several complications, the block diagram of Fig. 9 is not practical if implemented directly as shown. First, the feedback capacitors and their parasitics load the output nodes, reducing the speed. Second, because of the finite on-resistance of $S5$ and $S6$, the positive feedback loop around G_{m2} is not completely broken in calibration mode, making the circuit prone to oscillation. More importantly, when $S5$ and $S6$ turn off to end the calibration, any mismatch in their charge injection can trigger a false regeneration around G_{m2}. Since the feedback is designed for a fast response, this regeneration may not be overridden by small voltages at the input, hence causing a large overall input-referred offset for the comparator. Fig. 10 illustrates a modified comparator configuration that circumvents these problems. In this circuit, buffers $B1$ and $B2$ isolate nodes A and B from the feedback capacitors, while switches $S7$–$S10$ disable the feedback loop when required. Regeneration begins only after the input voltage has been sensed and amplified. It should be noted that the offsets of $B1$ and $B2$ are also stored on $C1$ and $C2$.

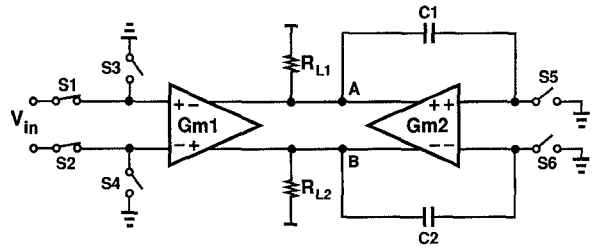

Fig. 9. CMOS comparator simplified block diagram.

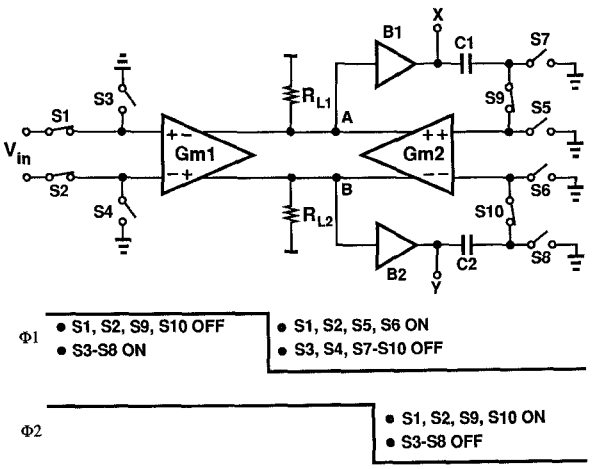

Fig. 10. Modified CMOS comparator block diagram and timing.

B. Circuit Details

A CMOS implementation of the topology in Fig. 10 is shown in Fig. 11. In this circuit, differential pairs $M1$, $M2$ and $M3$, $M4$ constitute amplifiers G_{m1} and G_{m2}, respectively, with source followers $M9$ and $M10$ serving as the buffers $B1$ and $B2$. Transistors $M7$ and $M8$ operate as active loads, while $M5$ and $M6$ set the output common-mode voltage and control the gain [2]. The additional currents supplied by $M7$ and $M8$ both decrease the voltage drop across $M5$ and $M6$ and increase the available gain, two important advantages when the circuit must operate from a single 5-V supply. Moreover, by boosting the currents that charge and discharge nodes A and B, the push–pull operation of $M3$ with $M7$ and $M4$ with $M8$ improves the large-signal response in two ways: it increases the output voltage swing and enhances the speed. This can be seen by noting that if, for example, node E goes high and node F goes low, the current in $M7$ is reduced, thus allowing $M3$ to more rapidly discharge node A to a lower voltage, while the current in $M8$ is increased, thereby pulling node B more quickly to a higher voltage.

Since the comparator of Fig. 11 includes calibration of both the preamplifier and the latch, its residual offset is due primarily to mismatches among switches $S5$–$S10$. Because of mismatches in their dimensions and threshold voltages, two nominally identical MOS devices carry slightly different charges in their inversion layers. This difference results in charge injection mismatch when the two switches turn off and charge absorption mismatch when they turn on. In the comparator circuit, both types of mismatch exist: charge injection mismatch from

$S5$–$S8$ when they turn off to end the calibration, and charge absorption mismatch from $S9$–$S10$ when they turn on to establish a positive feedback loop around G_{m2}.

Because $S5$ and $S6$ discharge their respective nodes to the same potential, their charge injection mismatch can be cancelled by an auxiliary switch placed between nodes E and F that turns off a few nanoseconds after $S5$ and $S6$, thereby equalizing the voltages at E and F [6]. With the same principle applied to $S7$ and $S8$, the charge absorption mismatch between $S9$ and $S10$ becomes the only significant contribution to the offset. This offset manifests itself when $S9$ and $S10$ turn on, absorbing charge from $C1$ and $C2$ into their channels. The charge absorption mismatch creates an offset voltage between the gates of $M3$ and $M4$ that is multiplied by the gain of the $M3$ and $M4$ pair when it appears at nodes A and B and is divided by the gain of the $M1$ and $M2$ pair when referred to the main input. The resulting input-referred offset is

$$V_{OS} = \frac{\Delta Q}{C} \frac{g_{m34} + g_{m78}}{g_{m12}} \tag{9}$$

where ΔQ is the channel-charge mismatch of $S9$ and $S10$ when they are on, $C = C1 = C2$, and g_{m34}, g_{m78}, and g_{m12} are the transconductance values of differential pairs $M3$–$M4$, $M7$–$M8$, and $M1$–$M2$, respectively. This equation indicates that, for a given ΔQ, V_{OS} can be reduced by: 1) increasing C, which increases the recovery and regeneration delays, as well as the area; 2) decreasing $g_{m34} + g_{m78}$, which is accomplished by decreasing $I2$ and not only degrades the regeneration speed but also lowers the output swing; and 3) increasing g_{m12}, which either increases the input capacitance (if $M1$ and $M2$ are widened) or limits the input and output swings (if $I1$ is increased). As a compromise among these trade-offs, $C = 0.5$ pF and $g_{m12} = 2(g_{m34} + g_{m78})$ were used in this design.

Equation (9) indicates that, in contrast to OOS and IOS configurations, the circuit in Fig. 11 imposes no constraint between the preamplifier voltage gain and the residual offset, thus allowing a better optimization of the load devices for speed and input range.

Since the flicker noise at the input of the comparator in Fig. 11 is removed by periodic offset cancellation, only thermal noise needs to be considered. If the noise contributions of source followers $M9$ and $M10$ and capacitors $C1$ and $C2$ are neglected, the total input-referred thermal noise power density is

$$\frac{\overline{v_n^2}}{\Delta f} = 8kT\left(\frac{g_{m12} + g_{m34} + g_{m56} + g_{m78}}{g_{m12}^2}\right) \tag{10}$$

where g_{mij} represents the transconductance of each device in the pair M_i, M_j. For this design, $\sqrt{\overline{v_n^2}} \approx 200\ \mu$V for a bandwidth of 80 MHz.

The comparator of Fig. 11 generates a differential output voltage of approximately 2.6 V. A second CMOS latch—such as the one in the BiCMOS comparator described in Section II—can be used to develop full CMOS levels from the differential output, as long as a carefully

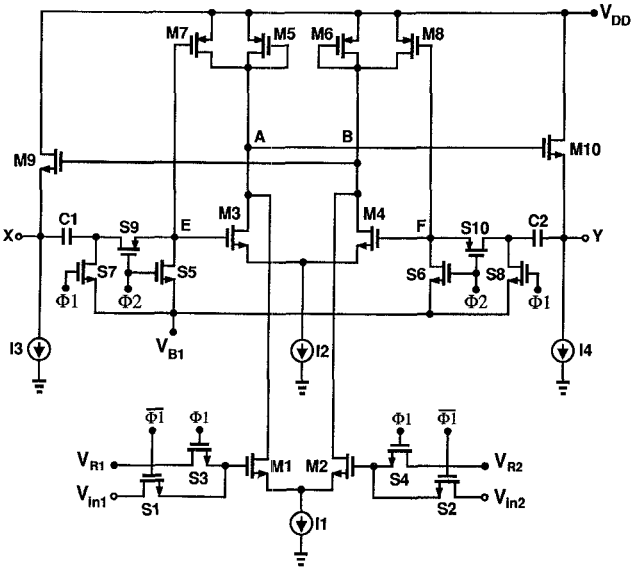

Fig. 11. CMOS comparator circuit diagram.

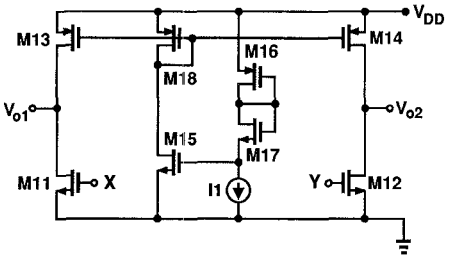

Fig. 12. CMOS comparator output amplifier.

delayed phase of Φ_2 is used to properly time the regeneration. A simpler approach is to employ a nonregenerative amplifier, such as the one shown in Fig. 12. Since the outputs X and Y of the comparator track the positive supply voltage by $|V_{GS6}| + V_{GS9}$ and $|V_{GS5}| + V_{GS10}$, respectively, the amplifier inputs cannot simply be referenced to ground because, under worst-case conditions of supply and process variations, the amplifier may not provide rail-to-rail swings at its output. By replicating the X and Y common-mode voltage at the source of $M17$, the circuit in Fig. 12 generates pull-up currents in $M13$ and $M14$ that, during reset, are twice the pull-down currents in $M11$ and $M12$ if the latter two are driven from X and Y. In this case, V_{O1} and V_{O2} closely approach the supply rails. Since a single bias network, $M15$–$M18$, can be used for an array of comparators, the equivalent power dissipation of the output amplifier remains below 0.5 mW.

C. Simulation Results

Simulated waveforms for the CMOS comparator are shown in Figs. 13 and 14, wherein the amplitudes of Φ_1 and Φ_2 (= 5 V) have been reduced for clarity. Fig. 13 depicts the waveforms at nodes X and Y. At $t = 2$ ns, Φ_1 goes low and the preamplifier senses the analog inputs (V_{in1} and V_{in2} in Fig. 11), amplifying their difference so as to produce a larger differential voltage at nodes X and Y. At $t = 6$ ns, Φ_2 goes low to close the positive feedback

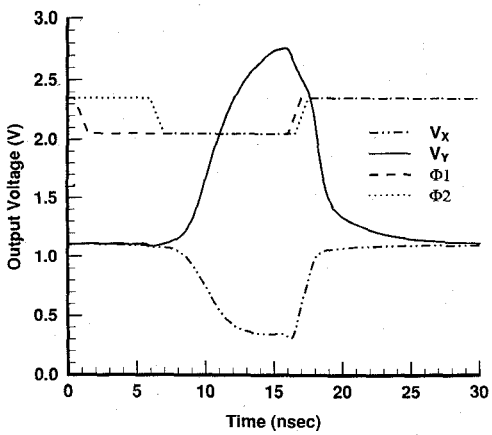

Fig. 13. CMOS comparator output waveforms (Φ_1 and Φ_2 amplitudes not to scale).

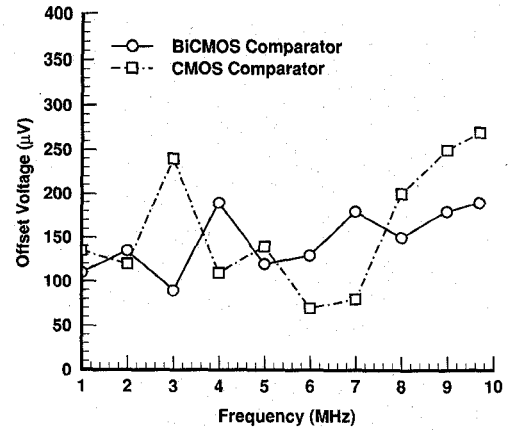

Fig. 15. Offset of comparators as a function of clock frequency.

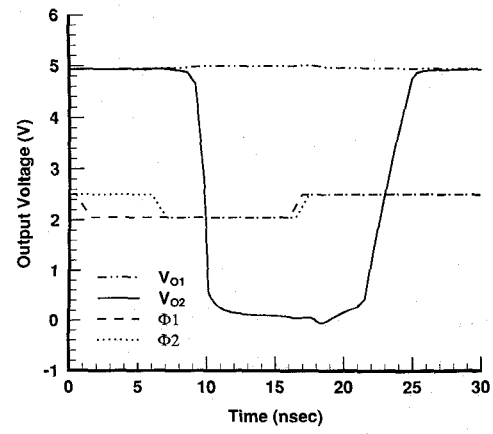

Fig. 14. Output amplifier waveforms (Φ_1 and Φ_2 amplitudes not to scale).

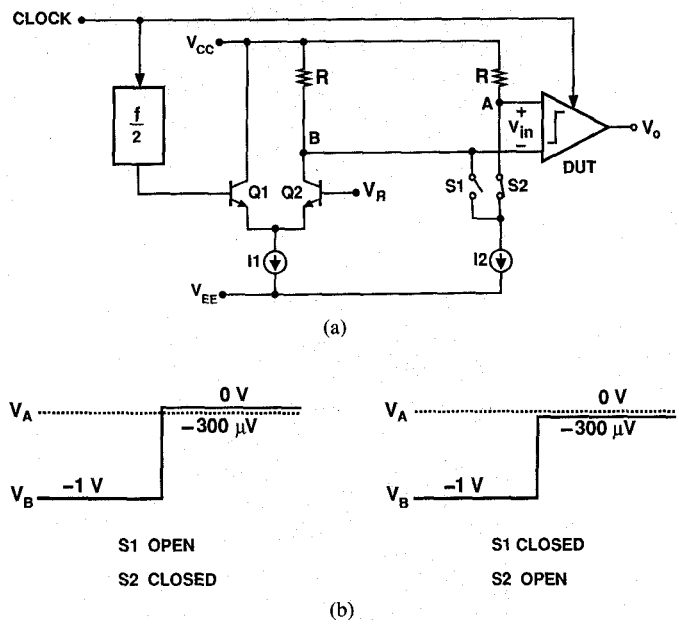

Fig. 16. Overdrive recovery test: (a) setup, and (b) dynamic input.

around G_{m2}, and $V_X - V_Y$ is amplified regeneratively. At $t = 16$ ns, the comparator is reset and returns to the offset cancellation mode.

Fig. 14 shows the V_{O1} and V_{O2} waveforms of the output amplifier. For a small difference between V_X and V_Y, V_{O1} and V_{O2} are both high. When $|V_X - V_Y|$ is amplified to a few volts, $|V_{O1} - V_{O2}|$ approaches full CMOS levels.

V. Experimental Results

The BiCMOS and CMOS comparators have been fabricated in a 2-μm BiCMOS process [7] and a 1-μm CMOS process [8], respectively. The performance of these experimental prototypes was evaluated for both dc and time-varying inputs. Typical measured input-referred offsets for two circuits are plotted as a function of the clock frequency in Fig. 15. The sharp variations in offset with frequency are attributed to ringing and clock coupling in the package and the test setup.

To demonstrate the effectiveness of the offset cancellation, as well as the overdrive recovery at 10 MHz, the circuit responses were also examined for dynamic inputs. The purpose of these tests is to verify that, at a 10-MHz comparison rate, the comparators can recover from a large differential input and subsequently detect a small differential input. Fig. 16(a) depicts the experimental setup employed for these tests [9]. In this circuit the differential waveform generated at the inputs of the comparator consists of a large voltage difference in one cycle and a small difference in the next. To generate this input signal the clock is divided in frequency by a factor of 2 and then applied to the bipolar differential pair $Q1$ and $Q2$ so that the voltage at node B remains low for one cycle and high for the next. The other input of the comparator is held at a dc voltage close to the high level at B. If the $Q1$, $Q2$ pair completely switches the current $I1$, then the magnitude and polarity of the small differential input that follows the large transition can be precisely controlled by the value of RI_2 and the position of switches $S1$ and $S2$. Two typical waveforms produced by this arrangement are illustrated in Fig. 16(b).

The oscillographs in Figs. 17 and 18 show that the comparators indeed accomplish full offset cancellation and overdrive recovery, yielding an output of one when $(V_{in1} - V_{in2})_{\text{BiCMOS}} = +300\ \mu\text{V}$ and $(V_{in1} - V_{in2})_{\text{CMOS}} = +1$ mV, and an output of zero when $(V_{in1} - V_{in2})_{\text{BiCMOS}} = -300\ \mu\text{V}$ and $(V_{in1} - V_{in2})_{\text{CMOS}} = -1$ mV.

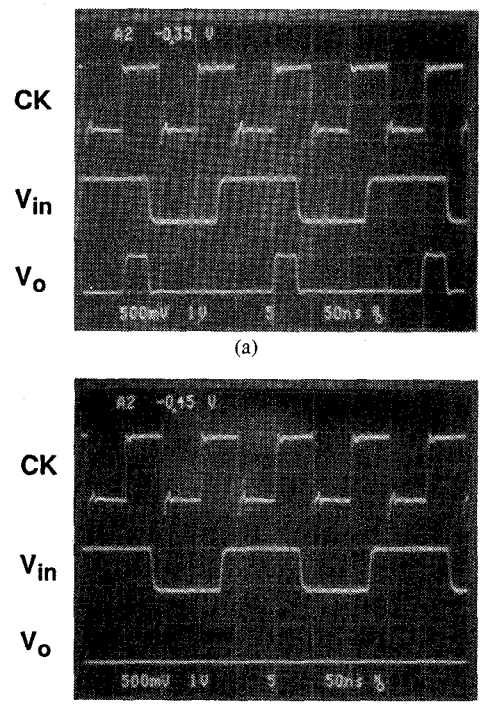

Fig. 17. BiCMOS comparator overdrive test: (a) $V_{in1} - V_{in2} = +300\ \mu V$, and (b) $V_{in1} - V_{in2} = -300\ \mu V$.

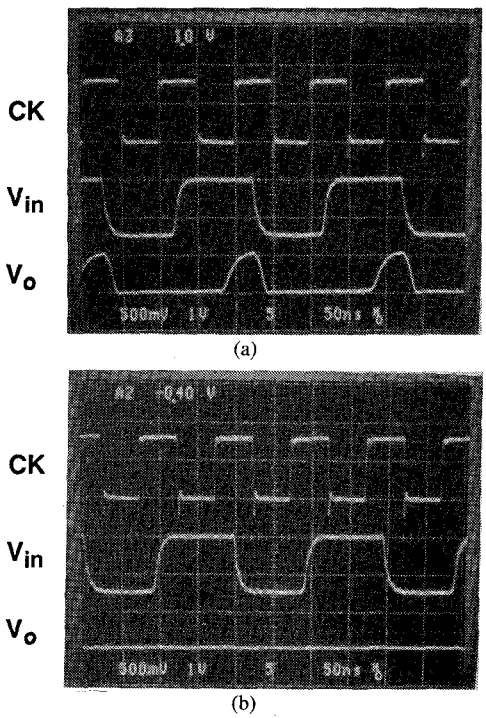

Fig. 18. CMOS comparator overdrive test: (a) $V_{in1} - V_{in2} = +1$ mV, and (b) $V_{in1} - V_{in2} = -1$ mV.

The performance of the two comparators is summarized in Table I. It can be seen that the BiCMOS comparator achieves a higher performance in a 2-μm process than the CMOS comparator in a 1-μm technology. Their low power dissipation and small input capacitance make both of these circuits suitable for integration in high-resolution parallel A/D converters.

TABLE I
PERFORMANCE OF BiCMOS AND CMOS COMPARATORS

	BiCMOS	CMOS
Input Offset	200 μV	300 μV
Comparison Rate	10 MHz	10 MHz
Input Range	3 V	2 V
Power	1.7 mW	1.8 mW
Power Supply	5 V	5 V
Input Capacitance	40 fF	40 fF
Area	100 × 250 μm^2	50 × 250 μm^2
Technology	2-μm BiCMOS	1-μm CMOS

VI. Conclusion

The design of fast precision comparators requires careful trade-offs among parameters such as speed, resolution, power dissipation, and input capacitance. The speed of a comparator is often limited by its preamplifier overdrive recovery, while the resolution is constrained by the input offset of its latch. Thus, if the latch offset is reduced in a reliable way, the preamplifier can be designed for lower gain and hence faster recovery.

The availability of bipolar and CMOS devices on the same substrate can be exploited to design high-performance compact analog circuits. In particular, the high speed and low offset of bipolar transistors together with the zero-offset switching and rail-to-rail swing capabilities of CMOS devices allow the implementation of fast amplifiers, sensitive latches, and low-power level translators. Employing these attributes, a 10-MHz BiCMOS comparator with a 200-μV input offset and a power dissipation of 1.7 mW has been designed.

A CMOS comparator utilizing a new offset cancellation technique has also been introduced. To achieve a small residual offset, this comparator combines a preamplifier and a regenerative latch, both with offset cancellation. This topology significantly relaxes the preamplifier gain requirements, allowing high speed and low power dissipation. The comparator maintains an offset of less than 300 μV at conversion rates up to 10 MHz while dissipating 1.8 mW.

Appendix
Transient Analysis of the Charge-Steering Latch

Fig. 19 depicts a general regenerative circuit consisting of two transconductance amplifiers in a positive feedback loop. The differential voltage between nodes X and Y in this circuit, denoted as v_{XY}, satisfies the equation

$$C\frac{dv_{XY}}{dt} = G_m v_{XY}. \tag{11}$$

A simplified version of the bipolar latch described in Section II is shown in Fig. 20, wherein R_{12} represents the equivalent resistance of transistor $M12$ in Fig. 6, and C includes load capacitance as well as C_μ and C_π of $Q5$ and $Q6$. The transconductance of $Q5$ and $Q6$, g_m, varies from approximately $(V_{EE} - V_{BE})/R_{12}V_T$, where $V_T = kT/q$

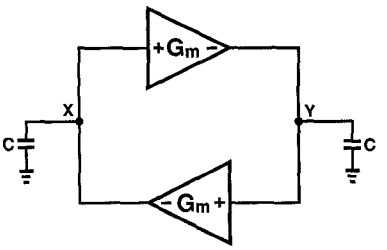

Fig. 19. Regenerative amplifier.

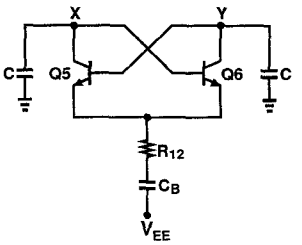

Fig. 20. Simplified circuit of bipolar latch.

(when $M12$ turns on) to zero (when the drain current of $M12$ falls to zero). Therefore, $Q5$ and $Q6$ cannot be simply replaced with a small-signal equivalent circuit and (11) cannot be applied to this case. However, by deriving a time-dependent representation of g_m and substituting it for G_m in (11), an estimate of the equivalent gain of the latch can be obtained. A comparison of analytical results and SPICE simulations indicates that this approximation is indeed representative of the latch's behavior.

The current through R_{12} in Fig. 20, i_{D12}, can be approximated as

$$i_{D12} \approx \frac{V_{EE} - V_{BE}}{R_{12}} \exp\left(\frac{-t}{R_{12}C_B}\right). \tag{12}$$

If, for the moment, the base resistance of $Q5$ and $Q6$ is neglected and β is assumed to be infinite, g_m is approximately

$$g_m = \left[r_e + \frac{2R_{12}V_T}{V_{EE} - V_{BE}} \exp\left(\frac{t}{R_{12}C_B}\right)\right]^{-1} \tag{13}$$

where r_e is the emitter resistance of $Q5$ and $Q6$. In (13) the collector currents of $Q5$ and $Q6$ are assumed equal. Since this only holds for small v_{XY}, the analysis is valid for amplification of very small signals, and in fact gives an upper bound for the equivalent gain of the latch.

Substituting (13) in (11) and rearranging terms yields

$$C\frac{dv_{XY}}{v_{XY}} = \frac{dt}{r_e + \frac{2R_{12}V_T}{V_{EE} - V_{BE}} \exp\left(\frac{t}{R_{12}C_B}\right)}. \tag{14}$$

Integrating both sides of this expression

$$\int_{v_{XY0}}^{v_{XY}} C\frac{dv_{XY}}{v_{XY}} = \int_0^t \frac{dt}{r_e + \frac{2R_{12}V_T}{V_{EE} - V_{BE}} \exp\left(\frac{t}{R_{12}C_B}\right)} \tag{15}$$

where v_{XY0} is the initial imbalance applied to the latch. Since

$$\int \frac{dt}{a + b\exp(t/\tau)} = -\frac{\tau}{a}\ln\left(1 + \frac{a}{b}\exp\frac{-t}{\tau}\right) \tag{16}$$

(15) can be written as

$$\ln\frac{v_{XY}}{v_{XY0}} = -\frac{R_{12}C_B}{r_eC}\ln\left[1 + \frac{r_e(V_{EE} - V_{BE})}{2R_{12}V_T} \cdot \exp\left(\frac{-t}{R_{12}C_B}\right)\right] + \frac{R_{12}C_B}{r_eC} \cdot \ln\left[1 + \frac{r_e(V_{EE} - V_{BE})}{2R_{12}V_T}\right]. \tag{17}$$

The asymptotic equivalent gain of the circuit can be obtained by letting $t \to \infty$ in (17) and solving for v_{XY}/v_{XY0}. For $t = \infty$, the first term on the right-hand side of (17) vanishes; hence

$$\ln\frac{v_{XY\infty}}{v_{XY0}} = \frac{R_{12}C_B}{r_eC}\ln\left[1 + \frac{r_e(V_{EE} - V_{BE})}{2R_{12}V_T}\right] \tag{18}$$

where $v_{XY\infty}$ is the final voltage difference between X and Y. The second term within the square brackets in (18) is typically less than 0.2. Since for small x, $\ln(1 + x) \approx x - x^2/2$, (18) can be approximated accordingly to yield

$$\frac{v_{XY\infty}}{v_{XY0}} = \exp\left(\frac{C_B}{C}\frac{V_{EE} - V_{BE}}{2V_T}\right) \cdot \exp\left[-\frac{r_eC_B}{2R_{12}C}\left(\frac{V_{EE} - V_{BE}}{2V_T}\right)^2\right]. \tag{19}$$

The first exponential term in (19) represents the maximum available gain of the latch. The second term takes into account the effect of finite emitter resistance of $Q5$ and $Q6$ and, as simulations show, can also include base resistance r_b by replacing r_e with $r_e + r_b/\beta$. For typical values used in this design, (19) gives an asymptotic equivalent gain of approximately 8000 for the latch.

Acknowledgment

The authors wish to thank Dr. P. Lim for his invaluable comments. They are also indebted to Dr. J. Shott and the Stanford Integrated Circuits Laboratory staff for fabricating the BiCMOS prototype, and to National Semiconductor Corporation and L. Stoian for supporting this work and fabricating the CMOS prototype.

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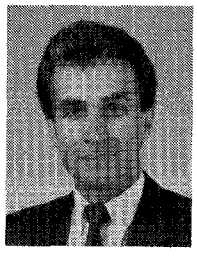

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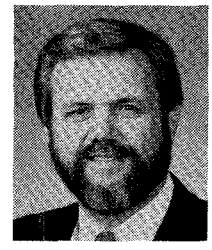

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