A 10-Bit 800-MHz 19-mW CMOS ADC

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***Abstract*—A pipelined ADC employs charge-steering op amps to relax the trade-offs among speed, noise, and power consumption. Such op amps afford a fourfold increase in speed and a twofold reduction in noise for a given power consumption and voltage gain. Applying full-rate nonlinearity and gain error calibration, a prototype realized in 65-nm CMOS technology exhibits a Nyquist SNDR of 52.2 dB and draws 19 mW at 800 MHz. The ADC also demonstrates a new histogram-based background calibration technique.**

***Index Terms*—Charge-steering, digital calibration, dynamic op amp, nonlinearity correction, pipelined ADCs.**

I. Introduction

THE raw performance of pipelined analog-to-digital converters (ADCs) primarily hinges upon that of their constituent op amps. The voltage gain and output swing limitations imposed by technology and supply scaling have motivated various digital correction techniques that afford the use of low-gain op amps in high-resolution ADCs [1]–[3]. For example, the designs in [4]–[6] have progressively reduced the residue amplifier complexity and gain, eventually reaching a simple resistively-loaded differential pair with capacitive feedback.

This work explores the notion of charge steering in the design of op amps and ADCs [7]. It is shown that charge-steering op amps offer significant advantages over their continuous-time (or switched) counterparts. A full-speed foreground calibration method along with a background calibration scheme are proposed that improve the performance of charge-steering op amps to the 10-bit level, achieving a low-frequency figure of merit (FoM) of 53 fJ/conversion-step at a sampling rate of 800 MHz.

Section II describes the charge-steering op amp and its properties. Section III presents the ADC architecture and Sections IV and V the foreground and background calibration techniques, respectively. Section VI summarizes the experimental results.

II. Charge-Steering Op Amps

A. Basic Idea

The concept of charge steering has been recently revived as a means of achieving low power dissipation at high speeds [8]. While not identified as such, this concept has also been utilized in op amps in [9], [10], and [11] but only in open-loop configurations and for linearities of 7 bits or less, and in comparators in [12] and [13].

A continuous-time differential pair can be transformed to a charge-steering stage as shown in Fig. 1(a): the load resistors are replaced with load capacitors, and the tail current source with a charge sink. In the reset mode, nodes X and Y are precharged to V_{DD} and the tail is left open. In the amplification mode, X and Y are released, the tail sink begins to draw current from the differential pair, and V_X and V_Y experience both a differential and a common-mode (CM) change.

The choice of the tail charge sink in Fig. 1(a) determines whether or not V_X and V_Y eventually collapse to zero. If the tail employs a capacitance comparable to C_X and C_Y [8], then V_X and V_Y have only moderate swings. On the other hand, for a large tail capacitance or a switch directly tied to ground, V_X and V_Y fall to zero. For reasons that become clear below, we choose the latter here.

Fig. 1(b) sketches the single-ended and differential output waveforms of the circuit, revealing that the amplified differential signal is available around $t = t_1$, but diminishes thereafter because V_X and V_Y collapse. Thus, V_{XY} must be captured by the following stage before t_1. Another issue is that the peak voltage gain provided by one charge-steering stage is limited to about 5, making nonlinearity calibration difficult. This is because such a low gain gives rise to a high closed-loop nonlinearity, demanding high-order polynomials and creating greater sensitivity to PVT variations. Nonetheless, we note that, if the conduction period from t_0 to t_2 is short compared to the clock cycle, the circuit can achieve a low power consumption—as quantified in Section II-B.

In order to capture the output, another charge-steering stage can follow the first. Illustrated in Fig. 2(a), the idea is to enable the two stages simultaneously: the second stage continues to amplify until the outputs of the first stage fall below one NMOS threshold, holding the output thereafter. As shown in Fig. 2(b), once V_X and V_Y are low enough, V_P and V_Q freeze, and V_{PQ} represents $V_{\rm in}^+ - V_{\rm in}^-$ amplified by *two* stages. The overall gain can now reach about 10 in a practical design.

The waveforms in Fig. 2(b) assume that both the peak differential output of the first stage and the turn-off of the second stage occur at t_1. In general, the former depends on the main input CM level, but this coincidence can be roughly realized in a typical design.

In addition to consuming low power, charge-steering op amps offer three other unique and useful characteristics. First, their power dissipation linearly scales with the clock frequency, allowing one design to be used at multiple rates. In fact, the ADC described in this paper can operate from low frequencies to

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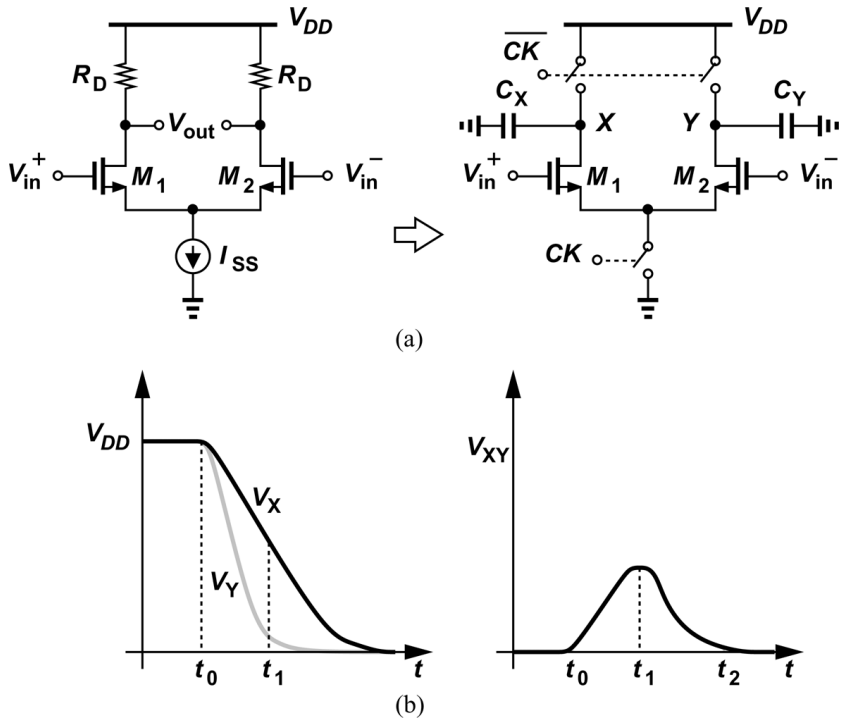

Fig. 1. (a) Transformation of current-steering pair to charge-steering amplifier; (b) output waveforms.

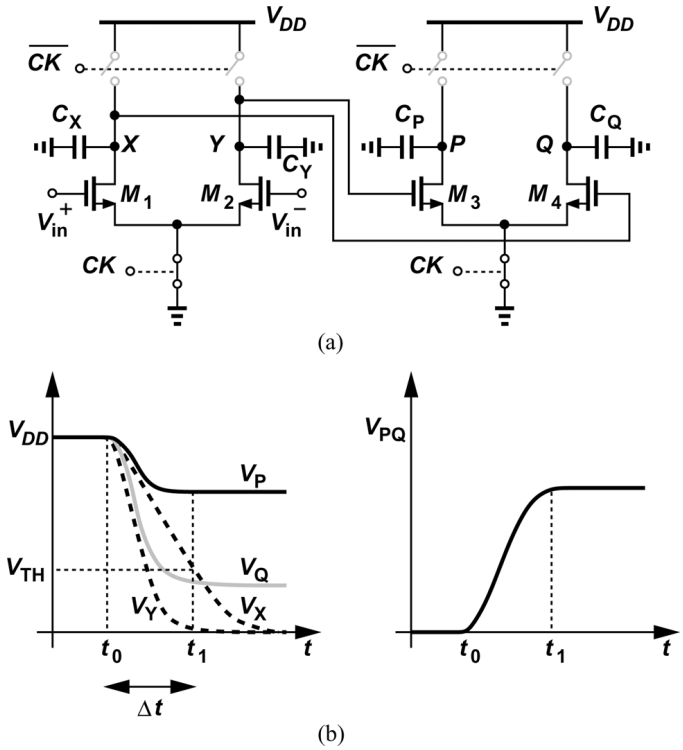

Fig. 2. (a) Two-stage charge-steering amplifier; (b) output waveforms.

800 MHz with a scalable power. Second, their gain can be raised by means of positive capacitive feedback. Third, they need not be stable in closed-loop operation! We discuss the latter two attributes in Sections II-D and II-F.

B. Gain Analysis

The small-signal voltage gain of the two-stage op amp in Fig. 2(a) is derived by noting that each stage integrates the differential MOS drain currents on its load capacitors. The transconductance of M_1 and M_2 remains relatively constant from t_0 to t_1, whereas that of M_3 and M_4 begins from a maximum $g_{m3,4\,\max}$, and falls to zero. Moreover, the differential voltage sensed by the second stage, V_{XY}, begins from zero at t_0 and reaches a maximum at t_1. We assume $\lambda = 0$ and $V_{\rm in}^+ - V_{\rm in}^- = V_{\rm in}$ is constant, and $t_0 = 0$ and write

$$V_{XY}(t) = \int \frac{g_{m1,2}}{C_X} V_{\rm in} dt = \frac{g_{m1,2}}{C_X} V_{\rm in} t \tag{1}$$

and use this result to drive the second stage:

$$V_{PQ}(t_1) = \int_{t_0}^{t_1} \frac{g_{m3,4}(t)}{C_P} \left(\frac{g_{m1,2}}{C_X} V_{\rm in} t \right) dt. \tag{2}$$

We now approximate $g_{m3,4}(t)$ by a linearly-declining function $(-g_{m3,4\,\max}/\Delta t)t + g_{m3,4\,\max}$ where $\Delta t = t_1 - t_0$. Such a function exhibits an average value $\overline{g_{m3,4}} = g_{m3,4\,\max}/2$. It follows that

$$V_{PQ}(t_1) = \frac{1}{3} \frac{g_{m1,2}}{C_X} \frac{\overline{g_{m3,4}}}{C_P} \Delta t^2 V_{\rm in}. \tag{3}$$

Our derivations assume that M_3 and M_4 turn off at the same time, a reasonable approximation if the op amp input is small and V_X and V_Y diverge by only a moderate amount. For large inputs, one can define an "effective" turn-off time for the second stage, e.g., half-way between when M_3 turns off and when M_4 turns off, but at the cost of more complex calculations.

If channel-length modulation is significant, the gain calculation becomes more complex as the transistor output resistances tend to discharge the voltage developed on the load capacitors. In order to simplify the analysis, we first observe that the input common-mode voltage and hence drain currents of the second differential pair decrease during the amplification phase, causing the output resistance to rise and eventually go to infinity as the pair shuts off. The effect of this resistance can be neglected because it draws a small current both at the beginning—when the differential output voltage is small—and near the end—when the resistance itself is large. Modeling the first pair output resistance by an average value, $r_{O1,2}$, we express the main output as

$$\begin{aligned} V_{PQ}(t_1) &= \frac{V_{\text{in}}}{C_P}\int_{t_0}^{t_1} g_{m1,2}r_{O1,2}\left(1-\exp\frac{-t}{\tau}\right) \\ &\quad\times\left(g_{m3,4\,\max}-\frac{g_{m3,4\,\max}}{\Delta t}t\right)dt \\ &= \frac{V_{\text{in}}}{C_P}g_{m1,2}g_{m3,4\,\max}r_{O1,2}\left[\frac{\Delta t}{2}-\tau\exp\frac{-\Delta t}{\tau}\right. \\ &\quad\left.+\left(\frac{\tau^2}{\Delta t}-\tau\right)\left(1-\exp\frac{-\Delta t}{\tau}\right)\right] \end{aligned} \tag{4}$$

where $\tau = r_{O1,2}C_X$. This expression is remarkably accurate, predicting the gain with less than 3% error with respect to simulations. The above equation has been derived for a constant-input common-mode level. In the closed-loop MDAC configuration, on the other hand, the input CM level drops as a result of the fall in the output CM level. According to simulations, this drop increases the open-loop gain by about 15%.

C. Noise Analysis

The charge-steering op amp of Fig. 2(a) exhibits two types of thermally-induced noise: (a) the kT/C noise deposited by the precharge switches on C_X, C_Y, C_P, and C_Q, and (b) the noise current of M_1–M_4 after integration on the load capacitors. We first focus on the latter, seeking the statistical properties of two functions: 1) white noise subjected to an integrate-and-dump operation, i.e., if white noise is integrated for a certain amount of time and the result is subsequently reset; 2) white noise convolved with a time-varying function and then subjected to an integrate-and dump operation. The former corresponds to an ideal charge-steering stage, and the latter to one with channel-length modulation. In the following derivations, the time origin, t_0, in Figs. 1 and 2 is assumed to be zero.

Since the drain noise current of a MOSFET has a two-sided spectrum given by $2kT\gamma g_m$, we can express the time-domain behavior as [14]

$$I_D(t) = \sqrt{2kT\gamma g_m}n(t) \tag{5}$$

when $n(t)$ is a white noise process with a spectral density of $S_n(f) = 1$. If applied to a capacitor C_L with a zero initial condition, $I_D(t)$ produces a noise voltage equal to

$$V_{\text{int}}(t) = \frac{1}{C_L}\int\sqrt{2kT\gamma g_m}n(t)dt. \tag{6}$$

Of interest to us here is the variance of this voltage, $E[V_{\text{int}}^2(t)]$, a quantity akin to the total average power of band-limited functions. To compute the variance of (6), we must resort to Ito's calculus [15], which proves that

$$E\left[\left(\int n(t)dt\right)^2\right] = E\left[\int dt\right] = t \tag{7}$$

if $n(t)$ is white noise.

This result implies that the power of integrated white noise grows linearly with the integration time. For example, if $\lambda = 0$, the output noise of the first stage in Fig. 2 due to M_1 and M_2 can be written as

$$E\left[V_{XY}^2(t)\right] = 2\frac{2kT\gamma g_{m1,2}}{C_X^2}t \tag{8}$$

where the factor of 2 accounts for the noise of both transistors.

In the presence of channel-length modulation, the drain noise current is convolved with the impulse response of a lossy integrator, i.e., $\exp[-t/(r_OC_L)]$. Thus, (6) must be modified to

$$\begin{aligned} V_{\text{int}}(t) &= \frac{\sqrt{2kT\gamma g_m}}{C_L}\int_0^t n(\alpha)\exp\frac{-(t-\alpha)}{r_OC_L}d\alpha \\ &= \frac{\sqrt{2kT\gamma g_m}}{C_L}\exp\frac{-t}{r_OC_L}\int_0^t\exp\frac{\alpha}{r_OC_L}n(\alpha)d\alpha. \end{aligned} \tag{9}$$

Ito's calculus also prescribes a simplification for the variance in this case:

$$E\left[\left(\int G(t)n(t)dt\right)^2\right] = E\left[\int G^2(t)dt\right]. \tag{10}$$

Noting that $\exp[\alpha/(r_OC_L)]$ in (9) can be viewed as $G(t)$, we have for the differential output noise of the first stage:

$$E\left[V_{XY}^2(t)\right] = 2\frac{kT\gamma g_{m1,2}r_{O1,2}}{C_X}\left(1-\exp\frac{-2t}{r_{O1,2}C_X}\right). \tag{11}$$

As expected, for long integration times, the output noise approaches $2\gamma g_{m1,2}r_{O1,2}(kT/C_X)$. The op amp designs in this work require the use of (11) as neither channel-length modulation is negligible nor t is large.

Before extending the foregoing calculations to two-stage op amps, we must revisit the initial switch-induced kT/C noise at nodes X and Y. With a finite transistor output resistance, this noise *decays* with time and does not fully contribute to the final output noise. For this reason, each switch-induced kT/C noise component must be multiplied by $\exp[-2t/(r_OC_L)]$ (as can be formally proved using Ito's integrals).

The output noise computation for a two-stage op amp and with $\lambda > 0$ is more involved. It can be shown that

$$\begin{aligned} E\left[V_{PQ}^2(t)\right] &= \frac{2kT\gamma g_{m1,2}r_{O1,2}}{5C_X}A_2^2\left(1-\exp\frac{-2t}{r_{O1,2}C_X}\right) \\ &\quad+2A_2^2\frac{kT}{C_X}\exp\frac{-2t}{r_{O1,2}C_X} \\ &\quad+\frac{2kT\gamma\overline{g_{m3,4}}r_{O3,4}}{C_P}\left(1-\exp\frac{-2t}{r_{O3,4}C_P}\right) \\ &\quad+\frac{2kT}{C_P}\exp\frac{-2t}{r_{O3,4}C_P}, \end{aligned} \tag{12}$$

where A_2 is the gain of the second stage and equal to $\overline{g_{m3,4}}r_{O3,4}\{1 - \exp[-t/(r_{O3,4}C_P)]\}$. The first and third terms represent the differential pair contributions, and the second and fourth terms the decaying kT/C noise components. In a typical design, the differential pair noise contributions are more than 10 times greater than the kT/C terms.

D. Power Consumption

The average power consumption of the op amp can be computed as follows. First, suppose the differential input in Fig. 2(a) is zero and the second stage output CM level is reset to V_{DD}. In each cycle, nodes X and Y swing between V_{DD} and zero and nodes P and Q between V_{DD} and $V_{DD}/2$. The average power drawn from the supply is therefore equal to

$$P_{\text{avg}} = 2\left(\frac{C_{X,\text{tot}}V_{DD}}{T_{CK}} + \frac{C_{P,\text{tot}}V_{DD}/2}{T_{CK}}\right)V_{DD} = 2f_{CK}\left(C_{X,\text{tot}} + \frac{C_{P,\text{tot}}}{2}\right)V_{DD}^2 \quad (13)$$

where the subscript total denotes the inclusion of transistor capacitances at each node as well, and T_{CK} and f_{CK} are the clock period and frequency, respectively. This result is also accurate for nonzero differential inputs. Simulations indicate less than 0.5% change in the power consumption as the input difference goes from zero to 60 mV (and hence the output from 0 to 600 mV). Equation (13) reveals that, once the power budget is given, the node capacitances are also known to some extent because $C_{X,\text{tot}} + C_{P,\text{tot}}/2$ is known and, in a typical design, $C_{P,\text{tot}}$ is roughly twice $C_{X,\text{tot}}$ (Fig. 2(a)).

The design procedure begins with a power budget and chooses rough values for $C_{X,\text{tot}}$ and $C_{P,\text{tot}}$ according to (13). Next, the first differential pair is sized such that nodes X and Y in Fig. 2(a) fall to one threshold above the ground in the required time, Δt. In the last step, the second differential pair is sized to establish an output CM level of around $V_{DD}/2$ by the time M_3 and M_4 turns off. Based on these preliminary design choices, the open-loop gain can be calculated from (4) and if it is insufficient, Δt must be chosen longer and the input transistors, narrower. Lastly, if the noise calculated from (12) is too high, a greater power budget is required.

E. Closed-Loop Behavior

The discrete-time nature of charge-steering op amps leads to interesting and useful closed-loop properties. In a typical multiplying digital-to-analog converter (MDAC) stage of a pipelined ADC, the op amp is configured as shown in Fig. 3(a) while the charge sampled on C_{in} flows to C_F and V_{out} goes from zero toward its final value.[1] A conventional op amp must exhibit adequate phase margin here for proper settling but a charge-steering op amp need not.

A charge-steering op amp employing two ideal integrating stages becomes completely unstable in the MDAC environment of Fig. 3(a). Fortunately, however, the second stage turns off after Δt seconds, and the output remains frozen [Fig. 3(b)]. Since channel-length modulation is significant, we analyze this phenomenon with $\lambda > 0$, i.e., with lossy integrators. The small-signal model shown in Fig. 3(c)[2] allows us to determine the loop transmission, $T(s)$, as

$$T(s) = \frac{C_F}{C_{\text{in}} + C_F} \cdot \frac{g_{m1,2}r_{O1,2}}{r_{O1,2}C_X s + 1} \cdot \frac{g_{m3,4}r_{O3,4}}{r_{O3,4}C_{eq}s + 1} \quad (14)$$

where $C_{eq} = C_P + C_{\text{in}}C_F/(C_{\text{in}} + C_F)$. Equating $T(s)$ to -1 yields the closed-loop poles as follows:

$$\omega_{p1,2} = \frac{-(r_{O1,2}C_X + r_{O3,4}C_{eq}) \pm \sqrt{D}}{2r_{O1,2}r_{O3,4}C_X C_{eq}} \quad (15)$$

where $D = r_{O1,2}^2C_X^2 + r_{O3,4}^2C_{eq}^2 - 2r_{O1,2}r_{O3,4}C_X C_{eq} - 4g_{m1,2}r_{O1,2}^2 g_{m3,4}r_{O3,4}^2 C_X C_{eq}C_F/(C_{\text{in}} + C_F)$. With typical values, the fourth term in D dominates and hence For the first MDAC stage in our ADC, we have $\omega_{p1,2} \leq 2\pi(-3.0 \pm j14.6)$ GHz, obtaining a damping factor of about 0.2. Equation (16) reveals that a closed-loop, two-stage charge-steering op amp exhibits two complex poles and an underdamped response.

This study indicates that the design of charge-steering op amps markedly departs from the conventional wisdom. The closed-loop circuit is allowed to be unstable so long as the stages turn off around the first peak value at the output.

We should note that, owing to the "self-timed" nature of the op amp, the gain[3] is *not* affected by the clock jitter: since the time at which the second stage turns off is determined by the circuit itself, a clock edge displacement shifts both the beginning and the end of the amplification phase by the same amount. As the waveform in Fig. 3(b) suggests, it is possible to select the turn-off time of the second stage, Δt, equal to half of the oscillation period, thereby achieving maximum voltage gain—in fact, a gain even greater than C_{in}/C_F! One concern in this case is the PVT variations of the closed-loop gain. For example, we wish to determine the change in the gain if Δt changes by a small amount, ϵ, According to simulations, if $\epsilon =$

[1]In an ADC environment, the op amp's internal and output nodes are preiodically reset to V_{DD}, the virtual ground node to a bias, and C_{in} to a reference voltage.

[2]Capacitor C_P in this figure includes the load capacitor, C_L, in Fig. 3(a).

[3]We define the closed-loop gain as the final output voltage divided by the sampled input.

$$\omega_{p1,2} = \frac{-(r_{O1,2}C_X + r_{O3,4}C_{eq}) \pm 2j\sqrt{g_{m1,2}g_{m3,4}C_X C_{eq}C_F/(C_{\text{in}} + C_F)}r_{O1,2}r_{O3,4}}{2r_{O1,2}r_{O3,4}C_X C_{eq}} \quad (16)$$

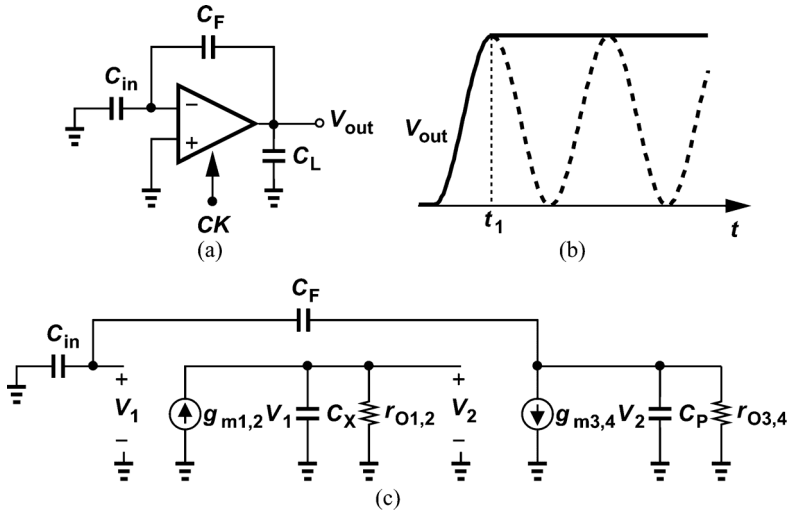

Fig. 3. (a) Closed-loop charge-steering amplifier, (b) step response, and (c) small-signal model.

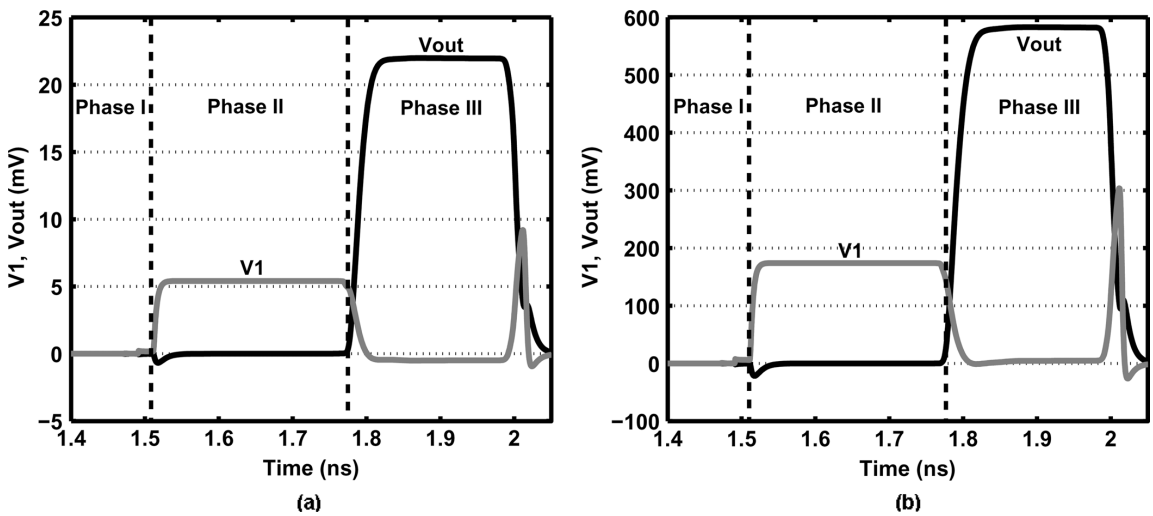

Fig. 4. Transient simulation of closed-loop op amp with (a) 10-mV input, and (b) 300-mV input.

10 ps, the closed-loop gain changes by less than 1%. Simulations suggest that as the temperature varies from 0 to 70°C, the closed-loop gain changes by less than 3.5%. The foreground and background calibration techniques presented later deal with systematic variations.

The sensitivity of the closed-loop gain to the ringing frequency, $\omega_{\rm ring}$, is also of interest. For $C_{\rm in} = 2C_F$, (16) gives $\omega_{\rm ring} = \sqrt{g_{m1,2}g_{m3,4}/(3C_XC_{eq})}$. We recognize that $\omega_{\rm ring}$ is proportional to the square root of the product of two g_m/C ratios while the turn-off time is inversely proportional to the g_m/C ratio of the first stage. We therefore surmise that the ringing period and the turn-off time track to some extent. For example, simulations suggest that a 20% reduction in all the capacitor values changes the closed-loop gain by less than 1.6%. The turn-off time can be expressed as

$$\Delta t = \frac{C_X(V_{DD} - V_{\rm th})}{I_{D1,2}} = \frac{2C_X(V_{DD} - V_{\rm th})}{\mu C_{ox}\left(\frac{W}{L}\right)_{1,2}(V_{GS1,2} - V_{th})^2} \tag{17}$$

and the first peak time for a second-order system as

$$t_p = \frac{\pi}{\omega_{\rm ring}} = \pi\sqrt{\frac{3C_XC_{eq}}{g_{m3,4}\mu C_{ox}\left(\frac{W}{L}\right)_{1,2}(V_{GS1,2} - V_{\rm th})}}. \tag{18}$$

Equations (17) and (18) show that Δt and t_p are inversely proportional to $(V_{GS1,2} - V_{\rm th})^2$ and $\sqrt{V_{GS1,2} - V_{\rm th}}$ respectively, suggesting that the relative time between Δt and t_p can be defined by $V_{GS1,2}$. Simulations indicate a 4% change in the closed-loop gain when the starting $V_{GS1,2}$ bias point is varied by 50 mV.

Fig. 4(a) shows the transient simulation of the closed-loop op amp with a small input. During Phase I, a 10-mV input is sampled on $C_{\rm in}$ while the op amp is reset. During Phase II, $C_{\rm in}$ switches to the common-mode ground, generating a differential voltage V_1 between the virtual-ground nodes. In Phase III, the op amp is clocked, amplifying V_1 and producing a rising $V_{\rm out}$. By virtue of negative feedback, $V_{\rm out}$ forces V_1 to converge

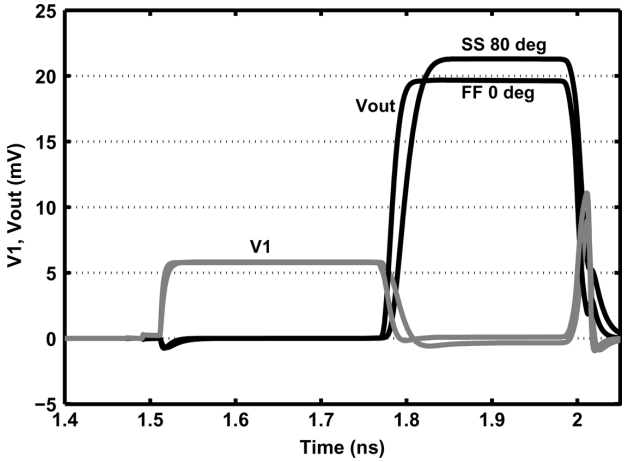

Fig. 5. Transient simulation of closed-loop op amp over corners.

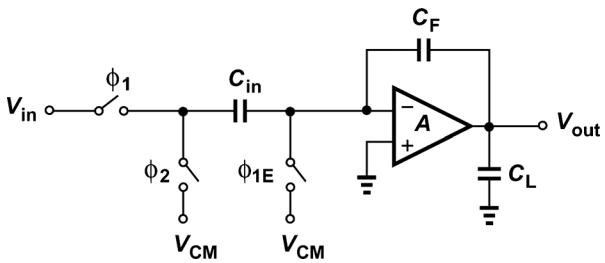

Fig. 6. MDAC environment for comparison of op amps.

to 0 V, but due to the underdamped behavior, V_1 undershoots 0 V while $V_{\rm out}$ overshoots its target value (20 mV). Before the closed-loop system has a chance to correct the under/overshoots, the self-timed op amp shuts off, breaking the feedback loop and freezing the voltages. Since the output remains at the overshoot point, the closed-loop gain is higher than $C_{\rm in}/C_F$. Fig. 4(b) repeats the simulation with a 300-mV input, revealing that the overshoot vanishes because of the open-loop gain reduction. In order to assess the robustness of this topology, Fig. 5 repeats the simulation results of Fig. 4(a), for the slow-slow 80°C and fast-fast 0°C corners. We observe that the closed-loop gain varied by about ±4%.

F. Comparison With Other Op Amps

The advantages of charge steering can be assessed in the MDAC environment of Fig. 6. Due to the large number of variables, we select certain design goals and evaluate the remaining aspects of the performance by transistor-level simulations in 65-nm technology. The design goals are: $V_{DD} = 1$ V, $P = 2$ mW, gain $= 10$, clock frequency $= 1$ GHz, differential output swing $= 0.6$ V, $C_{\rm in} = 480$ fF, $C_F = 240$ fF, and $C_L = 240$ fF.

We have considered two conventional op amps: a single-stage pair with current-source loads [Fig. 7(a)] and a two-stage topology [Fig. 7(b)][4]. For simplicity, large resistors are used to establish CM feedback. Table I summarizes the results, all obtained by transient simulations. We note that the charge-steering op amp outperforms (a) the one-stage topology with respect to signal-to-distortion ratio (SDR) and settling time, and (b) the two-stage op amp in terms of input noise and settling time. Note that a settling time equal to three time constants is considered because incomplete settling is corrected by calibration (Section IV).

The remarkable speed advantage of charge-steering op amps arises from their short duty cycle and hence the large supply current that they can afford to draw. In the above comparative example, this op amp draws a total peak current of 37 mA from the differential pairs, but allows it to drop to 1 mA in 150 ps.

The charge-steering op amp of Fig. 2(a) employs a pseudo-differential input pair, exhibiting some sensitivity to the input common-mode level. Also, it is difficult to define the output CM level by analog common-mode feedback. These issues are resolved at the ADC architecture level in Section III.

G. Modified Op Amp

The charge-steering op amp employed in the ADC includes three additional techniques. As shown in Fig. 8, two capacitors provide positive feedback around the first stage, thereby raising the equivalent open-loop gain. This increase in the gain is possible by virtue of the finite capacitive impedance driving the gates of M_1 and M_2, i.e., the MDAC capacitors $C_{\rm in}$ and C_F in Fig. 6. Note that such a method cannot be applied to continuous-time op amps.[5]

In order to appreciate the role of the C_M's in Fig. 8, let us consider only the first stage of the op amp and construct the equivalent circuit shown in Fig. 9, where C_D represents the driving capacitance and $\lambda = 0$ is for simplicity. Here, two instances of C_M account for positive feedback in a differential environment. We have

$$\frac{V_X}{V_{\rm in}}(s) = \frac{-(g_{m1,2} + C_M s)C_D}{(C_D C_X + C_M C_X + C_M C_D)s - g_{m1,2}C_M}. \tag{19}$$

With $C_M = 0$, on the other hand, $V_X/V_{\rm in}(s) = -g_m/(C_X s)$. Thus, C_M moves the first stage's pole from the origin to the *right-half plane*, creating an *exponential* growth rather than a ramp in response to a step input. In other words, during the amplification period, Δt, the first stage now provides a faster change in its output and hence a greater equivalent gain.[6]

The values shown in Fig. 8 correspond to the first MDAC stage. According to simulations, C_M's increase the open-loop gain from 10 to about 13 with negligible closed-loop speed and power penalty.

The second modification is the addition of the programmable tail resistor, R_M, in Fig. 8. This resistor allows fine adjustments in the output common-mode level and is set during calibration (Section IV).[7]

The third addition is the precharge of the tail nodes to V_{DD} so as to establish a well-defined initial voltage at these nodes. Without this precharge, the subthreshold currents of M_1–M_4 raise the tail voltages to ill-defined values, causing memory effects and interfering with full-speed calibration (Section IV).

[4]A switched op amp was also simulated but proved far inferior in terms of settling speed and distortion (due to memory effects)

[5]In a continuous-time op amp, the transient currents drawn by any capacitors around the first stage do not affect the final output of the stage.

[6]It can be proved that, if one of the two open-loop poles is located in the right-half plane, then so is one of the closed loop poles.

[7]The programmable resistor adjusts the CM level by 250 mV and, inevitably, the differential gain by 1.5%.

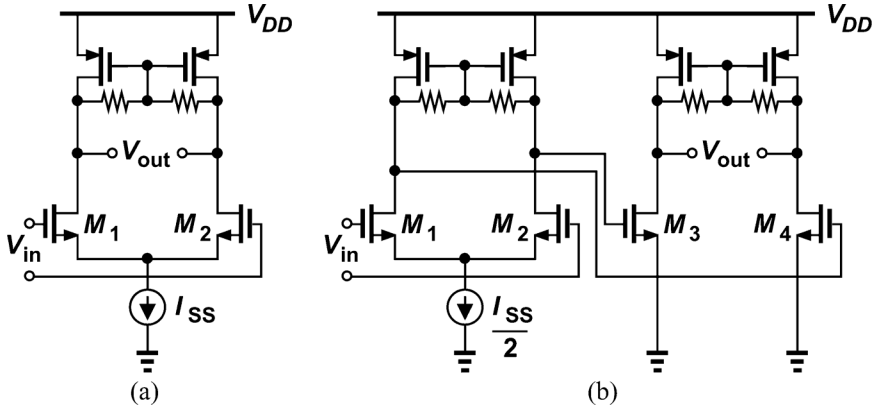

Fig. 7. Conventional (a) single-stage and (b) two-stage op amps.

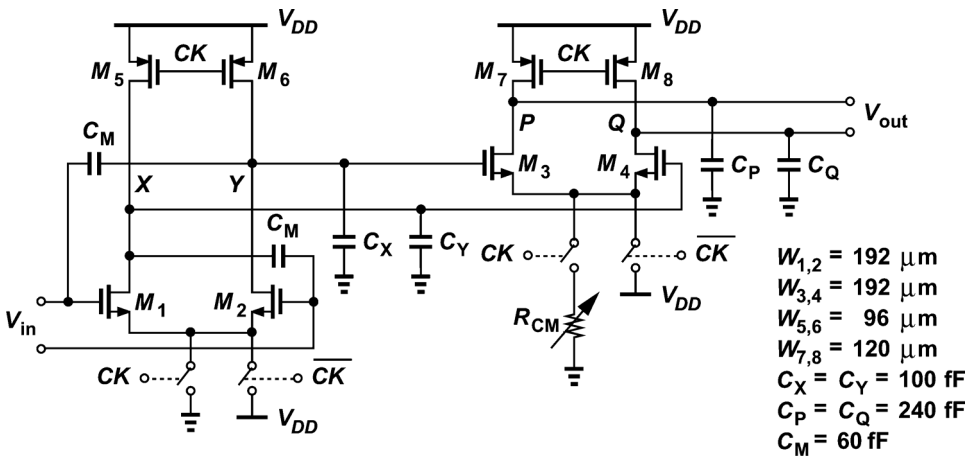

Fig. 8. Charge-steering amplifier used in first stage of ADC.

III. ADC Architecture

A. Choice of Stage Resolution

The pipelined ADC architecture employing charge-steering op amps is shown in Fig. 10. The first stage incorporates a "folded" 1.5-bit [16] topology while stages 2 through 12 are based on a conventional 1.5-bit configuration. All stages have a nominal residue gain of 2. The role of the digital back end is explained in Section IV. Using four comparators in its sub-ADC, the 1.5-bit folded stage exhibits the residue characteristic depicted in Fig. 11, where the folds at $V_{\rm in} = \pm 3V_{\rm REF}/4$ reduce the residue magnitude to $V_{\rm REF}/2$, and, therefore, relax the op amp linearity requirements. A higher sub-ADC resolution further exploits this trend, but the need for additional low-impedance references (e.g., $\pm V_{\rm REF}/8$, $\pm 3V_{\rm REF}/8$, etc.) and hence higher power dissipation outweigh the benefits. Also, in contrast to a standard 2-bit stage, our approach avoids reference values such as $\pm 3V_{\rm REF}/4$, thus operating with simple NMOS or PMOS switches rather than bootstrapped circuits. Table II summarizes these considerations.

TABLE I
Op Amp Comparison Summary

	One−Stage Op Amp	Two−Stage Op Amp	Charge−Steering Op Amp
SDR	48 dB	53 dB	54 dB
Input−Referred Noise	67 nV²	138 nV²	65 nV²
Settling Time (3τ)	560 ps	370 ps	80 ps

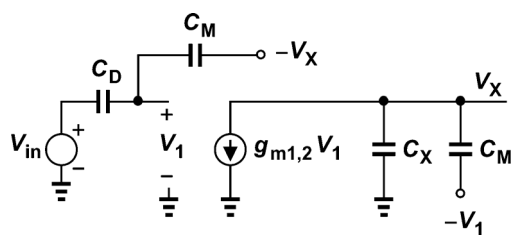

Fig. 9. Positive feedback in charge-steering amplifier.

B. Scaling Considerations

As with conventional pipelined ADCs, our design can benefit from scaling of the stages. With the stage resolutions and gains prescribed above, we must still consider various scaling scenarios so as to determine the optimal solution. We assume "linear" scaling, i.e., all of the op amp devices and the feedback network capacitors are scaled by the same factor. The principal issue is that "steep" scaling in a pipeline accumulates noise sharply and "gentle" scaling consumes substantial power. Thus,

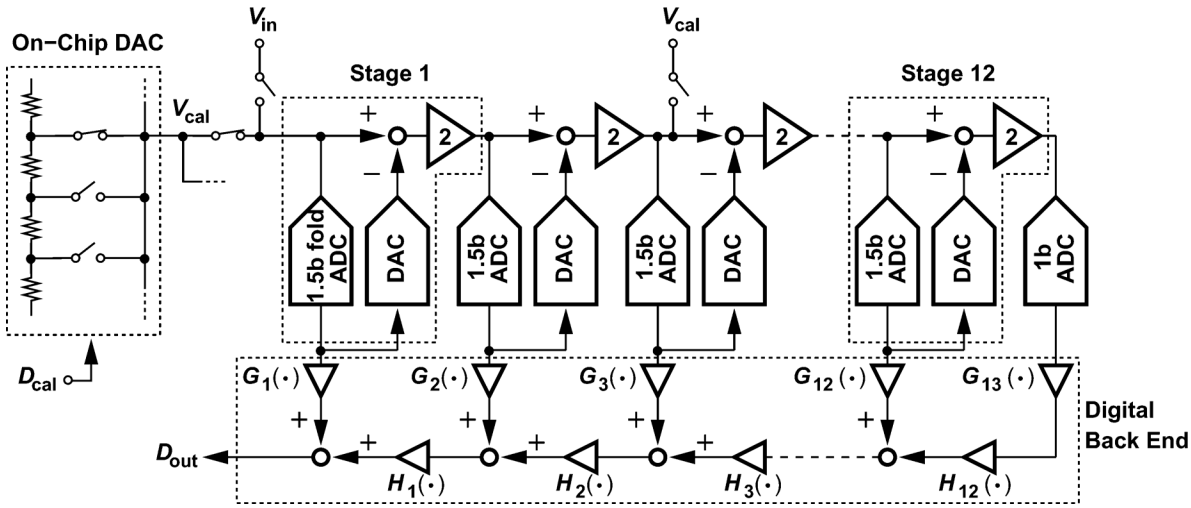

Fig. 10. ADC architecture.

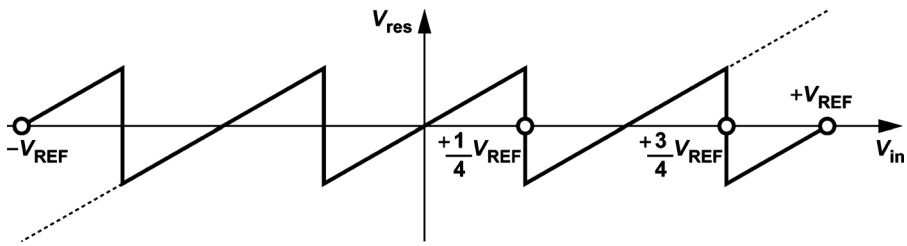

Fig. 11. Residue characteristics of conventional (dashed line) and folded 1.5-bit (solid line) topologies.

TABLE II
STAGE TOPOLOGY PARAMETERS AND COMPARISON

Stage Configuration	1.5−b	Folded 1.5−b	2−b
Stage Gain	2	2	2
Max. Output Swing ($\times \pm V_{REF}$)	1	$\frac{1}{2}$	$\frac{1}{2}$
MDAC References ($\times \pm V_{REF}$)	$0, \frac{1}{2}$	$0, \frac{1}{2}, 1$	$\frac{1}{4}, \frac{3}{4}$
Comparator References ($\times \pm V_{REF}$)	$\frac{1}{4}$	$\frac{1}{4}, \frac{3}{4}$	$0, \frac{1}{2}$

the ADC figure of merit (FoM) must reach a minimum for a certain scaling factor. For example, [17] assumes a given SNR and seeks the minimum power consumption.

Our study of scaling selects a certain transistor-level design—and hence a certain input capacitance—for the first stage and considers the following scenarios. (1) Scaling by a factor of S is applied to stages 2 to 5 and stops thereafter. (2) Stages 1 and 2 are identical, and scaling is applied to stages 3 to 6, stopping thereafter. (3) Stages 1 to 3 are identical, and scaling is applied to stages 4 to 7, stopping thereafter. We compute the power consumption and total input-referred noise of the pipeline in each case, translating the results to an equivalent FoM and SNR.

Fig. 12 illustrates the outcomes of this study. Fig. 12(a) indicates that the FoM reaches a minimum for $S \approx 0.25$ in the first two scenarios and for $S \approx 0.2$ in the third.[8] It also shows the benefit of scaling from the second stage. Fig. 12(b), on the other hand, reveals that the SNR steadily declines as the scaling becomes more aggressive, both in terms of the scaling factor and with respect to the stage number at which the scaling begins. Notably, at $S \approx 0.25$, the first scenario's SNR is about 4.5 dB short of the 10-bit goal even though providing the lowest FoM. We have chosen $S = 0.5$ and the first scenario in our ADC.

IV. FOREGROUND CALIBRATION

For 10-bit resolution, the pipelined ADC requires gain calibration to correct for the errors due to capacitor mismatches

[8]Since the FoM favors low SNR designs, the optimal point here is at a lower scaling factor than that found in [17], where *power* is plotted as a function of the scaling factor for a fixed SNR

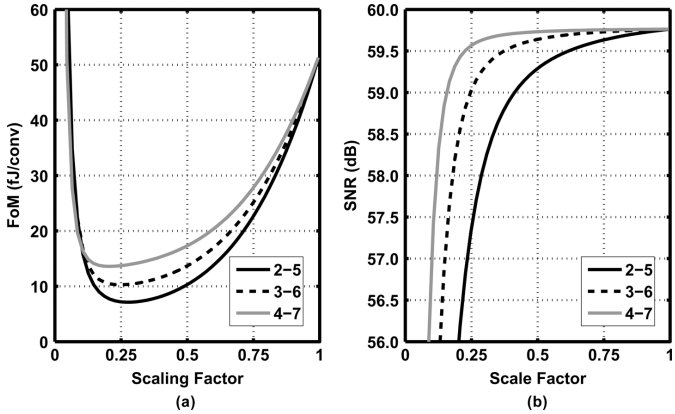

Fig. 12. (a) FoM vs. stage scaling factor, (b) SNR vs. stage scaling factor. (The notation, e.g., 2-5 means stages 2 through 5 are scaled.)

and the low op amp gain, and linearity calibration to suppress the effect of op amp nonlinearity. Previous work [4], [6] suggests that a particular on-chip resistor ladder structure exhibits a linearity of about 12 bits and can serve as a high-precision DAC to calibrate the ADC. The digital calibration back end in Fig. 10 implements the inverse function of each pipelined stage by gain correction factors, G_j, and third-order polynomials, H_j. The idea is to apply "golden" voltages using the DAC and adjust the coefficient within the G and H blocks so as to minimize $|D_{\rm out} - D_{\rm cal}|$ [4]. The calibration begins by applying the DAC output to the last stage and moves toward the front end, utilizing an LMS algorithm to set the coefficients. In principle, one can calibrate the entire chain as one entity, but with a large number of equations to solve so as to compute the β and α coefficients for all of the inverse functions. While possible, such an approach proves more complex and may face convergence issues.

A. CM Issues

As mentioned in Section II, the pseudo-differential input pair of the op amp makes the open-loop characteristics somewhat sensitive to the input CM level, posing a challenge in calibration if 10-bit linearity must be achieved with an open-loop gain of about 13. Specifically, if the second stage of the pipeline receives different CM levels from the DAC during calibration and from the first stage during regular operation, then the digital back-end coefficients are not optimally set.

The foregoing issue is avoided by treating the first and second pipelined stages as *one* block and adjusting their G and H coefficients simultaneously. The second stage is thus always driven by and its coefficients are tailored for the output CM level of the first stage.[9]

In order to define the output CM level of each op amp, a programmable tail resistor finely adjusts the total charge drawn by the second stage from its load capacitors (Fig. 8). To accommodate maximum output voltage swings with acceptable distortion, the op amp design must establish an output CM level around $V_{DD}/2$. Since the CM level upon power-up to some extent depends on the process, $R_{\rm CM}$ can be programmed to shift the CM value by about 250 mV. However, this CM level proves difficult to sense because, in contrast to that of continuous-time op amps, it is raised to V_{DD} and then released in every cycle. The output CM level settles only near the end of the amplification phase, by which time both stages are off and hence incapable of making CM adjustments. Fortunately, it is possible to see the *consequences* of a non-optimal CM level by examining the cost function, $|D_{\rm out} - D_{\rm cal}|$, as the op amp gain reduction eventually manifests itself in the residual error after calibration. Note that the CM levels are not measured directly and are automatically adjusted along with the α and β coefficients by the LMS machine. From another perspective, if we adjust the output CM level of each op amp during calibration, then $|D_{\rm out} - D_{\rm cal}|$ can come closer to zero (provided, of course, that the LMS algorithm converges).

The above observation leads to the "mixed-signal" output CM feedback shown in Fig. 13. In addition to the α and β coefficients, the LMS machine also adjusts the value of $R_{\rm CM}$ within each op amp, thereby establishing the optimum CM level after the LMS loop settles. The tail resistor is programmable in 16 steps. The calibration sweeps the 16 values of $R_{\rm CM}$ in one stage at a time, selecting the step that corresponds to minimum error (For the first and second stages, $R_{\rm CM}$ is adjusted in both simultaneously).[10]

B. Full-Rate Calibration

Dynamic errors such as incomplete op amp settling and reference voltage ringing make it desirable to perform the ADC calibration at the full clock rate. However, the output resistance of the calibration DAC and the input capacitance of the first stage create a long time constant, on the order of 100 ps. We introduce a technique here that affords full-rate calibration while utilizing a slow ladder.

Illustrated conceptually in Fig. 14(a), the idea is to allow a sufficiently long time for the *acquisition* of the DAC voltage but confine the residue generation to half of the clock cycle. At the end of this half cycle, the residue is sampled by the remainder of the pipeline and digitized, capturing dynamic effects.

In order to realize the timing shown in Fig. 14(a), we gate the main clock by a sub-multiple of its frequency, in this case by $f_{CK}/16$. As depicted in Fig. 14(b), the MDAC senses $V_{\rm cal}$ for 16 clock cycles and, at t_1, begins to compute the difference between $V_{\rm cal}$ and $KV_{\rm REF}$. The entire foreground calibration requires approximately 3.3e6 cycles or 4.1 ms during startup.

V. Background Calibration

The gain and nonlinearity of op amps drift to some extent with temperature and supply variations, calling for fine background calibration after foreground calibration is completed. Among various background calibration techniques reported for pipelined ADCs [1], [3], [18], [19], that described in [21] is particularly attractive as it simply utilizes the nonidealities in the output histogram to measure circuit imperfections and set the calibration coefficients. However, this technique adjusts only

[9]To avoid significant input CM variations during calibration and main operation, we assume that the analog input to the ADC is ac-coupled, and its CM level is forced to be equal to that of the calibration ladder. Starting in the third stage, the op amp uses fully-differential sampling to reject the input common-mode [20]. The fully-differential topology incurs a power penalty and hence was avoided in the most power-hungry first and second stages.

[10]According to simulations, a 10-mVpp 10-MHz sinusoidal noise on the supply degrades the signal-to-distortion ratio by 1 dB.

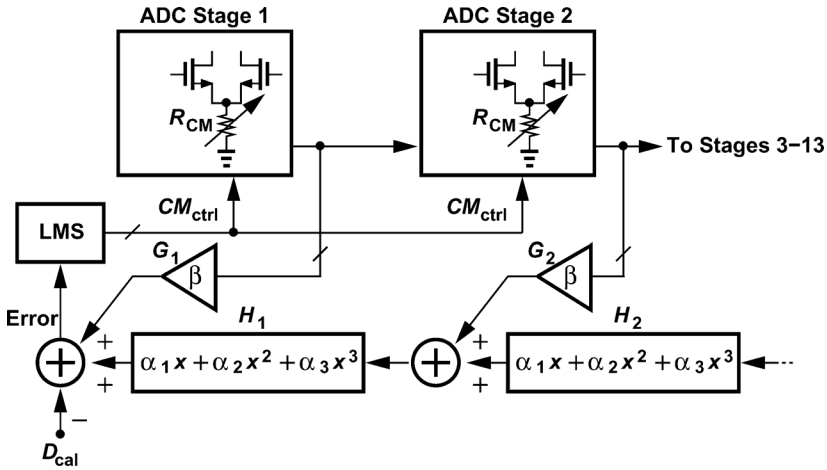

Fig. 13. Mixed-signal common-mode feedback.

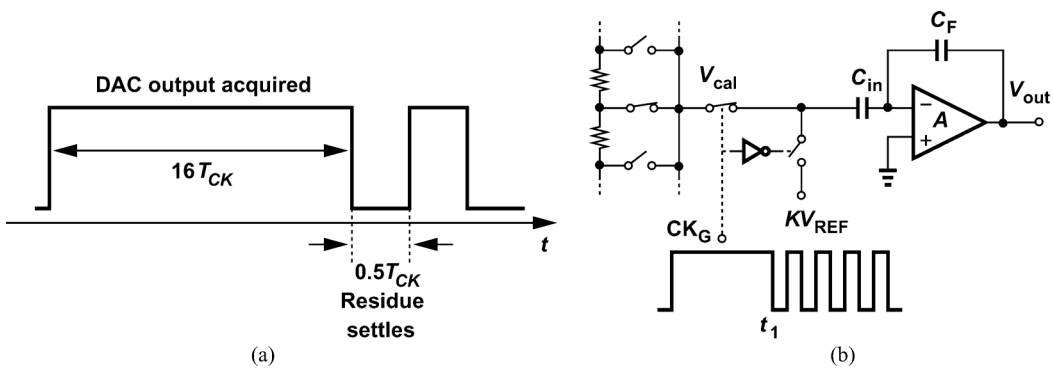

Fig. 14. Full-rate calibration: (a) gated clock waveform, and (b) MDAC switch control.

one type of error, proving insufficient for our ADC. As explained below, we propose to adjust two types of error so as to achieve 10-bit resolution in the presence of drifts in op amp characteristics. We should also point out that the work in [21] is solely based on simulations, with a minimum op amp gain of 243, and has not been applied to an actual op-amp-based ADC prototype. The technique may thus face issues if such imperfections as op amp nonlinearity and reference ringing are considered.

A. Effect of Stage Nonidealities on Histogram

The transfer characteristic of a pipelined stage can be expressed as $V_{\rm res} = (A + \Delta A)[V_{\rm in} - K(1 + \epsilon)V_{\rm REF}]$, where A denotes the nominal residue gain, ΔA is the residue gain error, K is the sub-ADC digital output, and ϵ is the DAC gain error. The work in [21] adjusts ϵ (or, equivalently, K) but not ΔA. Note that, in the absence of op amp nonlinearity, coefficients β and α_1 in Fig. 13 are the same as $K(1 + \epsilon)$ and the inverse of $A + \Delta A$, respectively.

An ideal 1.5-bit/stage pipelined ADC sensing a uniformly-distributed analog input exhibits the residue characteristic and output histogram shown in Fig. 15(a). The three residue regions translate to three distinct blocks in the histogram. We denote the width of the middle block by W. We wish to determine how the histogram is distorted if ΔA or ϵ is not zero.

If $\Delta A < 0$ and $\epsilon = 0$, the residue fails to reach its ideal extrema [Fig. 15(b)], creating missing codes in the digital output and hence gaps in the histogram. To determine the relationship between ΔA and the width of each block, we consider the close-up shown in Fig. 15(c) and examine the results for two input values, V_1 and V_2, very close to $-V_{\rm REF}/4$. At $V_{\rm in} = V_1$, the actual residue reaches its peak, leading to a final ADC output of D_1. Since all of the codes between D_1 and $D_{\rm max}$ are missing, the histogram displays empty bins as $D_{\rm out}$ exceeds D_1. Similarly, at $V_{\rm in} = V_2$, the actual residue yields a final digital output of D_2 and missing codes between $D_{\rm min}$ and D_2. The second histogram block thus begins at $D_{\rm out} = D_2$. Note that the width of the middle histogram block varies with ΔA.

If $\Delta A > 0$ and $\epsilon = 0$, then the residue and the histogram behave as shown in Fig. 15(d). Due to the nonmonotonicity in the input-output characteristic of the overall ADC around $\pm V_{\rm REF}/4$, some codes repeat, thus creating two peaks in the histogram.

Let us now repeat the above analysis for $\Delta A = 0$ but $\epsilon < 0$ or $\epsilon > 0$. As illustrated in Fig. 16, based on the final ADC outputs, we observe gaps or peaks from D_1 to D_2 and from D_3 to D_4. In this case, the width of the middle histogram block is independent of ϵ.

The key point emerging from these studies is that, while both residue gain error and DAC gain error produce missing or repeated codes, only the former alters the width of the histogram's middle block—a critical property exploited in our work.

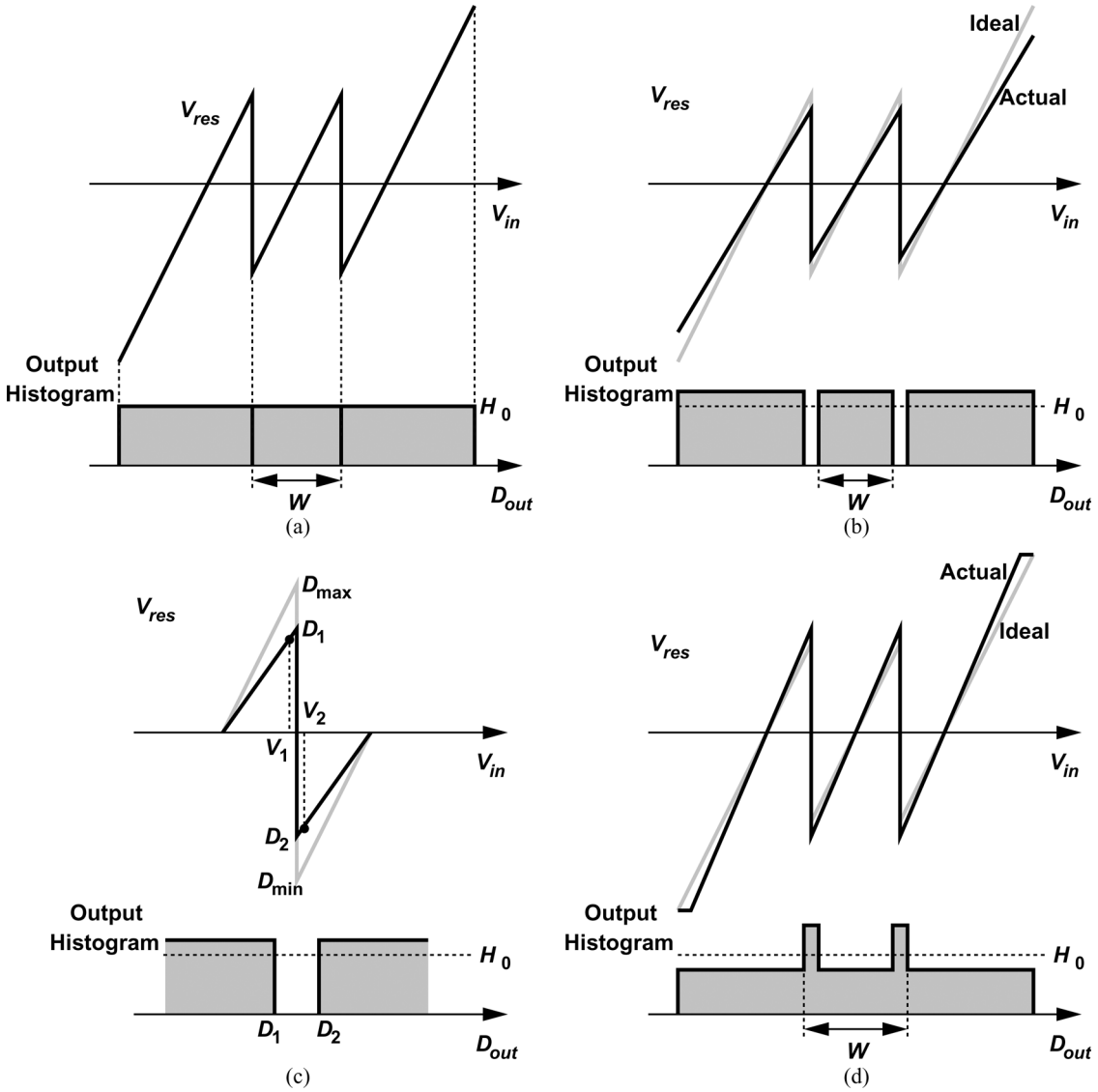

Fig. 15. ADC stage transfer characteristic and histogram with $\epsilon = 0$: (a) ideal, (b) $\Delta A < 0$, (c) close-up view, and (d) $\Delta A > 0$.

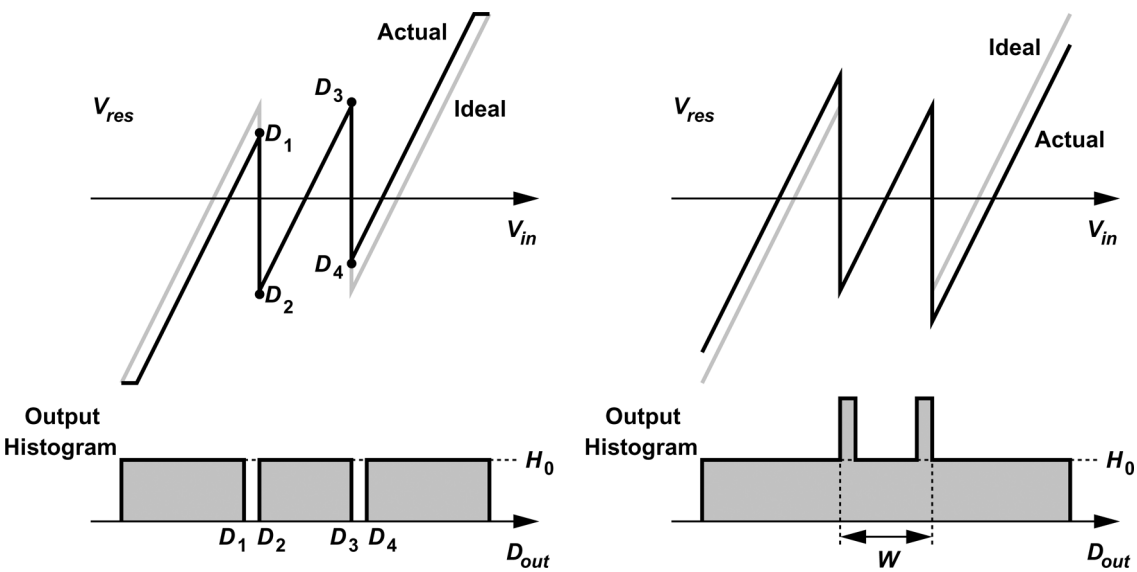

Fig. 16. ADC stage transfer characteristic and histogram with DAC gain error.

B. Proposed Algorithm

The foregoing analysis reveals that it is difficult to isolate the individual contributions of the residue and DAC gain errors by examining the missing or repeated codes. However, one can measure *changes* in the residue gain error, ΔA, by monitoring the width of the middle histogram block. Thus, upon completion of foreground calibration, this width, W, can be memorized and its variation thereafter can serve as an error signal signifying drifts in ΔA.

Our algorithm computes W as follows. As the histogram accumulates, we count how often a given digital output code is produced by each region in the residue characteristic. For example, in Fig. 15(c), the codes slightly above D_2 arise only from $-V_{\rm REF}/4 < V_{\rm in} < +V_{\rm REF}/4$ whereas in Fig. 15(d), the codes within the first peak come from both $-V_{\rm REF}/4 < V_{\rm in} < +V_{\rm REF}/4$ and $V_{\rm in} < -V_{\rm REF}/4$. We then consider only the output codes contributed by the middle residue region, $-V_{\rm REF}/4 < V_{\rm in} < +V_{\rm REF}/4$, computing the lower and upper edges of W as the minimum and maximum output codes contributed by this region, respectively. Such a procedure applies to both $\Delta A < 0$ and $\Delta A > 0$.

The background calibration algorithm begins by storing W for each stage at the end of foreground calibration as a reference. As W drifts, the algorithm adjusts the α_1 coefficients in Fig. 13 so as to restore W to its reference value. After this update, the calibration adjusts the β coefficients, aiming to remove the gaps or peaks in the histogram. As with foreground calibration, this procedure begins from the back-end stages and progresses toward the front end.

The proposed background calibration technique is generally applicable to pipelined ADCs and resides entirely in the digital domain, obviating the need for additional analog complexities such as injection of a random signal [1], [3], [18], a second slow-but-accurate ADC [19], etc. Moreover, in the presence of low op amp gain, high op amp nonlinearity, and possibly reference ringing, our technique leads to a lower integral nonlinearity (INL) than that described by [21] as experimentally demonstrated in Section VI.

As with other histogram-based calibration techniques [1], [21], the proposed method does make some assumptions: (1) the signal sensed by the ADC continually exercises the codes in the vicinity of the residue boundaries; (2) the drift in op amp nonlinearity, op amp offset, and sub-ADC decision thresholds is negligible. Fig. 17 plots the simulated INL profile of the first two stages before and after a temperature change from 27 to 60°C. Arising from the change in the DAC gain, the jumps account for most of the error. It can also be shown that when the supply is varied, the closed-loop linear gain error dominates the INL. Thus, background calibration need only correct the linear gain terms.

VI. Experimental Results

The ADC has been fabricated in TSMC's 65-nm CMOS technology. The die micrograph is shown in Fig. 18; the active area, including the high-precision ladder, measures $720\,\mu\text{m} \times 250\,\mu\text{m}$. The chip is directly mounted on a printed-circuit board and tested with a 1-V supply. The output

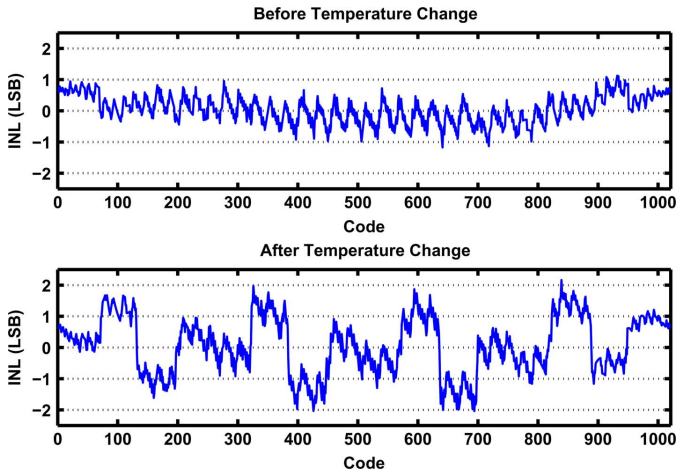

Fig. 17. Simulated integral nonlinearity before and after temperature change.

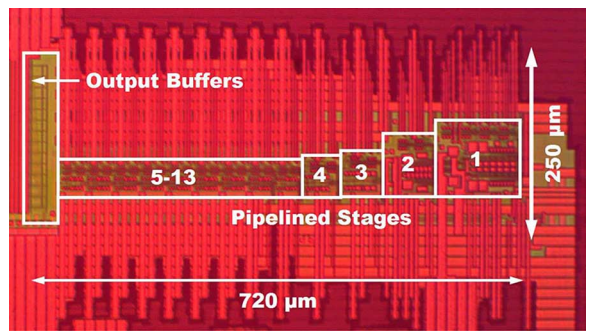

Fig. 18. Die micrograph.

is downsampled by a factor of 243 and digital calibration is performed off-chip. Unless stated otherwise, all measurement results are reported for a sampling rate of 800 MHz. At this rate, the ADC consumes 19 mW, of which 6.2 mW is drawn by the analog section, 11.1 mW by the digital section,[11] and 1.4 mW by the references. Note that the ADC incorporates no continuous-time biasing,[12] drawing power in proportion to the clock frequency.

A. Foreground Calibration

Figs. 19 and 20, respectively, plot the measured differential nonlinearity (DNL) and integral nonlinearity before and after foreground calibration. The peak DNL falls from 2.9 LSB to 0.9 LSB and the peak INL from 11 LSB to 1.8 LSB. Fig. 21(a) and (b) shows the measured output spectrum with input frequencies of 9.8 MHz and 399.2 MHz, respectively; the SNDR reaches 54.8 dB in the former case and 52.2 dB in the latter. Fig. 22 plots the measured SNDR as a function of the input frequency. The ADC achieves an FoM of 53 fJ/conversion-step at low input frequencies and 71 fJ/conversion-step at the Nyquist rate.

The board-level interleaved channels have been tested with an overall sampling rate of 1 GHz (500 MHz per channel). In this case, the SNDR reaches 56.9 dB at 9.3 MHz and 52.3 dB at 491 MHz. The total power consumption is 22.8 mW, yielding

[11]Excludes the off-chip digital calibration power.

[12]The resistor ladder is turned off after foreground calibration.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	Zhu12	Mulder11	Hashemi12	Sahoo12	This Work	
Sampling Rate	500 MHz	800 MHz	1000 MHz	1000 MHz	800 MHz	1000 MHz
Power	8.2 mW	105 mW	36 mW	33 mW	19 mW	22.8 mW
SNDR @ Nyq.	52.9 dB	59.0 dB	52.7 dB	52.4 dB	52.2 dB	52.3 dB
FoM@DC (fJ/conv−step)	34	180	70	93	53	40
FoM@Nyq (fJ/conv−step)	45	180	102	97	71	68
Resolution	10 b	12 b	10 b	10 b	10 b	10 b
Area (mm^2)	0.046	0.880	0.175	0.225	0.180	0.360
Supply	1.2 V	1.0 / 2.5 V	1.2 V	NA	1.0 V	1.0/0.9 V
Technology	65 nm	40 nm	65 nm	65 nm	65 nm	65 nm

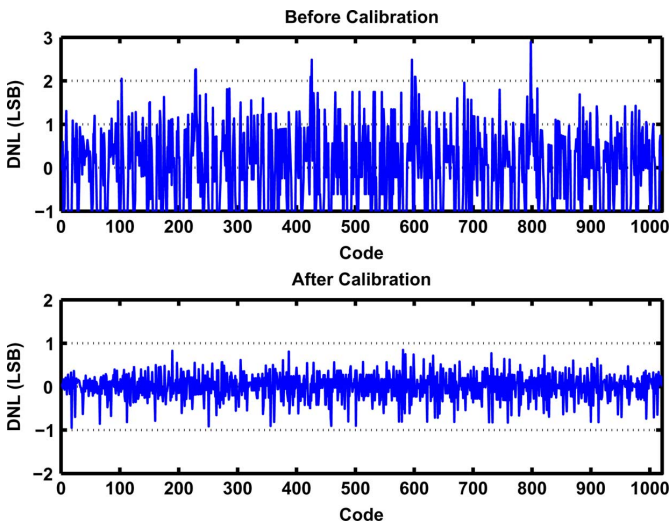

Fig. 19. Differential nonlinearity before and after calibration.

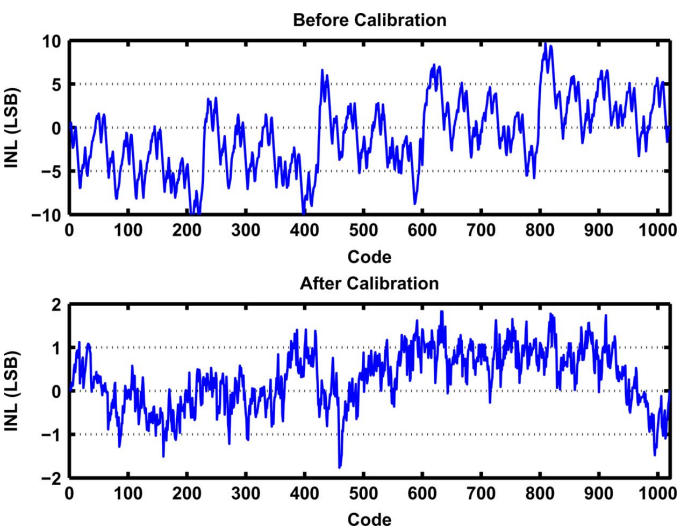

Fig. 20. Integral nonlinearity before and after calibration.

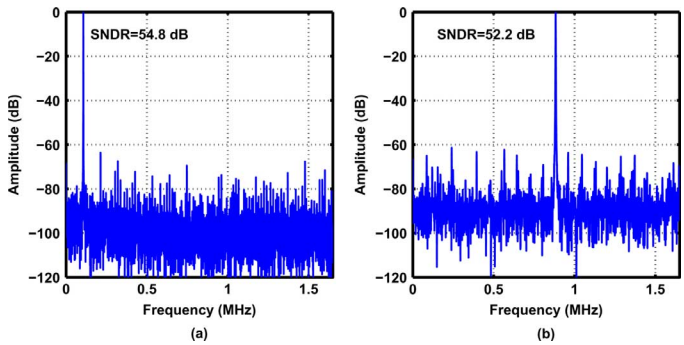

Fig. 21. Output spectrum for $f_s = 800$ MHz and (a) $f_{\rm in} = 9.8$ MHz, (b) $f_{\rm in} = 399.2$ MHz.

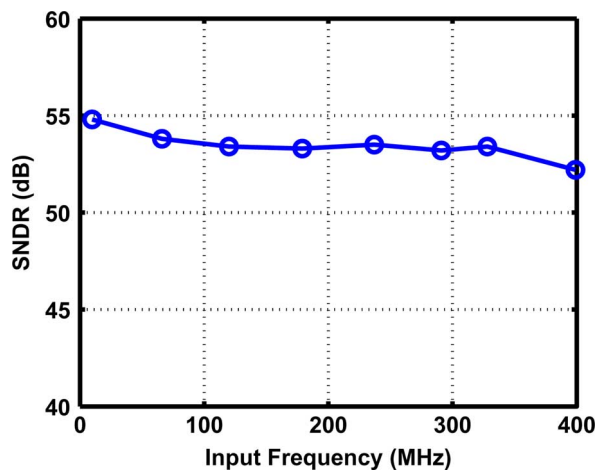

Fig. 22. Measured SNDR as a function of the input frequency with $f_s = 800$ MHz.

low-frequency and Nyquist-rate FoMs of 40 and 68 fJ/conversion-step, respectively.

Table III summarizes the performance of our single-channel and interleaved prototypes and recent ADCs with a resolution of 10 to 12 bits and a sampling rate of 500 to 1000 MHz.

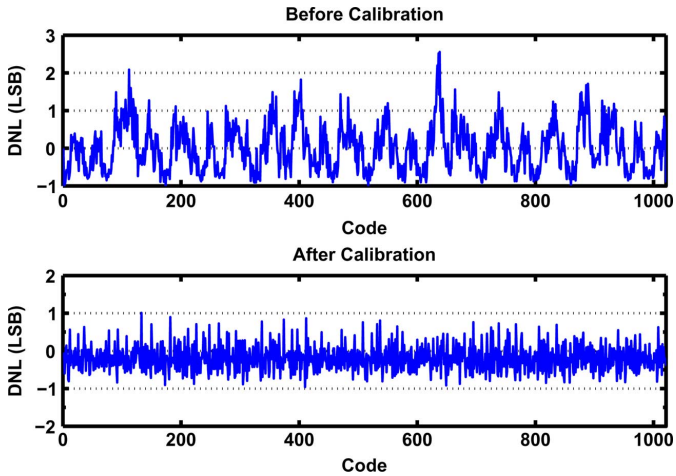

Fig. 23. Differential nonlinearity before and after background calibration.

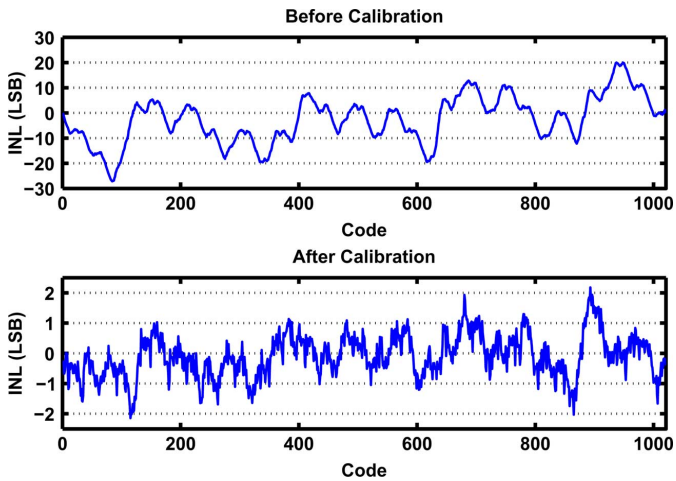

Fig. 24. Integral nonlinearity before and after background calibration.

B. Background Calibration

We assess the proposed background calibration technique as follows. After foreground calibration is completed and the ADC enters regular operation, the supply voltage is raised from 1 V to 1.1 V. Next, background calibration is enabled and the digital back-end coefficients are updated based on 2^{15} samples with a full-scale sinusoidal input.[13]

Figs. 23 and 24 respectively plot the DNL and INL before and after background calibration[14], indicating good performance and hence negligible change in the op amp nonlinearity. For comparison, if, as described in [21], only the DAC gain error is adjusted, then the results shown in Fig. 25 are obtained. The more accurate correction provided by our proposed technique can be attributed to the extra degree of freedom afforded by *two* variables, α_1 and β, and the ability to approximate the inverse function more closely.

[13]Since the PDF of a sinusoid is smooth and continuous near the comparator thresholds, the background calibration is able to correctly identify the region boundaries.

[14]The INL degradation with the supply indicates supply sensitivity and hence the need for background calibration to deal with supply drifts.

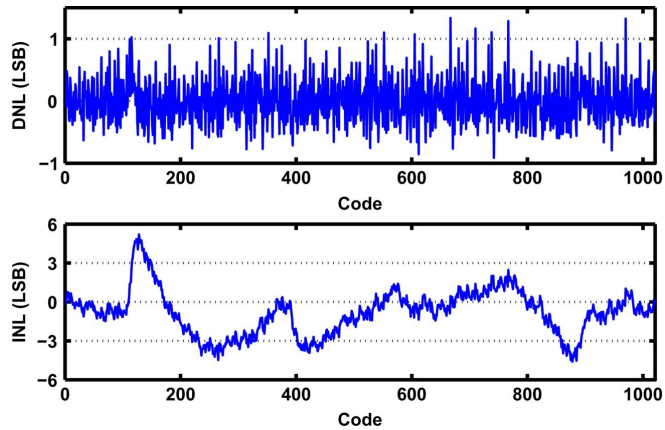

Fig. 25. Differential and integral nonlinearity after background calibration using [21].

VII. Conclusion

Charge-steering op amps hold promise for high-speed analog and mixed-signal systems, presenting a "raw" performance superior to their continuous-time counterparts. These op amps also lend themselves to calibration in ADCs and can provide relatively high resolutions. The closed-loop behavior of these op amps goes against traditional stability concerns, and their power consumption scales with frequency.

A 10-bit pipelined ADC employing charge-steering op amps has been designed in 65-nm CMOS technology. With the aid of calibration, the prototype achieves low-frequency and Nyquist-rate FoMs of 53 and 71 fJ/conversion-step, respectively, while sampling at 800 MHz.

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References

[1] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[2] A. Panigada and I. Galton, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.

[3] B. N. Fang and J. T. Wu, "A 10-bit 300-MS/s pipelined ADC with digital calibration and digital bias generation," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 670–683, Mar. 2013.

[4] A. Verma and B. Razavi, "A 10-Bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.

[5] B. Sahoo and B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1442–1452, Jun. 2013.

[6] S. Hashemi and B. Razavi, "A 10-bit 1-GS/s CMOS ADC with FOM = 70 fJ/conversion," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2012.

[7] S. W. Chiang, H. Sun, and B. Razavi, "A 10-bit 800-MHz 19-mW CMOS ADC," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2013.

[8] J. W. Jung and B. Razavi, "A 25-Gb/s 5-mW CMOS CDR/deserializer," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 684–697, Mar. 2013.

[9] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2x interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 466–468.

[10] B. Verbruggen *et al.*, "A 2.6 mW 6b 2.2 GS/s 4-times interleaved fully dynamic pipelined ADC in 40 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 296–297.
[11] J. Lin *et al.*, "A 0.55 V 7-bit 160 MS/s interpolated pipeline ADC using dynamic amplifiers," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2013.
[12] D. Schinkel *et al.*, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 314–605.
[13] M. Miyahara *et al.*, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2008, pp. 269–272.
[14] P. Nuzzo *et al.*, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.
[15] B. Oksendal, *Stochastic Differential Equations*. New York, NY, USA: Springer-Verlag, 1992.
[16] O. Stroeble, V. Dias, and C. Schwoerer, "An 80 MHz 10b pipeline ADC with dynamic range doubling and dynamic reference selection," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 462–539.
[17] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, Mar. 1996.
[18] Z. M. Lee, C. Y. Wang, and J. T. Wu, "A CMOS 15-bit 125-MS/s time-interleaved ADC with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2149–2160, Oct. 2007.
[19] H. Wang *et al.*, "Nested digital background calibration of a 12-bit pipelined ADC without an input SHA," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2780–2789, Oct. 2009.
[20] J. Brunsilius *et al.*, "A 16b 80 MS/s 100 mW 77.6 dB SNR CMOS pipeline ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 186–187.
[21] L. Brooks and H. S. Lee, "Background calibration of pipelined ADCs via decision boundary gap estimation," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 11, pp. 2969–2979, Nov. 2008.
[22] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
[23] S. M. Jamal *et al.*, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.

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