Stacked Inductors and Transformers in CMOS Technology

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***Abstract*—A modification of stacked spiral inductors increases the self-resonance frequency by 100% with no additional processing steps, yielding values of 5 to 266 nH and self-resonance frequencies of 11.2 to 0.5 GHz. Closed-form expressions predicting the self-resonance frequency with less than 5% error have also been developed. Stacked transformers are also introduced that achieve voltage gains of 1.8 to 3 at multigigahertz frequencies. The structures have been fabricated in standard digital CMOS technologies with four and five metal layers.**

***Index Terms*—Inductors, oscillators, quality factor, RF circuits, self-resonance frequency, stacked spirals, transformers, tuned amplifiers.**

I. Introduction

MONOLITHIC inductors have found extensive usage in RF CMOS circuits. Despite their relatively low quality factor (Q) such inductors still prove useful in providing gain with minimal voltage headroom and operating as resonators in oscillators. Monolithic transformers have also appeared in CMOS technology [1], allowing new circuit configurations.

This paper introduces a modification of stacked inductors that increases the self-resonance frequency $f_{\rm SR}$ by as much as 100%, a result predicted by a closed-form expression that has been developed for $f_{\rm SR}$. Structures built in several generations of standard digital CMOS technologies exhibit substantial reduction of the parasitic capacitance with the technique applied, achieving self-resonance frequencies exceeding 10 GHz for values as high as 5 nH. The modification allows increasingly larger inductance values or higher self-resonance as the number of metal layers increases in each new generation of the technology.

The paper also presents a new stacked transformer that achieves nominal voltage or current gains from 2 to 4. Fabricated prototypes display voltage gains as high as 3 in the gigahertz range, encouraging new circuit topologies for low-voltage operation.

Section II reviews the definitions of Q. Section III provides the motivation for high-value inductors and summarizes the properties of stacked inductors. Section IV deals with the theoretical derivation of the self-resonance frequency of such inductors and Section V exploits the results to propose the modification. Section VI presents the stacked transformers and describes a distributed circuit model used to analyze their behavior. Section VII summarizes the experimental results.

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II. Definitions of the Quality Factor

Several definitions have been proposed for the quality factor. Among these, the most fundamental is

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}}. \tag{1}$$

The above definition does not specify what stores or dissipates the energy. However, for an inductor, only the energy stored in the magnetic field is of interest. Therefore, the energy stored is equal to the difference between peak magnetic and electric energies.

If an inductor is modeled by a simple parallel *RLC* tank, it can be shown that [2]

$$\begin{aligned} Q &= 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} \\ &= \frac{R_p}{L\omega} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] \\ &= \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \end{aligned} \tag{2}$$

where R_p and L are the equivalent parallel resistance and inductance, respectively, ω_0 is the resonance frequency, and Z is the impedance seen at one terminal of the inductor while the other is grounded. Although definition (2) has been extensively used, it is only applicable to the frequencies below the resonance because it falls to zero at the self-resonance frequency.

On the other hand, if only the magnetic energy is considered, then (1) reduces to

$$\begin{aligned} Q &= 2\pi \cdot \frac{\text{peak magnetic energy}}{\text{energy loss in one oscillation cycle}} \\ &= \frac{R_p}{L\omega}. \end{aligned} \tag{3}$$

Definition (3) has two advantages over (2). First, it can be used over a wider frequency range. Second, it can more explicitly express R_p. It should be noted that at low frequencies, the Q's obtained by (2) and (3) are quite close because the energy stored in the electric field is much smaller than that stored in the magnetic field.

III. Large Inductors with High Self-Resonance Frequencies

Inductors are extensively used in tuned amplifiers and mixers with high intermediate frequencies (IFs) (Fig. 1). In these applications, to maximize the gain (or conversion gain), the equiva-

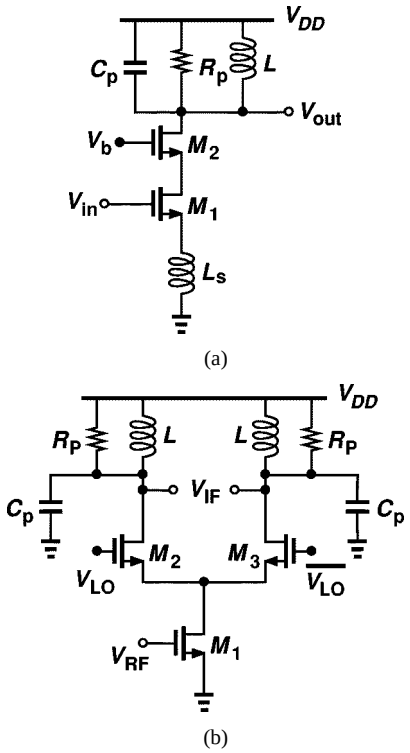

Fig. 1. (a) Low-noise amplifier and (b) mixer with high IF.

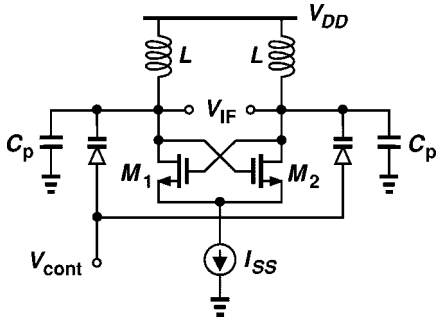

Fig. 2. Representative VCO.

lent parallel resistance of the inductor (R_p) must be maximized. From definition (3) of the Q, R_p can be expressed as

$$R_p = Q \cdot L\omega. \tag{4}$$

Therefore, to maximize R_p, the *product* of Q and L must be maximized. Since the Q of on-chip inductors in CMOS technology is quite limited, it is reasonable to seek methods of achieving high inductance values with high self-resonance frequencies and a moderate silicon area.

If a method of reducing the parasitic capacitance C_p of inductors is devised, it also improves the performance of voltage-controlled oscillators (VCOs). In the topology of Fig. 2, for example, reduction of C_p directly translates to a wider tuning range because the varactor diodes can contribute more variable capacitance. Simulations indicate that the inductor modification introduced in this paper increases the tuning range of a 900-MHz CMOS VCO from 4.2% to 23% for a 2× varactor capacitance range.

A candidate for compact high-value inductors is the stacked structure of Fig. 3, originally introduced in GaAs technology [3]

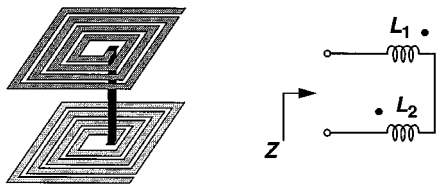

Fig. 3. Two-layer inductor.

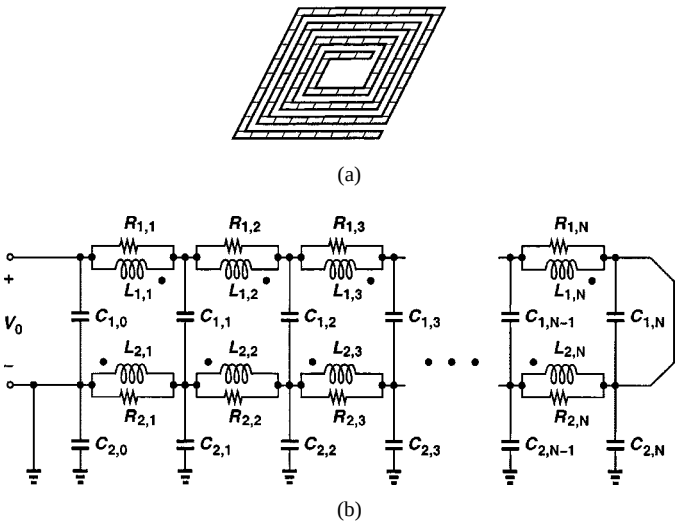

Fig. 4. (a) Decomposing a spiral into equal sections. (b) Distributed model of a two-layer inductor.

and later used in CMOS technology as well [4]. From the circuit model of Fig. 3, it can be seen that the input impedance of this structure is

$$Z = j\omega(L_1 + L_2 + 2M) \tag{5}$$

where L_1 and L_2 are the self-inductance of the spirals and M is the mutual inductance between the two. In a stacked inductor, the two spirals are identical ($L_1 = L_2 = L$) and the mutual coupling between the two layers is quite strong ($M \approx \sqrt{L_1 L_2} = L$). The total inductance is therefore increased by nearly a factor of 4. Similarly, for an n-layer inductor the total inductance is nominally equal to n^2 times that of one spiral. With the availability of more than five metal layers in modern CMOS technologies, stacking can provide increasingly larger values in a small area.

IV. Derivation of Self-Resonance Frequency

Stacked structures typically exhibit a single resonance frequency. Thus, they can be modeled by a lumped *RLC* tank with $f_{\rm SR} = (2\pi\sqrt{L_{eq}C_{eq}})^{-1}$, where L_{eq} and C_{eq} are the equivalent inductance and capacitance of the structure, respectively. While the equivalent inductance can be obtained by various empirical expressions [5], [6], Greenhouse's method [7], or electromagnetic field solvers [8], no method has been proposed to calculate the equivalent capacitance. We derive an expression for the capacitance in this section.

For $f_{\rm SR}$ calculations, we decompose each spiral into equal sections as shown in Fig. 4(a) such that all sections have the same inductance and parasitic capacitance to the substrate or the other spiral. This decomposition yields the distributed model illustrated in Fig. 4(b). In this circuit, inductive elements $L_{i,j}$'s

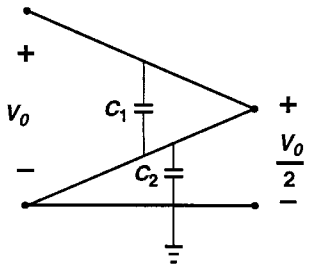

Fig. 5. Voltage profile across each capacitor.

represent the inductance of each section in Fig. 4(a) and they are all mutually coupled. The capacitance between the two layers is modeled by capacitors $C_{1,j}$ and that between the bottom layer and the substrate by capacitors $C_{2,j}$. To include the finite Q of the structure, all sources of loss are lumped into parallel resistor elements $R_{i,j}$. Also, we neglect trace-to-trace capacitances of each spiral. The validity of these assumptions will be explained later.

The simple circuit model of Fig. 4(b) still does not easily lend itself to current and voltage equations. However, we can use the physical definition of resonance. The resonance frequency can be viewed as the frequency at which the peak magnetic and electric energies are equal. In other words, if we calculate the total electric energy stored in the structure for a given peak voltage V_0 and equate that to $C_{eq}V_0^2/2$, then we can obtain C_{eq}.

To derive the electric energy stored in the capacitors, we first compute the voltage profile across the uniformly distributed capacitance of the structure. Assuming perfect coupling between every two inductors in Fig. 4, we express the voltage across each as

$$V_{L,l,m} = \sum_{k=1}^{2}\sum_{n=1}^{N} j\omega I_{k,n}L_{k,n}, \tag{6}$$

where $I_{l,m}$ is the current through $L_{l,m}$ and N is the number of the sections in the distributed model. Equation (6) reveals that all inductors sustain *equal* voltages. Therefore, for a given applied voltage V_0, we have

$$V_{L,l,m} = \frac{V_0}{2N}. \tag{7}$$

From (6) and (7), it follows that the voltage varies linearly from V_0 to 0 across the distributed capacitance C_1 and from 0 to $V_0/2$ across C_2 (from left to right in Fig. 5).

Having determined the voltage variation, we write the electric energy stored in the mth element, $C_{1,m}$, as

$$E_{e,C_{1,m}} = \tfrac{1}{2}\,C_{1,m}[(V_0 - mV_{L,l,m}) - mV_{L,l,m}]^2. \tag{8}$$

The total electric energy in C_1 is therefore equal to

$$E_{e,C_1} = \tfrac{1}{2}\sum_{m=0}^{N} C_{1,m}(V_0 - 2mV_{L,l,m})^2. \tag{9}$$

As mentioned earlier, all sections are identical, i.e., $C_{1,m} = C_1/(N+1)$, and if we substitute (7) in (9), define a new variable $x = m/N$, and let N go to infinity, then we obtain

$$E_{e,C_1} = \tfrac{1}{2}\,C_1V_0^2\int_0^1 (1-x)^2\,dx \tag{10}$$

$$= \frac{1}{2}\cdot\frac{C_1}{3}\,V_0^2. \tag{11}$$

The above equation states that if the voltage across a distributed capacitor changes linearly from zero to a maximum value V_0, then the equivalent capacitance is 1/3 of the total capacitance. Since C_2 sustains a maximum voltage of $V_0/2$, its electric energy is equal to

$$E_{e,C_2} = \frac{1}{2}\cdot\frac{C_2}{3}\cdot\left(\frac{V_0}{2}\right)^2 \tag{12}$$

$$= \frac{1}{2}\cdot\frac{C_2}{12}\,V_0^2. \tag{13}$$

From (11) and (13), the total electric energy stored in the inductor is

$$E_e = E_{e,C_1} + E_{e,C_2} \tag{14}$$

$$= \frac{1}{2}\cdot\frac{4C_1 + C_2}{12}\,V_0^2 \tag{15}$$

yielding the equivalent capacitance as

$$C_{eq} = \tfrac{1}{12}\,(4C_1 + C_2). \tag{16}$$

The foregoing method can be applied to a stack of multiple spirals as well. For an inductor with n stacked spirals, (6) suggests that the voltage is equally divided among the spirals. Therefore, interlayer capacitances sustain a maximum voltage of $2V_0/n$, whereas the bottom-layer capacitance sustains V_0/n. Now, using the result of (11) and adding the electric energy of all layers, we have

$$E_e = \frac{1}{2}\sum_{i=1}^{n-1}\frac{C_i}{3}\left(\frac{2V_0}{n}\right)^2 + \frac{1}{2}\cdot\frac{C_n}{3}\left(\frac{V_0}{n}\right)^2 \tag{17}$$

$$= \frac{1}{2}\cdot\frac{4\sum_{i=1}^{n-1}C_i + C_n}{3n^2}\,V_0^2 \tag{18}$$

and hence

$$C_{eq} = \frac{1}{3n^2}\left(4\sum_{i=1}^{n-1}C_i + C_n\right). \tag{19}$$

The simplified model used to derive the equivalent capacitance is slightly different from the exact physical model of a stacked inductor. The following three issues must be considered.

1) We have assumed that all inductors in the distributed model are perfectly coupled. However, the coupling between orthogonal segments of a spiral or different spirals is very small. Nonetheless, if we assume that the inductor elements that are on top of each other are strongly coupled, then they sustain equal voltages. Therefore, the total voltage is still equally divided among the spirals. Furthermore, since each spiral is composed of a few groups of coupled inductors, the linear voltage profile is a reasonable approximation. To verify the last statement, a two-turn single spiral has been simulated. The spiral has been divided into 20 sections (twelve sections for the outer turn and eight sections for the inner turn). Then, inductor elements in the same segment and parallel adjacent segments are strongly coupled while there is no magnetic coupling between other segments (orthogonal and parallel segments with opposite current direction).

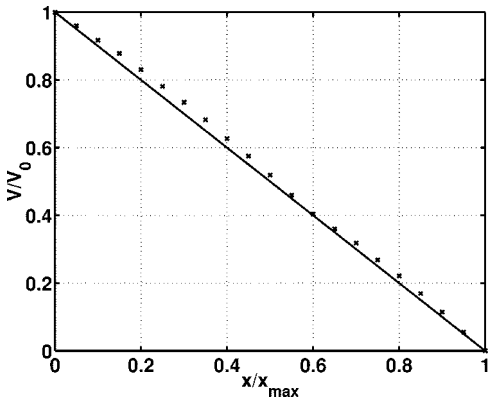

Fig. 6. Simulated voltage profile of a single spiral.

Fig. 6 shows the voltage profile for this structure. As seen in this figure, the actual profile is relatively close to the linear approximation.

2) We have neglected the electric energy stored in the trace-to-trace capacitance $C_{\rm TT}$ (the capacitance between two adjacent turns in the same layer). Supported by the experimental results in Section VII, this assumption can be justified by two observations. First, the width of the metal segments is typically much greater than the metal thickness. Therefore, even for a small spacing between the segments, $C_{\rm TT}$ is usually smaller than the interlayer capacitance. Second, the adjacent turns in the same spiral sustain a small voltage difference. Noting that the electric energy is proportional to the square of voltage, we conclude that the effect of $C_{\rm TT}$ is negligible.
3) Presenting all of the loss mechanisms by parallel resistors in the distributed model introduces little error in the calculation of the self-resonance frequency. For metal resistance and magnetic coupling to the substrate, parallel resistors are a good model if $Q^2 \gg 1$.

It is important to note that measurements indicate that (19) provides a reasonable approximation for $f_{\rm SR}$ of a *single* spiral as well, though the focus of the paper is on stacked spirals.

V. Modification of Stacked Inductors

For a two-layer inductor, (16) reveals that the interlayer capacitance C_1 impacts the resonance frequency four times as much as the bottom-layer capacitance C_2. In addition, for two adjacent metal layers, C_1 is several times greater than C_2. Therefore, it is plausible to move the spirals farther from each other so as to achieve a higher self-resonance frequency. For example, in a typical CMOS technology with five metal layers, $C_{M_5-M_4} \cong 40$ aF/μm^2 and $C_{M_4-sub} \cong 6$ aF/μm^2, whereas $C_{M_5-M_3} \cong 14$ aF/μm^2 and $C_{M_3-sub} \cong 9$ aF/μm^2. It follows that for the structure of Fig. 7(a), $C_{eq,a} \approx 14$ aF/μm^2, whereas for Fig. 7(b), $C_{eq,b} \approx 5.4$ aF/μm^2, an almost three-fold reduction.

Equation (16) proves very useful in estimating the performance of various stack combinations. For example, it predicts that the structure of Fig. 7(c) has an equivalent capacitance $C_{eq,c} \approx 4$ aF/μm^2 because $C_{M_5-M_2} \cong 9$ aF/μm^2 and $C_{M_2-sub} \cong 12$ aF/μm^2. In other words, the self-resonance frequency of the inductor in Fig. 7(c) is almost twice that of the inductor in Fig. 7(a).

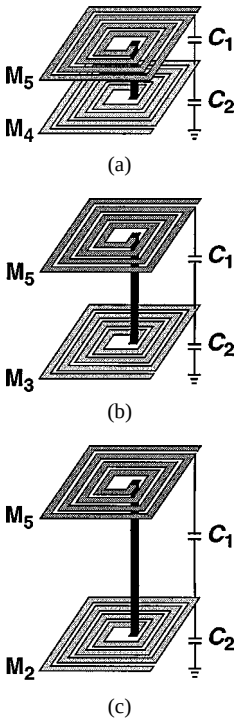

Fig. 7. Modification of two-layer stacked inductors.

Note that the value of the inductance remains relatively constant because the lateral dimensions are nearly two orders of magnitude greater than the vertical dimensions. By the same token, the loss through the substrate remains unchanged. Both of these claims are confirmed by measurements (Section VII).

The idea of moving stacked spirals away from each other so as to increase $f_{\rm SR}$ can be applied to multiple layers as well. For example, the structure of Fig. 8(a) can be modified as depicted in Fig. 8(b), thereby raising $f_{\rm SR}$ by 50%.

VI. Stacked Transformers

Monolithic transformers producing voltage or current gain can serve as interstage elements if the signals do not travel off chip, i.e., if power gain is not important. Such transformers can also perform single-ended-to-differential and differential-to-single-ended conversion.

A particularly useful example is depicted in Fig. 9, where a transformer having current gain is placed in the current path of an active mixer. Here, the RF current produced by M_1 is amplified by T_1 before it is commutated to the output by M_2 and M_3. The current gain lowers the noise contributed by M_2 and M_3 and it is obtained with no power, linearity, or voltage headroom penalty.

Fig. 10(a) shows the 1-to-2 transformer structure. The primary is formed as a single spiral in metal 4 and the secondary as two series spirals in metal 3 and metal 5. The performance of the transformer is determined by the inductance and series resistance of each spiral and the magnetic and capacitive coupling between the primary and the secondary. To minimize the capacitive coupling, the primary turns are offset with respect to

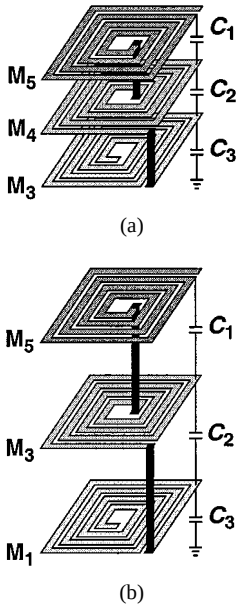

Fig. 8. Three-layer stacked inductor modification.

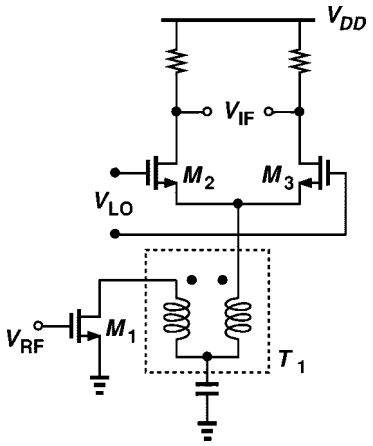

Fig. 9. Example of using a transformer to boost current in an active mixer.

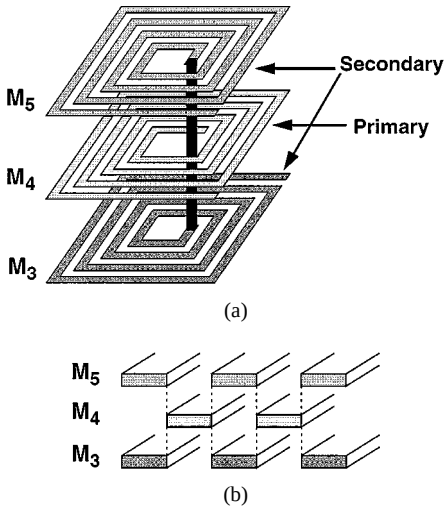

Fig. 10. Transformer structure.

the secondary turns as illustrated in Fig. 10(b). Thus, the capacitance arises only from the fringe electric field lines. The number

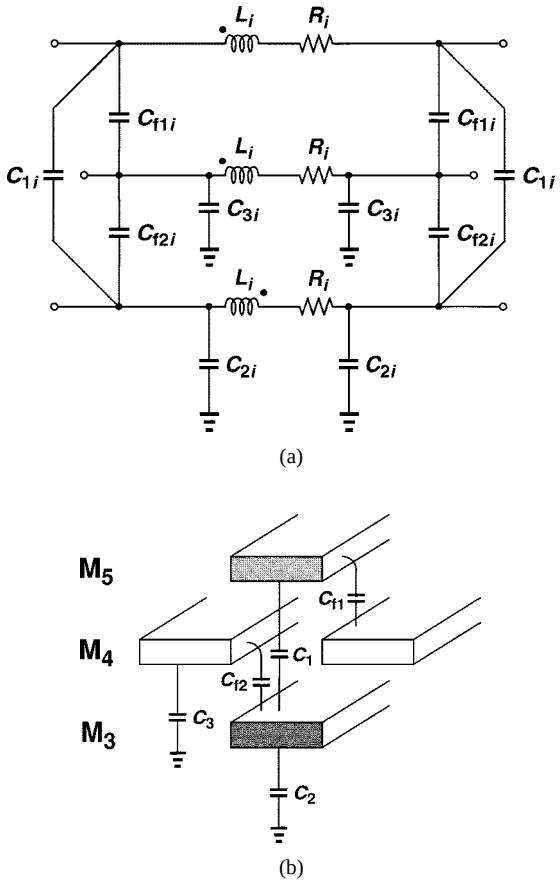

Fig. 11. Transformer model.

of turns in each spiral also impacts the voltage (or current) gain at a desired frequency because it entails a tradeoff between the series resistance and the amount of magnetic flux enclosed by the primary and the secondary. For single-ended-to-differential conversion, two of the structures in Fig. 10(a) can be cross-coupled so as to achieve symmetry.

To design the transformer for specific requirements, a circuit model is necessary. Fig. 11 illustrates one section of the distributed model developed for the 1-to-2 transformer. The segments L_i and R_i represent a finite element of each spiral, C_f's denote the fringe capacitances, C_1 models the capacitance between M_5 and M_3, and C_2 and C_3 are the capacitances between the substrate and M_3 and M_4, respectively. The values of L_i and R_i are derived assuming a uniformly distributed model and a Q of 3 for each inductor. The capacitance values are obtained from the foundry interconnect data. Fig. 12 depicts the simulated voltage gain of two transformers, one consisting of eight-turn spirals with 7-μm-wide metal lines and the others consisting of four-turn and three-turn spirals with 9-μm-wide metal lines.

Unlike stacked inductors, whose resonance frequency is not affected by the inductor loss, the transfer characteristics and voltage gain of the transformer depend on the quality factor of the spirals. In this simulation, a Q of 3 has been used for each winding. As Fig. 12, for the eight-turn transformer, capacitive coupling between the spirals is so large that it does not allow the voltage gain to exceed one, while for the four-turn and three-turn transformers we expect a gain of about 1.8 in the

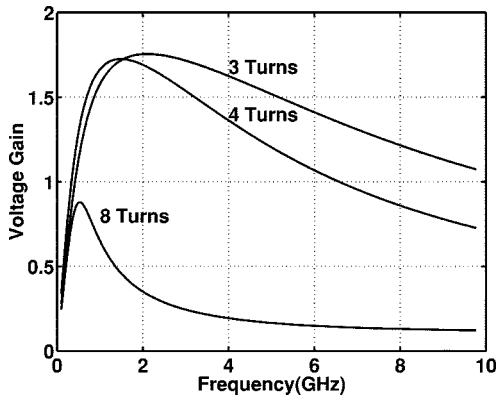

Fig. 12. Simulated voltage gain of the transformers.

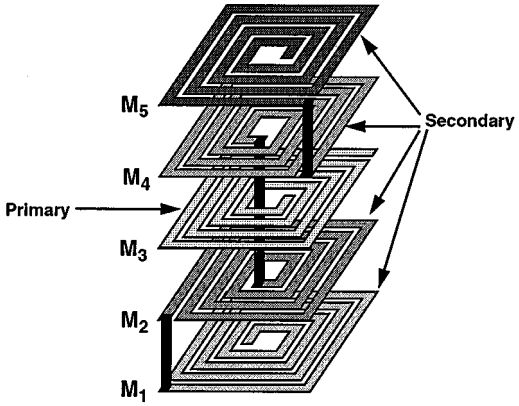

Fig. 13. 1-to-4 transformer structure.

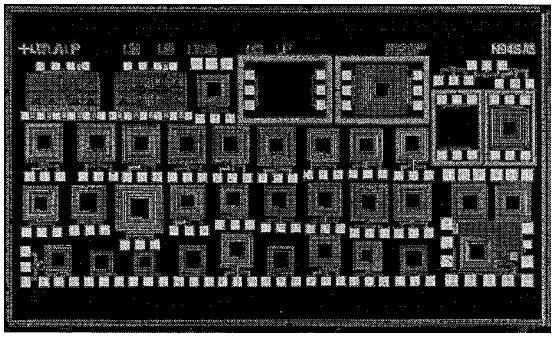

Fig. 14. Die photo.

vicinity of 2 GHz. Note that if the secondary is driven by a current source and the short-circuit current of the primary is measured, the same characteristics are observed.

The concept of stacked transformer can be applied to more layers of metal to achieve higher voltage gains. Fig. 13 shows a stacked transformer with a nominal gain of 4. In this structure, M_3 forms the primary and the rest of the metal layers are used for the secondary.

VII. Experimental Results

A large number of structures have been fabricated in several CMOS technologies with no additional processing steps. Fig. 14 is a die photograph of the devices built in a 0.25-μm process with five metal layers. Calibration structures are also included to de-embed pad parasitics.

TABLE I
MEASURED INDUCTORS IN 0.25-μm TECHNOLOGY (LINEWIDTH = 9 μm, LINE SPACING = 0.72 μm)

Inductor	Metal Layers	L (nH)	Measured f_{SR} (GHz)	Calculated f_{SR} (GHz)	Number of Turns
$L_1(240\mu m)^2$	5,4	45	0.92	0.96	7
$L_2(240\mu m)^2$	5,3	45	1.5	1.53	7
$L_3(240\mu m)^2$	5,2	45	1.8	1.79	7
$L_4(240\mu m)^2$	5,4,3	100	0.7	0.7	7
$L_5(240\mu m)^2$	5,3,1	100	1.0	1.0	7
$L_6(200\mu m)^2$	5,3,2	50	1.5	1.46	5
$L_7(200\mu m)^2$	5,2,1	48	1.5	1.54	5

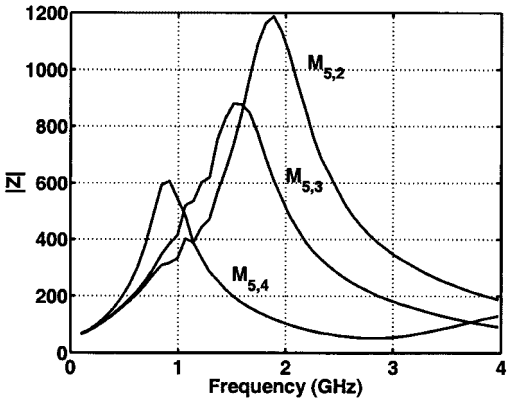

Fig. 15. Measured inductor characteristics.

TABLE II
HIGH-VALUE INDUCTORS IN 0.25-μm TECHNOLOGY (LINEWIDTH = 9 μm, LINE SPACING = 0.72 μm, NUMBER OF TURNS FOR EACH SPIRAL= 7)

Inductor Size	Metal Layers	L (nH)	Measured f_{SR}(GHz)	Calculated f_{SR}(GHz)
$(240\mu m)^2$	5,4	45	0.92	0.96
$(240\mu m)^2$	5,4,3	100	0.7	0.7
$(240\mu m)^2$	5,4,3,2	180	0.55	0.58
$(240\mu m)^2$	5,4,3,2,1	266	0.47	0.49

Table I shows the measured characteristics of some inductors fabricated in the 0.25-μm process. The Q at self-resonance is approximately equal to 3. As expected from Fig. 7, inductors L_1, L_2, and L_3, with two layers of metal, demonstrate a steady increase in f_{SR} as the bottom spiral is moved away from the top one. Fig. 15 plots the measured impedance of these inductors as a function of frequency, revealing a twofold increase in f_{SR}. For the three-layer inductors (L_4 and L_5 in Table I), proper choice of metal layers can considerably increase f_{SR}. To show how accurately (19) predicts the f_{SR}, calculated values are included as well. The error is less than 5%.

Table II shows how adding the number of metal layers can increase the inductance value. In this table, all inductors have the same dimensions but incorporate a different number of layers.

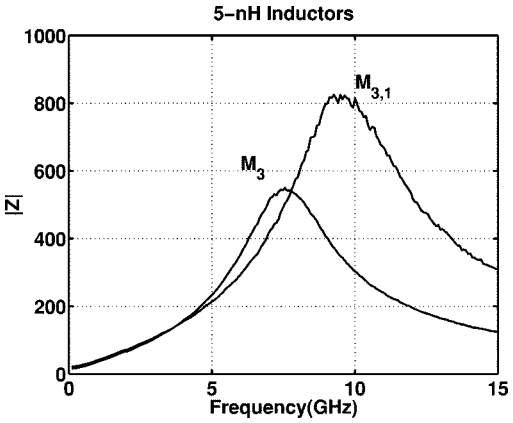

Fig. 16. Comparison of one-layer and two-layer structures for a given value of inductance.

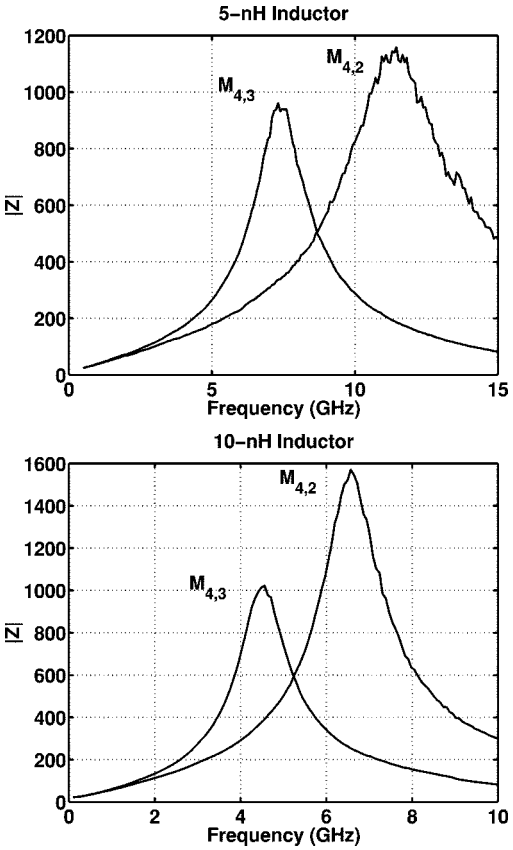

Fig. 17. Measured inductors in 0.4-μm technology.

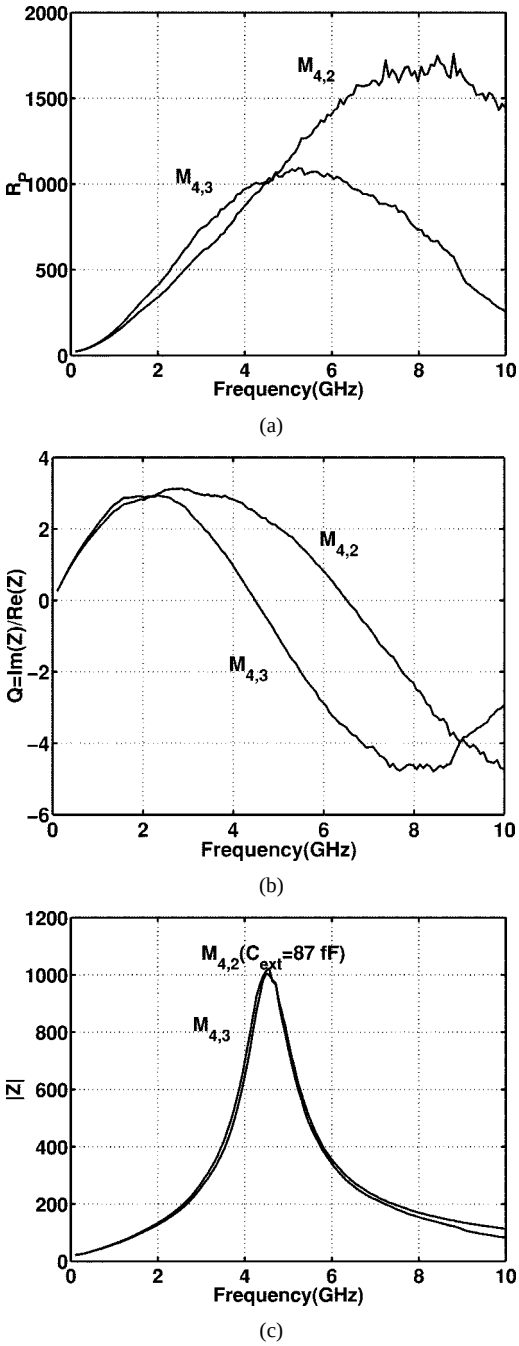

Fig. 18. Effect of inductor modification on Q.

Using five layers of metal yields an inductance value of 266 nH in an area of (240 μm)^2. Accommodating such high values in a small area makes these inductors attractive for integrating voltage regulators and dc–dc converters monolithically.

Stacking inductors can also be useful even for small values. Fig. 16 shows two 5-nH inductors fabricated in a 0.6-μm technology with three layers of metal. The two inductors were designed for the same inductance and nearly equal Q's. The plots in Fig. 16(b) show that the stacked structure has a higher $f_{\rm SR}$ because it occupies less area.

In Fig. 17, some other measured results for two pairs of 5-nH and 10-nH inductors in a 0.4-μm technology (with four layers of metal) are presented. In this case, the self-resonance frequency increases by 50% with the proposed modification. The Q at self-resonance is between 3 and 5 for the four cases. Note that for the 5-nH inductor resonating at 11.2 GHz, the skin effect is quite significant. Measured and calculated values of $f_{\rm SR}$ [from (19)] differ by less than 4%.

As mentioned before, with the proposed modification, the inductance remains relatively constant because the lateral dimensions are nearly two orders of magnitude greater than the vertical dimensions. This is indeed evident from the slope of $|Z|$ at low frequencies, which is equal to $2\pi L$ (Figs. 15 and 17).

The effect of the proposed modification on the Q is also studied. For the two 10-nH inductors of Fig. 17, we can derive the parallel resistance R_p as a function of frequency [Fig. 18(a)]. If the Q is defined as in (3), then the two inductors have equal

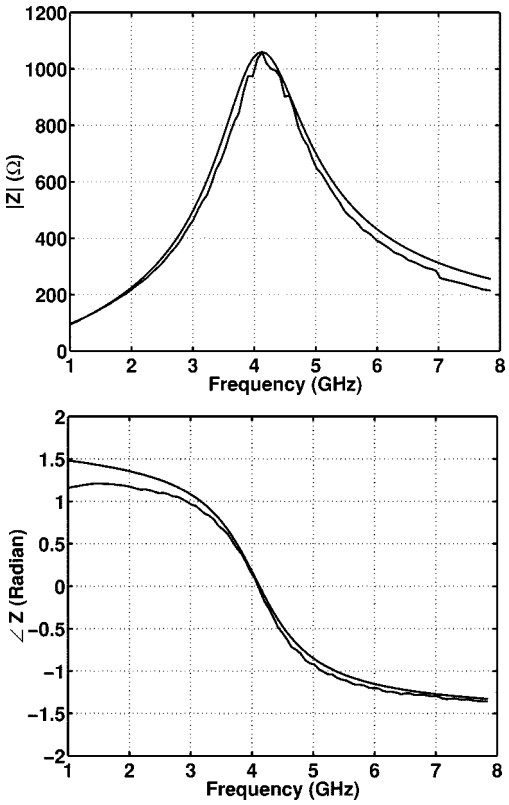

Fig. 19. Simulation and measurement comparison.

Q's around 5 GHz, and if (2) is used, the Q's are even closer for frequencies below the resonance [Fig. 18(b)].

Perhaps a fairer comparison is to assume each of the inductors is used in a circuit tuned to a given frequency (e.g., as in a VCO). We then add enough capacitance to the modified structure so that it resonates at the same frequency as the conventional one. Fig. 18(c) shows that the two inductors have the same selectivity and hence the same Q, while the modified structure can sustain an additional capacitance of 87 fF for operation at 4.5 GHz.

To simulate the behavior of an inductor, we can use the distributed circuit of Fig. 3 with a finite number of sections (e.g., 10). However, measured results indicate that for tuned applications, stacked inductors can be even modeled by a simple parallel *RLC* tank. Fig. 19 compares the simulation results of a parallel *RLC* tank and the measured characteristics. Here, the equivalent capacitance obtained from (16) and the measured value of the parallel resistance at the resonance frequency are used. These plots suggest that the magnitudes are nearly equal for a wide range and the phases are close for about $\pm 10\%$ around resonance.

Several 1-to-2 transformers have been fabricated in a 0.25-μm technology. Fig. 20 plots the measured voltage gains as a function of frequency. The measured behavior is reasonably close to the simulation results using the distributed model. The four-turn transformer achieves a voltage gain of 1.8 at 2.4 GHz and the three-turn transformer has nearly the same voltage gain over a wider frequency range. The plot also illustrates the effect of capacitive loading on the secondary (calculated using the measured S-parameters), suggesting that capacitances as high as 100 fF have negligible impact on the gain.

Fig. 21 shows the voltage gain of the 1-to-4 transformer of Fig. 13. This transformer is made of three-turn spirals with

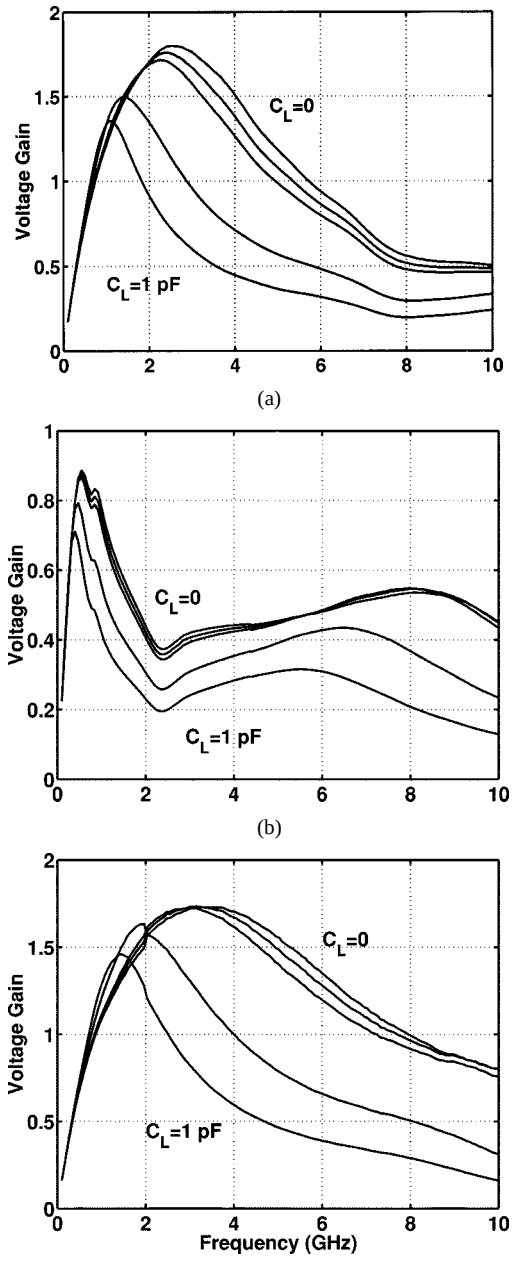

Fig. 20. Measured 1-to-2 transformer voltage gain for $C_L = 0$, 50 fF, 100 fF, 500 fF, 1 pF. (a) Four turns. (b) Eight turns. (c) Three turns.

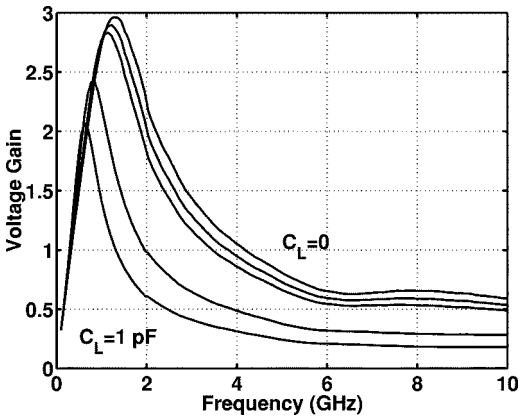

Fig. 21. Measured 1-to-4 transformer voltage gain for $C_L = 0$, 50 fF, 100 fF, 500 fF, 1 pF.

9-μm metal lines. The transformer achieves a voltage gain of 3 (9.5 dB) around 1.5 GHz. The short-circuit gain (from secondary to primary) exhibits identical characteristics.

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