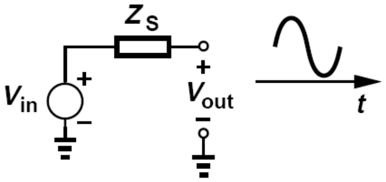
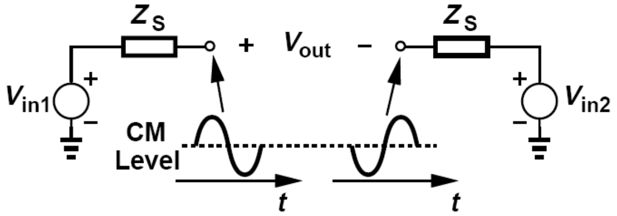
Differential Amplifiers

- **Differential & Single-Ended Operation**

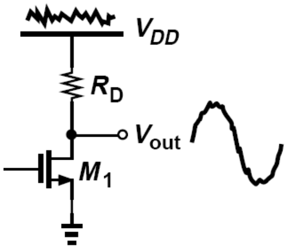
- A single-ended signal is taken with respect to a fixed potential (usually ground).

- A differential signal is taken between two nodes that have equal and opposite signals with respect to a "common mode" voltage and also equal impedances to a fixed potential (usually ground).

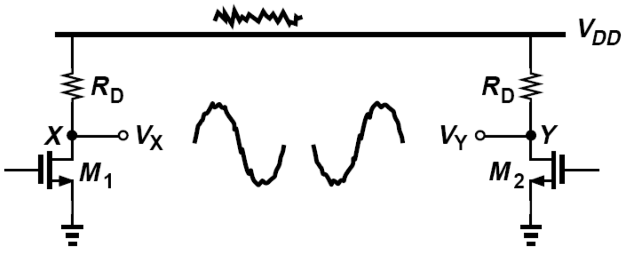




- **Why Differential?**
  - **Rejection of common-mode disturbance: supply noise, etc.**

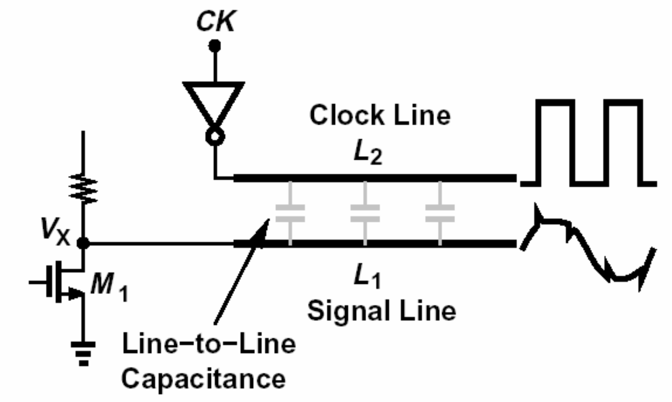


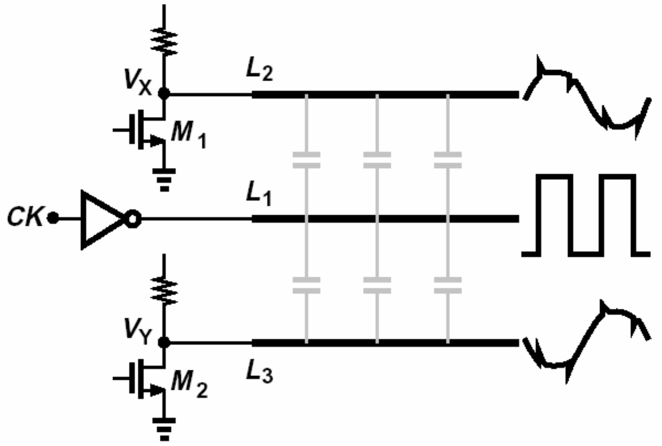
(a)



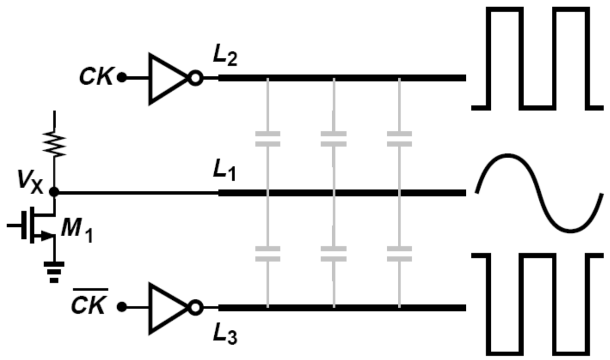
(b)

- **Rejection of coupling & feed through from other sources:**



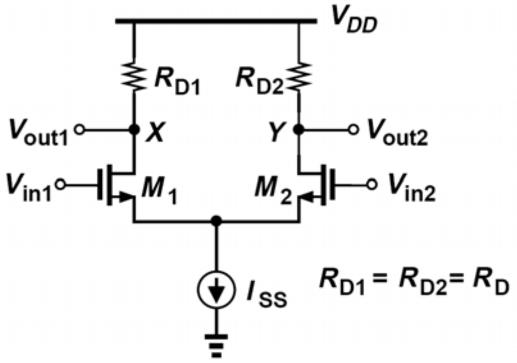


- **Reduction of coupling to other circuits;**

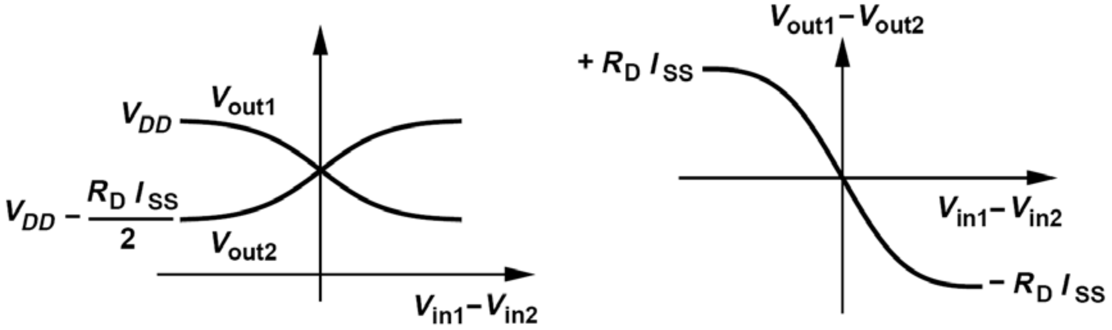


- **Maximum voltage swing almost twice that in single-ended operation;**
- **Even-order distortion suppressed (discussed later);**
- **Biasing is easier.**

Basic Differential Pair

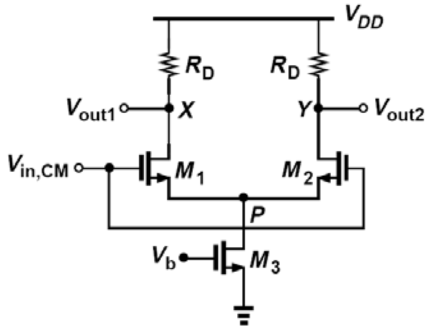


- Quantitative Analysis
Differential Behavior:

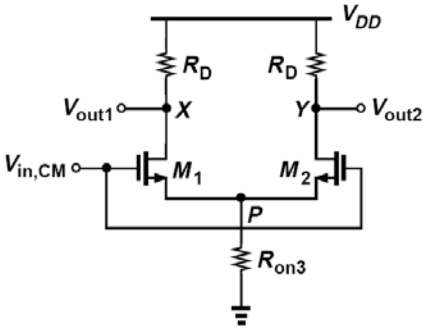


Where does the maximum small-signal gain occur?

Common-Mode Behavior:



(a)



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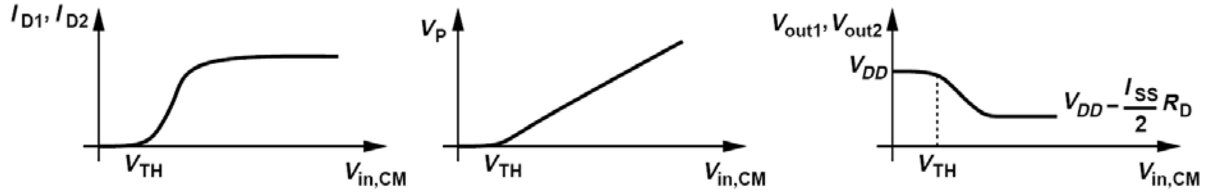
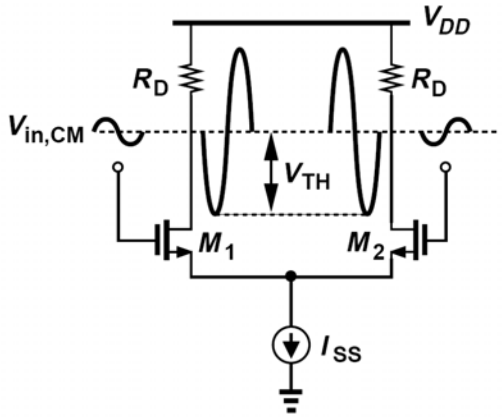


(c)

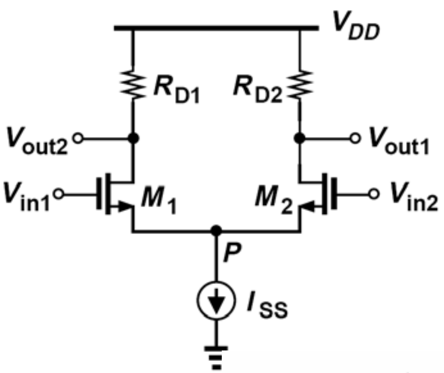
Observations:

- **The small-signal gain drops as the difference between V_{in1} and V_{in2} increases.**
- **The input and output common-mode levels must be chosen carefully. The current source requires some voltage so as to exhibit a high output impedance.**

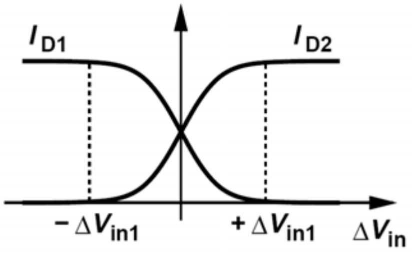
How large can the output swings be?



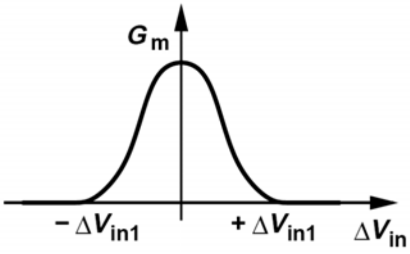
- Quantitative Analysis



$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$



(a)



(b)

Note: If neglect sub-threshold behavior, for some $V_{in1} - V_{in2}$ one transistor completely turns off. This occurs for a differential input of :

$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

This can be related to the overdrive at equilibrium:

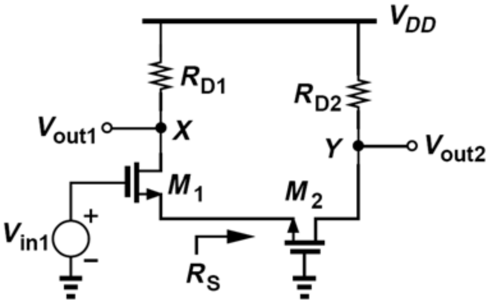
- **To achieve a wider linear range for $V_{in1} - V_{in2}$, need greater (equilibrium) overdrive. For a given bias current, this translates to lower transconductance for each device.**
- **How does the input-output characteristic change as W changes?**

Small-Signal Analysis

- **Method I**

Treat circuit as cascade of two stages and use superposition.

$$\frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$



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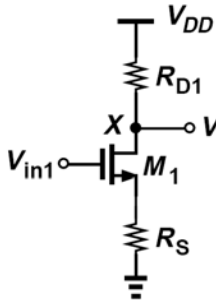
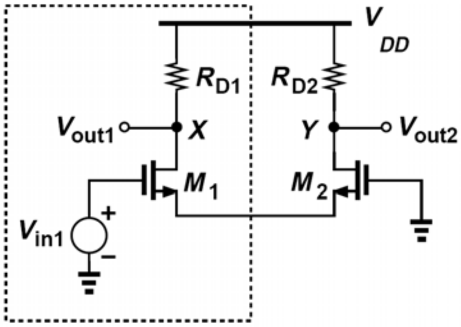
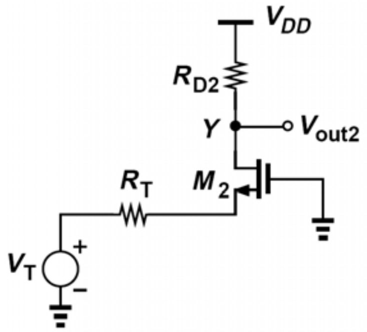


(c)

For V_Y,



(a)



(b)

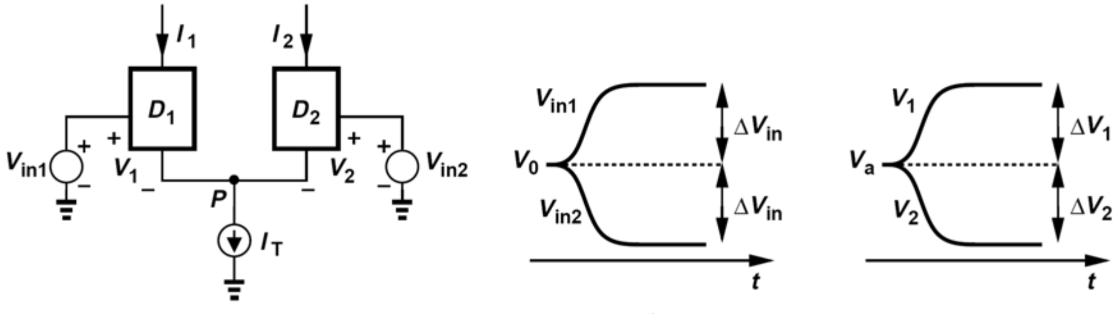
$$\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$$

- **Method II**

If the circuit is perfectly symmetric and V_{in1} and V_{in2} change by <u>equal</u> and <u>opposite</u> amounts from <u>equilibrium</u>, then we can use the concept of "half circuit."

<u>Lemma</u>

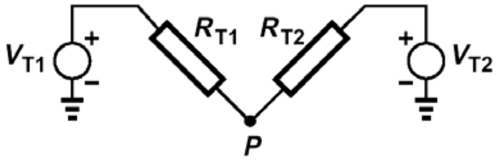
In the following symmetric circuit, if V_{in1} changes from V_0 to $V_0+\Delta V$ and V_{in2} changes from V_0 to $V_0-\Delta V$, then V_x does not change.



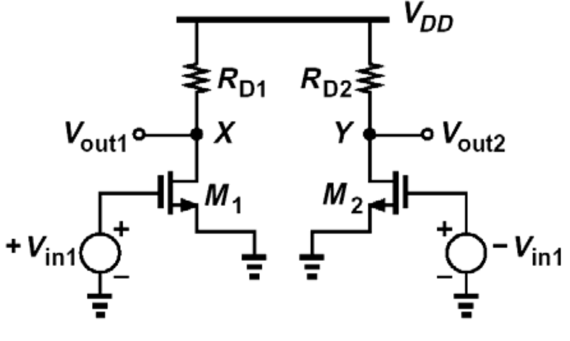
(a) (b) (c)

$$g_m \Delta V_1 + g_m \Delta V_2 = 0 \qquad V_0 + \Delta V_{in} - (V_a + \Delta V_1) = V_0 - \Delta V_{in} - (V_a + \Delta V_2)$$

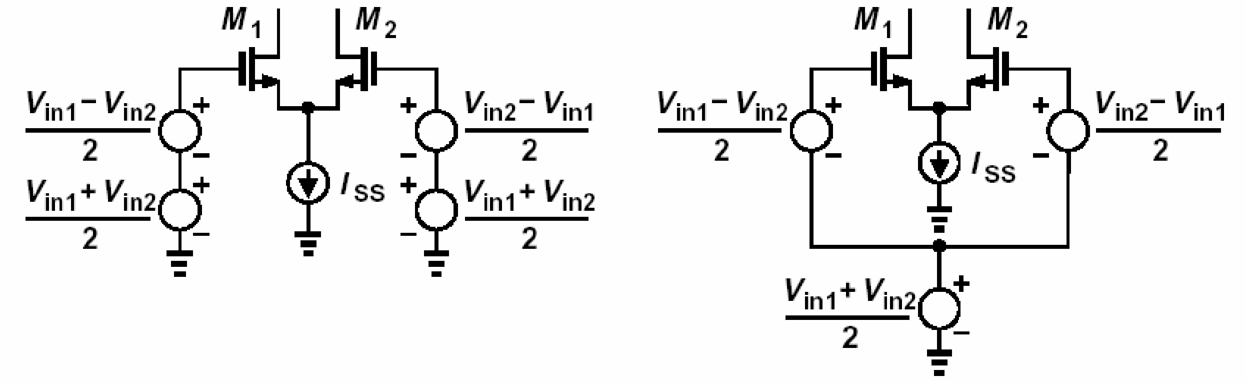
From another point of view, one transistor wants to pull V_x up while the other wants to pull it down.



=> V_x can be <u>grounded.</u>

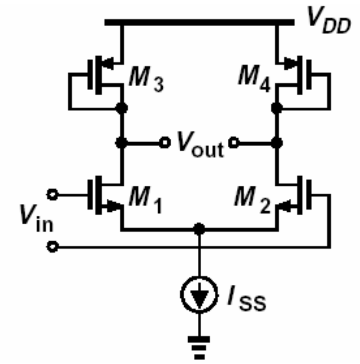


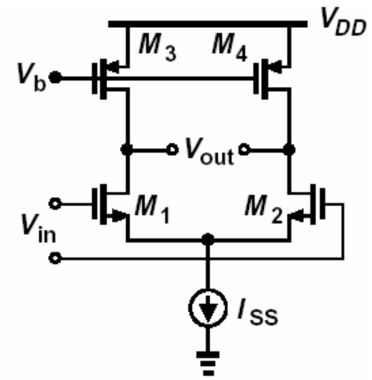
What if V_{in1} and V_{in2} are not exactly differential?

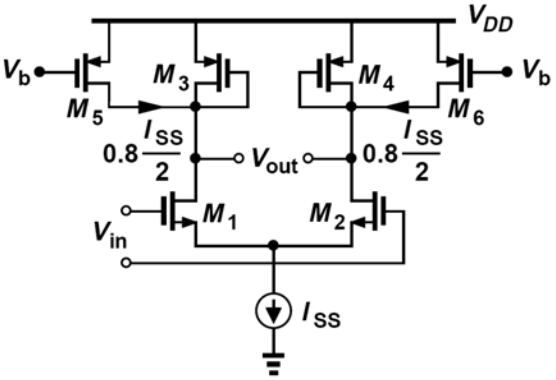


Use superposition to find the effect of differential and common-mode signals.

Other Types of Loads





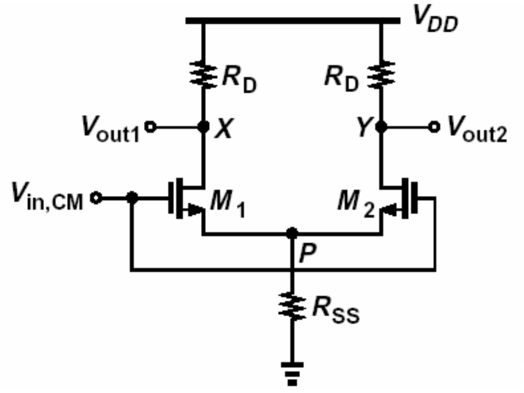


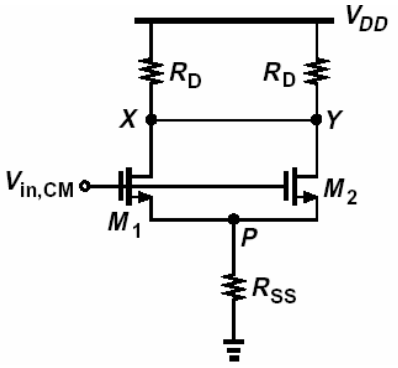
Calculate the voltage headroom requirement and small-signal gain.

How do we increase the gain of diff pair with current source loads?

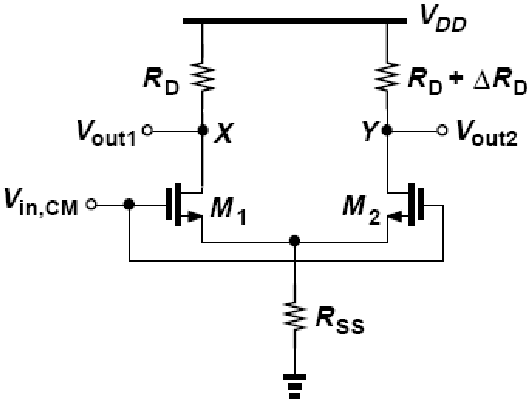
Common-Mode Response

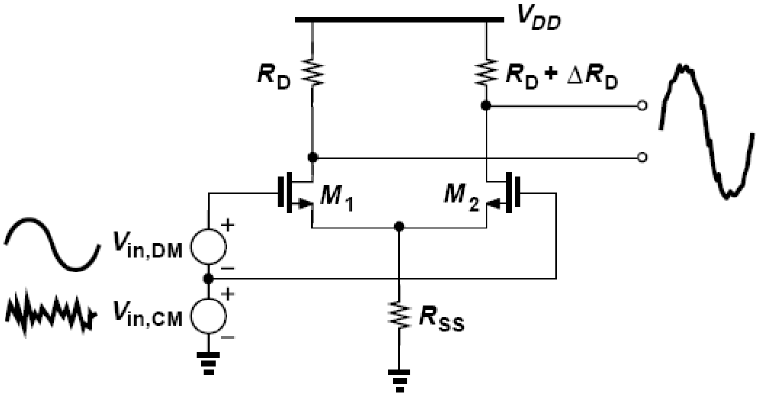
Case I : Symmteric Circuit





Case II: Asymmetric Circuit





Effect of load resistance mismatch:

$$\Delta V_X = \Delta V_{in,CM}\frac{g_m}{1+2g_mR_{SS}}R_D$$

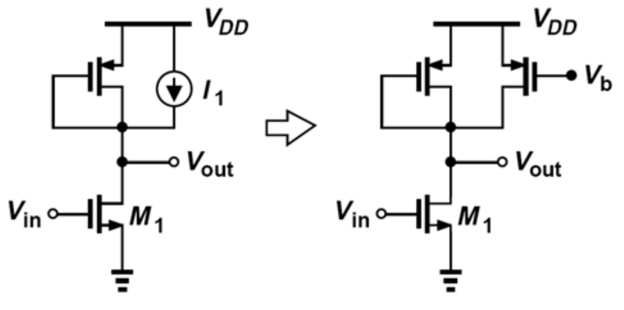
$$\Delta V_Y = \Delta V_{in,CM}\frac{g_m}{1+2g_mR_{SS}}(R_D+\Delta R_D)$$

EE215A
Fall 11

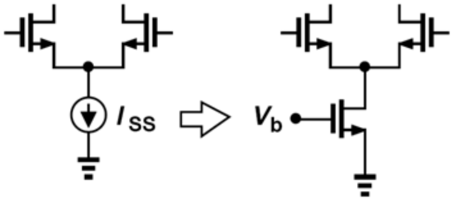
B. Razavi
HO #2

Current Mirrors & Active Loads

In analog design (and sometimes digital design), we may need to generate many well-defined bias currents. For example:

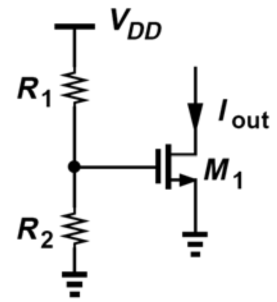


(a)



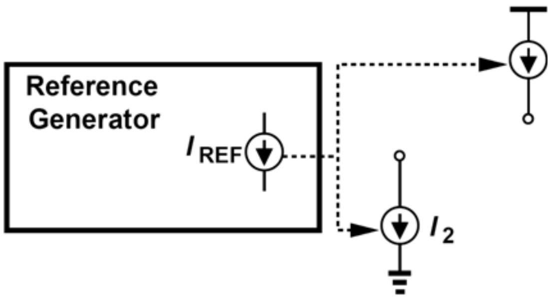
(b)

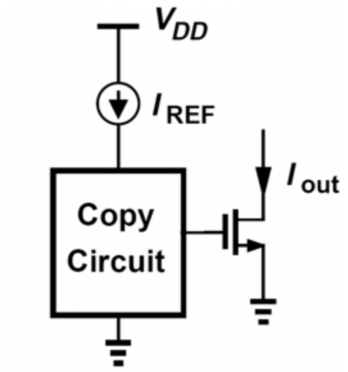
Each current source can be realized as:



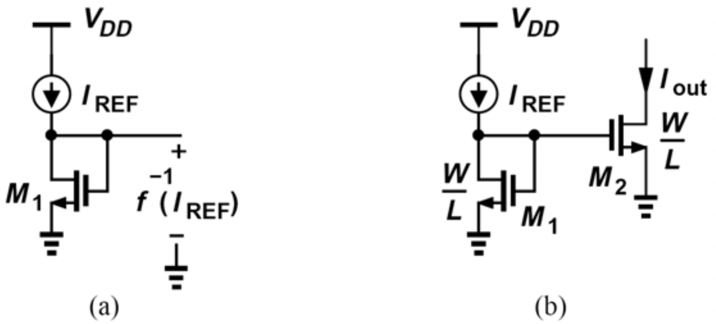
If we apply a self-defined <u>voltage</u> to the gate or the base, the current is NOT well-defined. In MOSFETs, V_{TH} can vary by tens of millivolts from wafer to wafer, causing significant error.

Better approach:

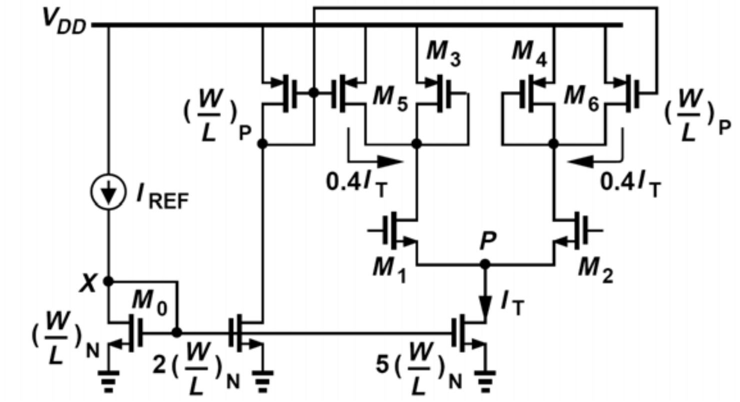




So, all we need to generate is one reference current. I_{REF} is established by precision bandgap techniques or sometimes provides externally.



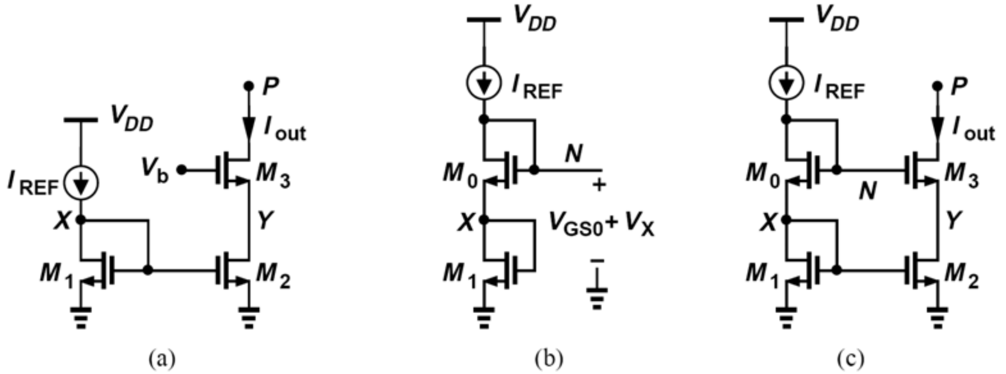
Example:



Cascode Current Mirrors

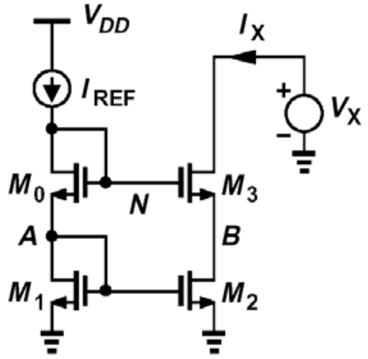
Channel-length modulation causes error if the voltage across the diode-connected device is not equal to V_{DS} of current sources.

To suppress this effect, we can use cascodes:

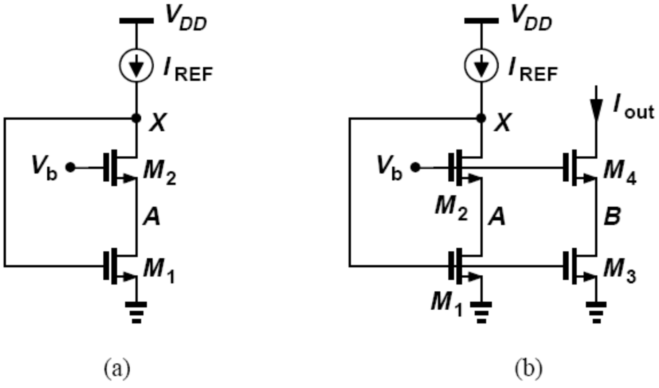


- **What is the minimum allowable voltage across the current source?**

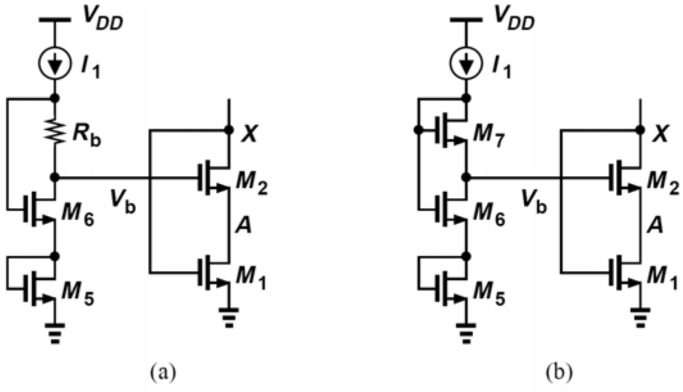
Example:



Low-Voltage Cascode



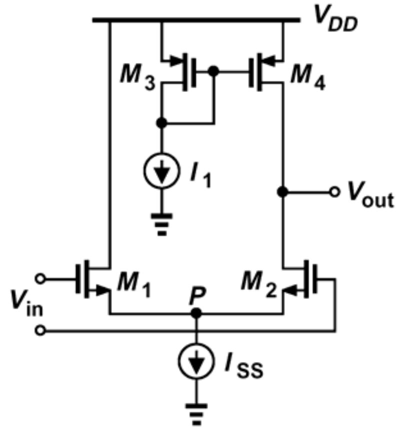
How to generate Vb?



(a) (b)

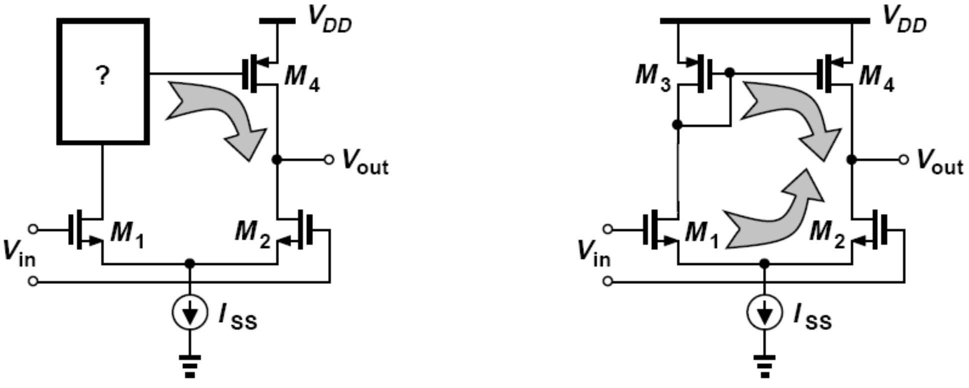
Active Load with Current Mirror

Suppose we need a high-gain differential amplifier with single-ended output:



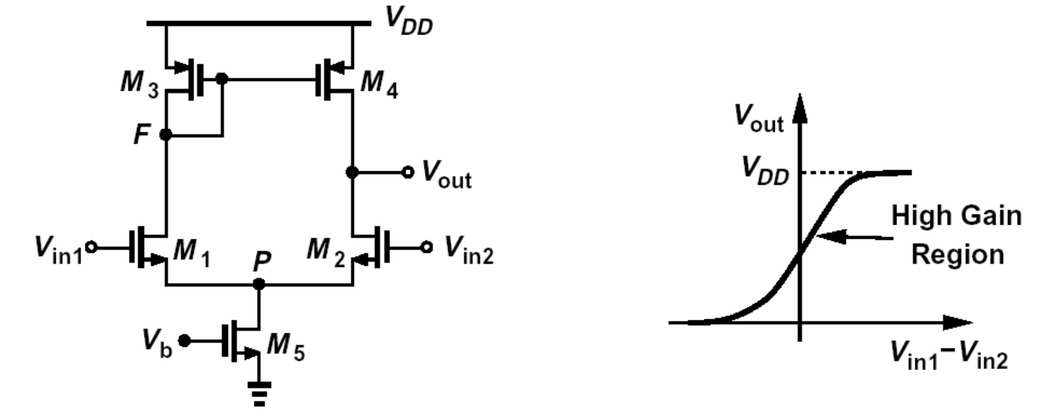
What is the voltage gain?

Active Load:

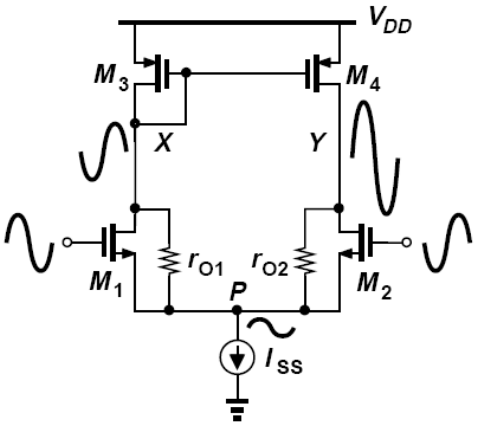


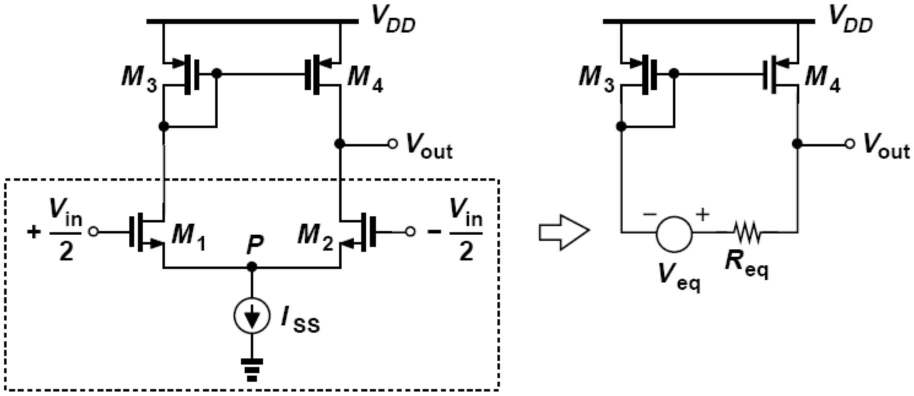
(a) (b)

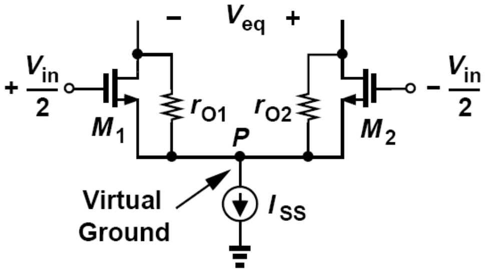
Large-Signal Behavior:



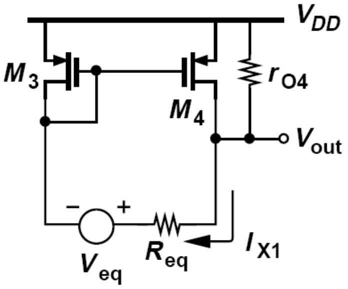
Small-Signal Behavior:







(a)

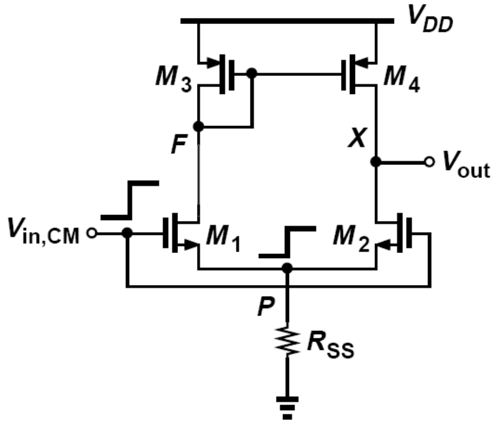


(b)

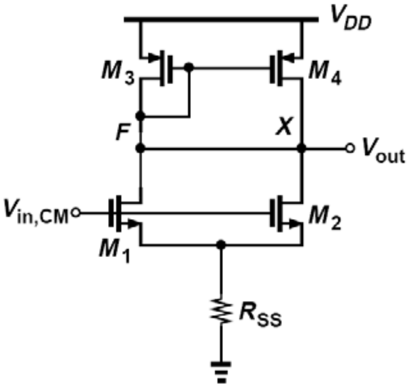
What is the dc output voltage in equilibrium?

How do we increase the voltage gain?

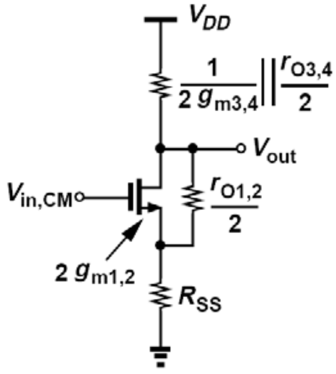
<u>Common-Mode Rejection</u>



What is the common-mode gain?



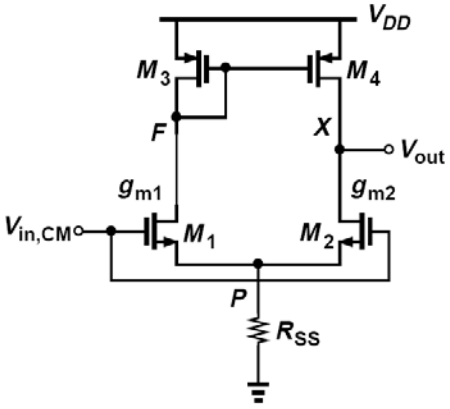
(a)



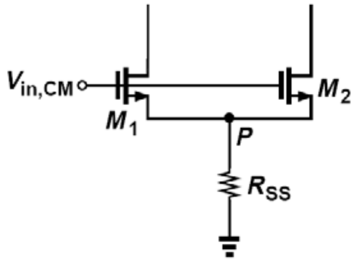
(b)

Thus, even if the circuit is perfectly symmetric, CMRR is not infinite.

In practice, random mismatches between the two sides result in a finite CMRR.



(a)



(b)

$$\Delta V_P = \Delta V_{in,CM} \frac{R_{SS}}{R_{SS} + \frac{1}{g_{m1} + g_{m2}}}$$

$$\begin{aligned} \Delta I_{D1} &= g_{m1}(\Delta V_{in,CM} - \Delta V_P) \\ &= \frac{\Delta V_{in,CM}}{R_{SS} + \frac{1}{g_{m1} + g_{m2}}} \frac{g_{m1}}{g_{m1} + g_{m2}} \\ \Delta I_{D2} &= g_{m2}(\Delta V_{in,CM} - \Delta V_P) \\ &= \frac{\Delta V_{in,CM}}{R_{SS} + \frac{1}{g_{m1} + g_{m2}}} \frac{g_{m2}}{g_{m1} + g_{m2}}. \end{aligned}$$