

Fall 2011

Analog Integrated Circuit Design

Instructor: Behzad Razavi
56-147D, Eng. IV
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Office Hours: MW, 1:00-2:30 pm

Time: MW 4:00-5:50 pm

Place: Boelter 5249

Prerequisites: Undergraduate electronics courses, e.g., EE 115B

Credit: 4 Units

Grading: Midterm 30%
Final 30%
Homeworks 20% (Late HW Policy: 25% deduction per day)
(Keep a copy. We are not responsible for lost homeworks.)
Final Project 20%

Use of laptops is not allowed during class.

Course Textbook:

B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

Recommended Books:

P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Edition, 2001, Wiley.

D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1997.

Important Dates:

Mon., Oct. 3,	HW#1 Due
Wed., Oct. 12	HW#2 Due
Mon., Oct. 24	HW#3 Due
Mon., Oct. 31	HW#4 Due
Wed., Nov. 2	Midterm Exam
Fri. Dec. 2	Final Project Due
Mon. Dec. 5, 8:00-11 am	Final Exam

Outline

- MOS Device Structure and Circuit Models
- Single-Stage and Differential Amplifiers
- Passive and Active Current Mirrors
- Frequency Response of Amplifiers
- Noise
- Feedback
- Op Amp Design
- Stability and Frequency Compensation
- Bandgap References
- Introduction to Switched-Capacitor Circuits

Simulation Platform: HSPICE or Cadence. The device models for 0.18-um technology are posted at <http://www.ee.ucla.edu/~brweb/teaching.html> and called 215a.sp (for HSPICE) and 215a.scs (for Cadence). The minimum device width is 0.6 um. The source/drain area is given by $W \times 0.6$ um, and the perimeter by $2W + 1.2$ um.

For a Cadence tutorial, visit http://www.ee.ucla.edu/~dejan/ee115c/ee115c_flow.htm. You need 8-10 hours to learn the basics; so be patient!