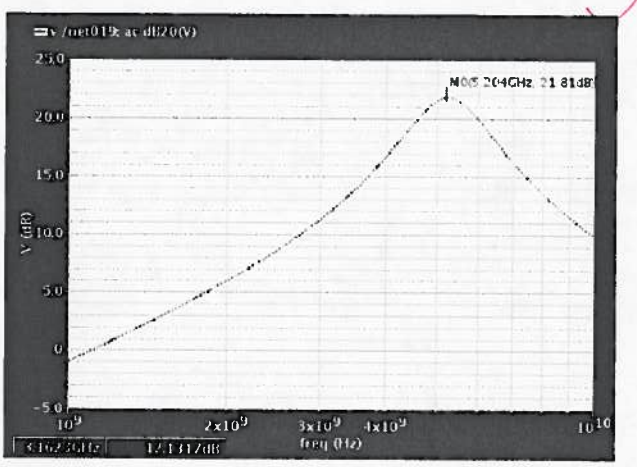
40/40

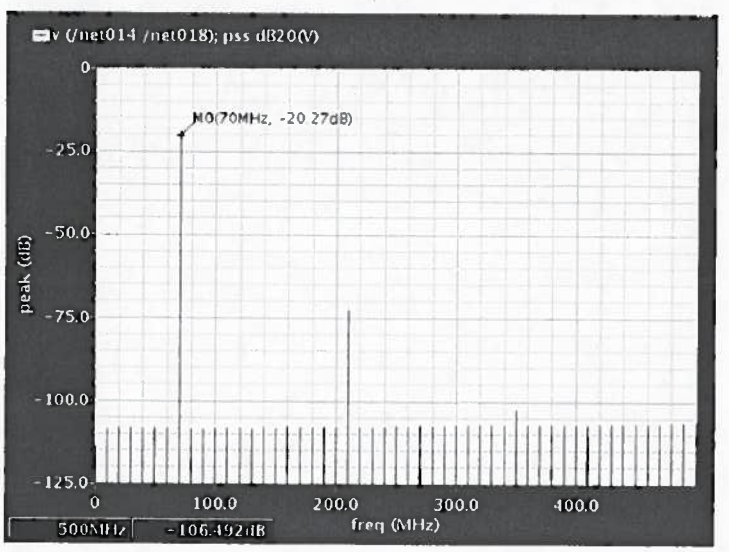
Homework 3

Yilei Li

5 a) In order to resonate at 5.2 GHz, the width of M2 is 7.8 um. The simulated AC response of the first stage is plotted below, the gain of LNA is 21.81 dB from input to output. The total gain from source to output should be about 21.81 dB-6 dB=15.81 dB since input of LNA is roughly matched.



10 b)With smaller width of M3 and M4, the on-resistance of M3 and M4 is large and thus makes gain small; on the other hand, oversizing makes gain drop due to parasitic capacitance. Width of M3 and M4 is 15 um to achieve largest conversion gain for the RF frontend. When the input power at 50 Ω antenna interface is -35 dBm, the voltage at the input of mixer Vin is -23.55 dBV , and the differential output is Vout=-20.27 dBV (as shown below). Thus the conversion gain of mixer is Vout/(Vin/2)=-20.27 dBV-(-23.55 dBV-6 dB)=9.28 dB. For the RF frontend, Vin/2 at input is -44.031 dBV, and so conversion gain is 23.73 dB. This is roughly the total gain of LNA plus the conversion gain of mixer, and the difference between those two should come from the non-perfect matching of LNA (input impedance is not 50 Ω and input at LNA is not exactly Vin/2).



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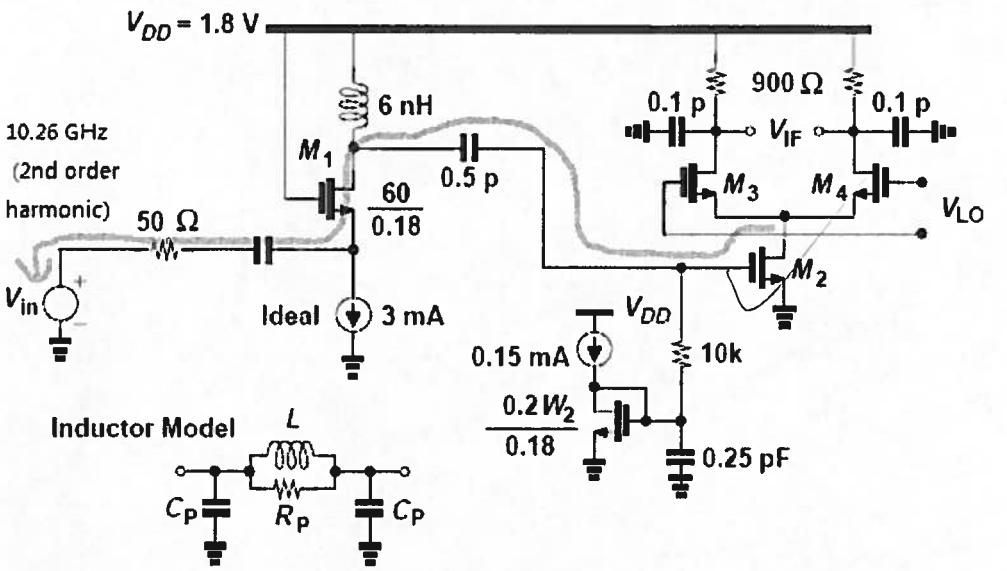
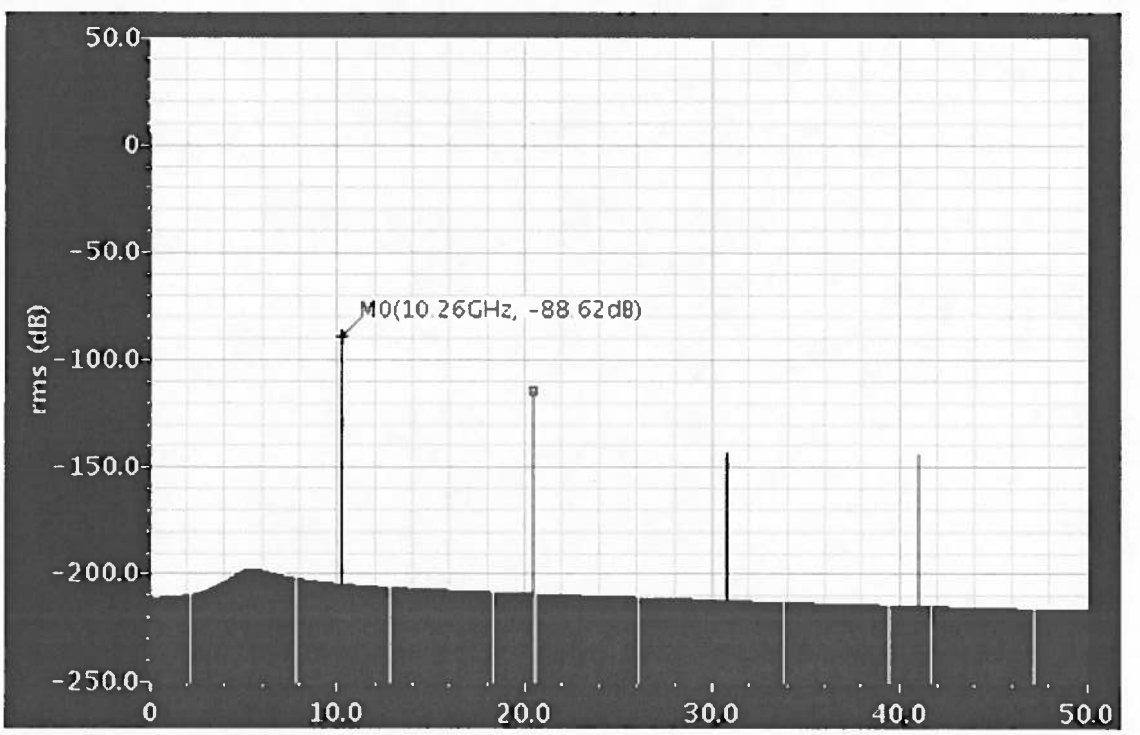
c)When there is no mismatch, the LO leakage is the second-order harmonic of LO (10.26 GHz) at the source of M3 and M4 through coupling capacitors to the output, as shown below.



The leakage is -88.62 dBV rms, which equals to 37.07 uVrms.



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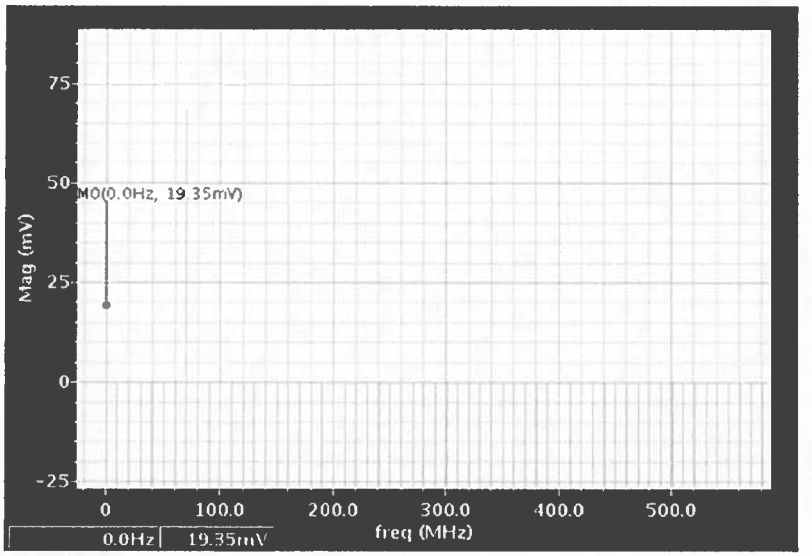
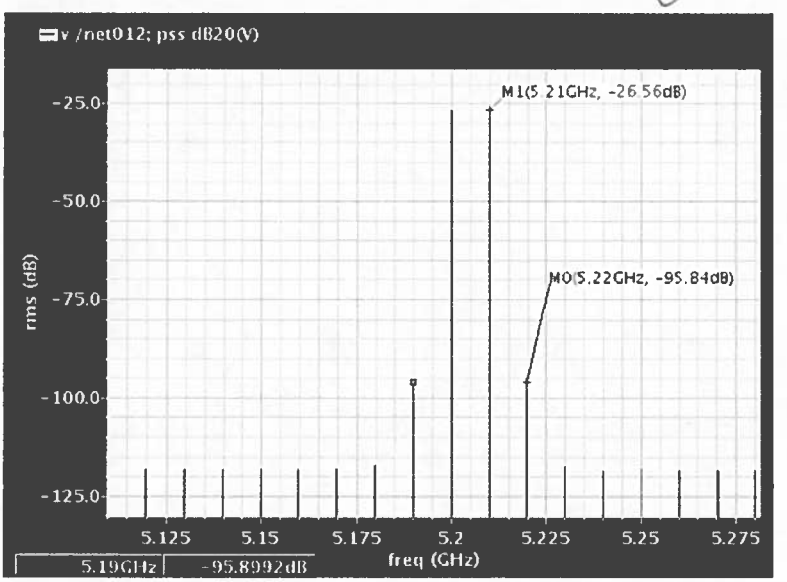
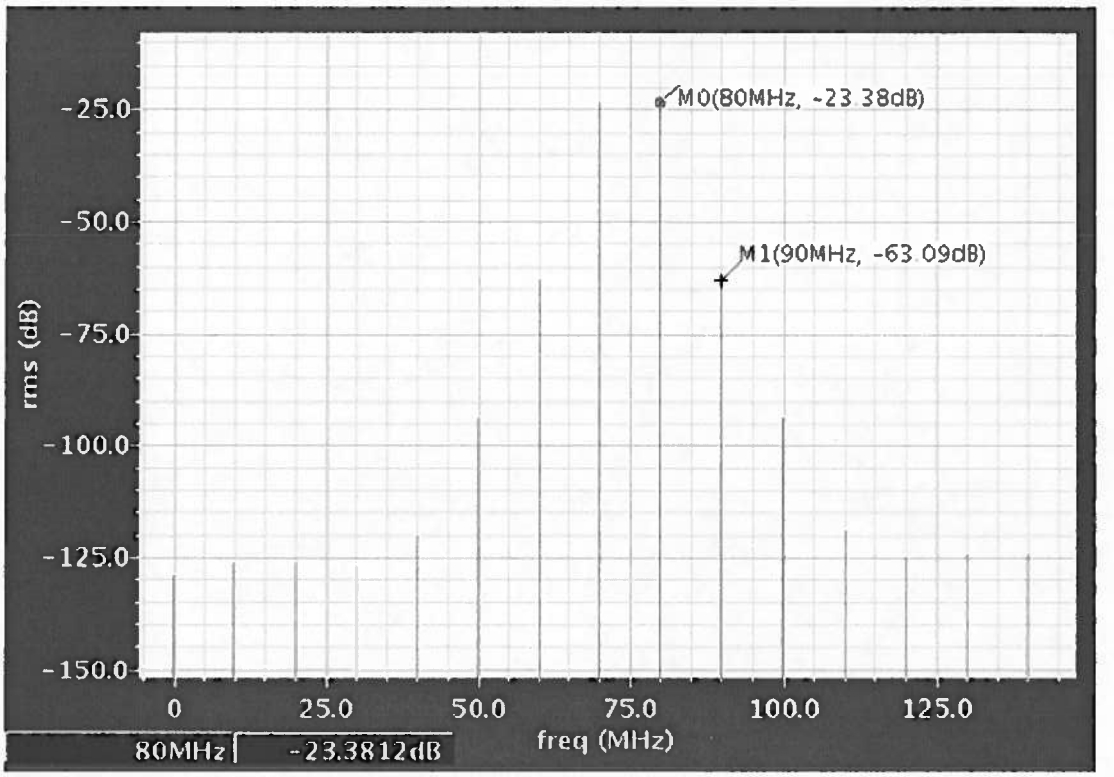
d)When M3 and M4 have Vth mismatch of 15 mV and LO has 6% second harmonic, the simulated DC offset is 19.35 mV at output. When the offset at M3 and M4 input has different polarity, the offset may vary. The 19.35 mV offset at output corresponds to worst case.



10 e)Input power is P_{in}=-35 dBm for the whole RF frontend. The ΔP_3 of LNA is ΔP_{3LNA}=69.28 dB (as shown below), and thus $IIP3_{LNA}$= P_{in} + ΔP_{3LNA} /2=-0.36 dBm.



The The ΔP_3 of overall circuit is ΔP_{3tot}=39.71 dB (as shown below), and thus $IIP3_{tot}$= P_{in} + ΔP_{3tot} /2=-15.14 dBm. Compared with the IIP3 of LNA, the IIP3 of the overall circuit is greatly degraded, and thus it can be concluded that the second stage is the bottleneck of linearity. This is due to the high gain of the first stage.


M0(80MHz, -23.38dB)
M1(90MHz, -63.09dB)
-25.0
-50.0
-75.0
-100.0
-125.0
-150.0
rms (dB)
0
25.0
50.0
75.0
100.0
125.0
freq (MHz)
80MHz
-23.3812dB