

Winter 2013

Analysis and Design of RF Circuits and Systems

Instructor: Behzad Razavi
 56-147D, Eng. IV
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 Office Hours: TR, 10:30-12:00
 Handouts posted at <http://www1.ee.ucla.edu/~brweb/teaching.html>

Time: TR, 4:00-5:50 pm

Place: Boelter 8500

Use of laptops is prohibited during lectures (and exams).

Prerequisites: EE215A (Preferably with a grade of A- or higher)
 Working Knowledge of Cadence

Credit: 4 Units

Grading: Midterm 30%
 Final 30%
 Homeworks 20% (Late HW Policy: 25% deduction per day)
 Final Project 20%
 (MS and PhD students are graded on the same curve.)

Course Textbook:

B. Razavi, *RF Microelectronics*, Second Edition, (US Edition), Prentice-Hall, 2012

Reference Book:

T. H. Lee, *The Design of Radio-Frequency CMOS Circuits*, Cambridge University Press, 2004.

Audit Policy: Individuals can audit if they do not collect the handouts.

Important Dates:

Thur. Jan. 17 (Start Cadence sims today!)	HW#1 Due
Thur. Jan. 24	HW#2 Due
Tue. Feb. 5	HW#3 Due
Thur. Feb. 14	HW#4 Due
Tue. Feb. 19	Midterm Exam
Fri.. March 15	Final Project Due
Thur. March 21, 11:30 am-2:30 pm	Final Exam

Outline

- Basic Concepts
 - Harmonic and Intermodulation Distortion, Third Intercept Point, Cascaded Stages
 - Random Processes and Noise, PDF, PSD, Noise Figure, Cascaded Stages
 - Sensitivity and Dynamic Range
- Brief Communications Background
 - Analog and Digital Modulation, AM, FM, QPSK Family, FSK, GMSK
 - Bandwidth and Power Efficiency
 - Multiple Access Techniques (FDMA, TDMA, CDMA)
 - Wireless Standards (IS-54, GSM, DECT, IS-95, WCDMA, WiFi)
- RF Transceiver Architectures
 - Heterodyne, Direct Conversion, and Image-Reject Receivers
 - Two-Step and Direct-Conversion Transmitters
- Low-Noise Amplifiers and Mixers
 - CMOS LNAs
 - Passive and Active Mixers
 - DSB and SSB Noise Figures
 - CMOS Mixers
- Oscillators
 - Basic LC Oscillator Topologies
 - Phase Noise
 - Phase Noise Mechanisms
 - CMOS VCOs
 - Quadrature Signal Generation
- Frequency Synthesizers
 - Phase-Locked Loops (Loop Dynamics, Building Blocks, Types I and II)
 - Phase-Locked Synthesizer Architectures (Integer-N, Fractional-N)
 - Frequency Dividers and Prescalers