EE 215D

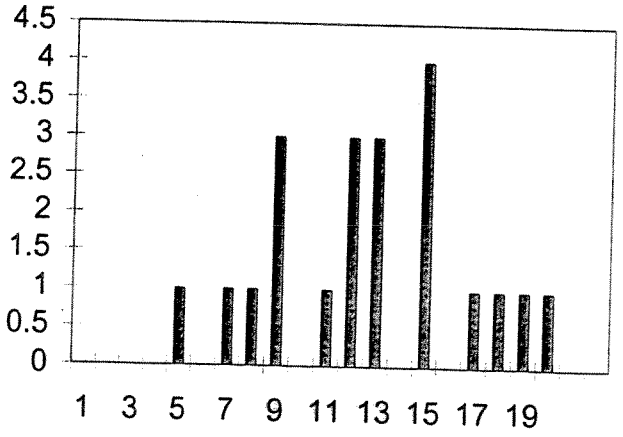
Midterm Exam

Spring 2003

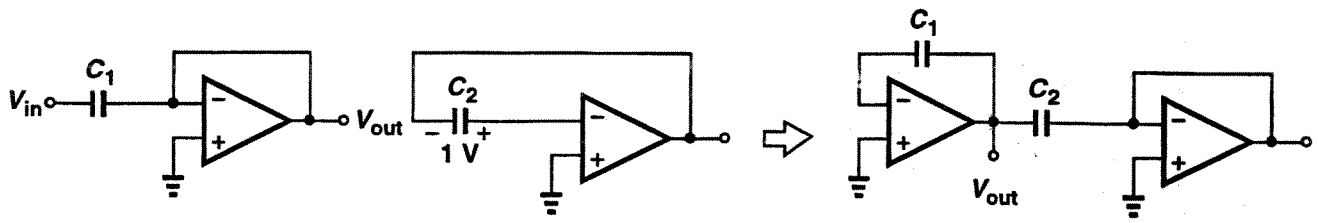
Name: Solutions

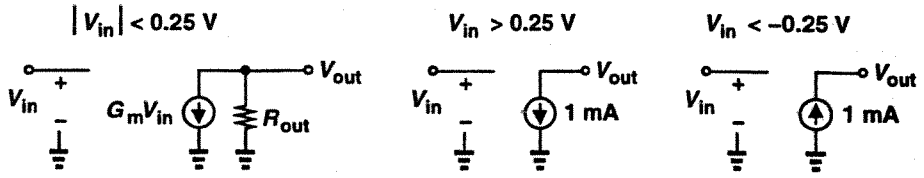
Time Limit: 2 Hours

Open Book, Open Notes



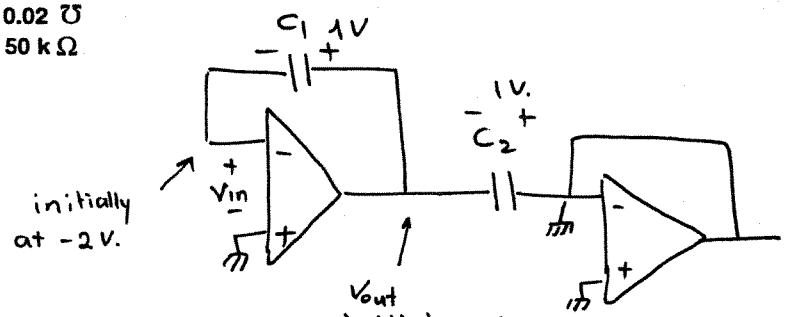
1. Two unity-gain samplers appear in a pipeline as shown below. When the first stage is in the acquisition mode, the second is in the hold mode and vice versa. Suppose $V_{in} = 1$ V and model the op amp as shown below. With the initial condition shown in the second stage, determine the time it takes V_{out} to reach within 0.1% of its final value. You can assume the second op amp creates a good virtual ground at its inverting input in this mode. Sketch the waveform for V_{out} as the first stage goes from sampling to hold. Assume $C_1 = C_2 = 1$ pF. (5)





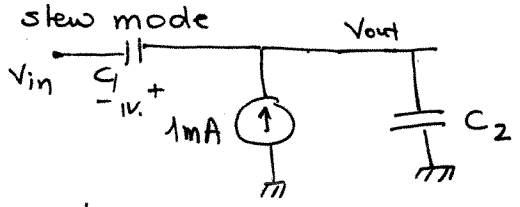
$G_m = 0.02$ ℧
$R_{out} = 50$ kΩ

Hold mode:



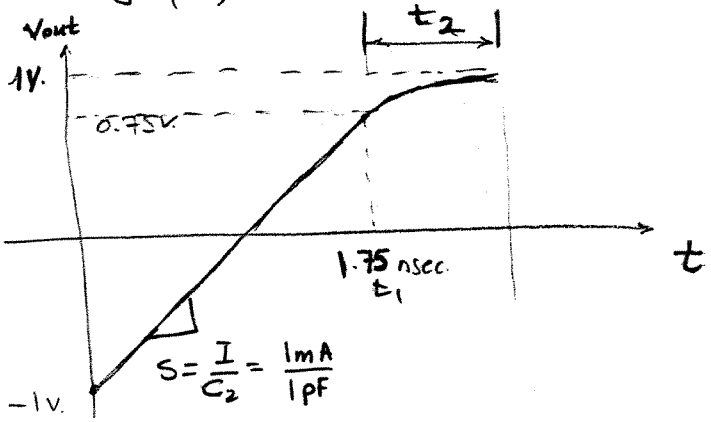
at $V_{in} = -2$ V.

* → slew mode



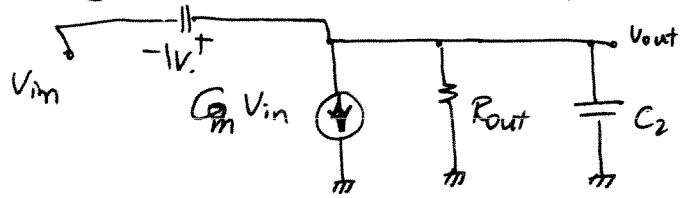
$V_{in} = V_{out} - 1$

V_{out} reaches 0.75 V. at 1.75nsec where $V_{in} = -0.25$ V.



at this point Vout starts to

* linearly settle to its final value.



$V_{in} = V_{out} - 1$

$V_{out}(0) = 0.75$ V.

$$-G_m(V_{out} - 1) = \frac{V_{out}}{R_{out}} + C_2 \frac{dV_{out}}{dt}$$

$$\therefore \left(-G_m - \frac{1}{R_{out}}\right) V_{out} + G_m = C_2 \frac{dV_{out}}{dt}$$

$G_m = 0.02$

$R_{out} = 50\,k$

$C_2 = 1\,pF$

$$\therefore \quad C_2 \frac{dV_{out}}{dt} + \left(G_m + \frac{1}{R_{out}}\right) V_{out} = + G_m . 1 \qquad \text{—①}$$

$V_{out}(0) = 0.75$

Solving Eqn (1)

$$\therefore V_{out}(t) = \frac{G_m . 1}{G_m + \frac{1}{R_{out}}} + \left(\frac{-G_m}{G_m + \frac{1}{R_{out}}} + \overbrace{0.75}^{V_{out}(0)}\right) e^{-\frac{t}{C_2}.\left(G_m + \frac{1}{R_{out}}\right)}$$

$$V_{out}(\infty) = \frac{G_m}{G_m + \frac{1}{R_{out}}} = 0.999 \text{ V.}$$

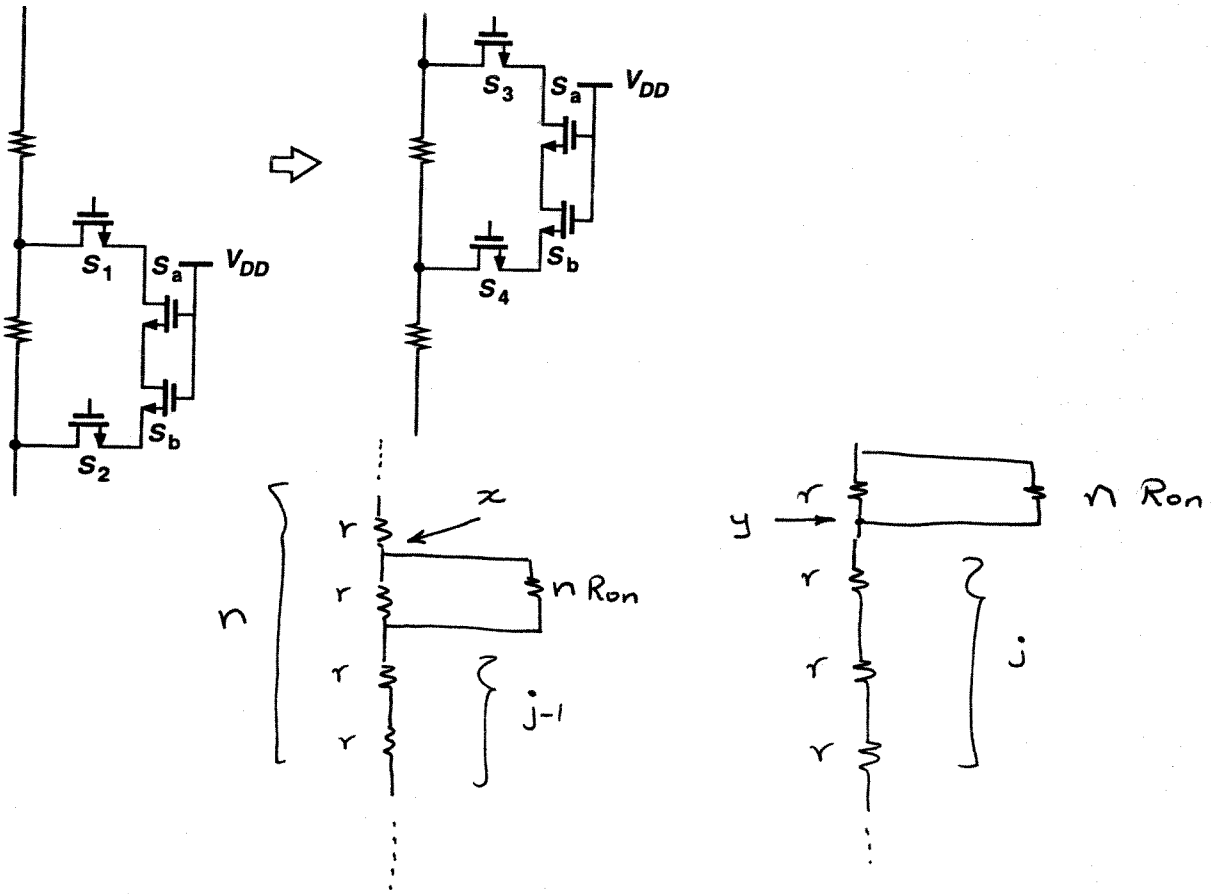
$$\therefore \text{ Error} = 0.1\,\% \; V_{out}(\infty) \cong 0.999 \text{ mV.} = 0.249\, e^{-\frac{t_2}{C_2}\left(G_m + \frac{1}{R_{out}}\right)}$$

$$\therefore \quad t_2 = 0.2758 \text{ nsec}$$

$\therefore$ The time it takes V_{out} to reach 0.1 % of its final value =

$$t_1 + t_2 = 1.75 + 0.2758 = \boxed{2.0258 \text{ nsec}}$$

2. A resistor-ladder DAC incorporates MOS switches as resistors in a secondary ladder. The diagram below shows how the secondary ladder slides up and down along the primary one. Is this DAC monotonic for any value of the MOS on-resistance, R_{on}? Why or why not? Use detailed analysis to support your claim. (5)



x, y are the same point but in two diff. situations :

$$V_x = \frac{(j-1)\,r + r\,//(n\,R_{on})}{(n-1)\,r + r//(n\,R_{on})} \quad , \quad V_y = \frac{j\,r}{(n-1)r + r\,//\,n R_{on}}$$

to be monotonic $\rightarrow$ $V_x \le V_y$

$\therefore$ $(j-1)r + r\,//(n\,R_{on}) \le j\,r$

$\rightarrow$ $r\,//\,(n\,R_{on}) \le r$ which is always true for any value of R_{on}.

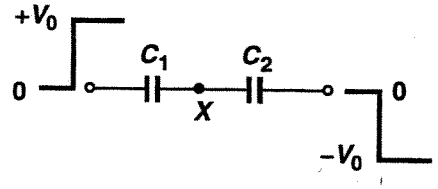
$\rightarrow$ This DAC is unconditionaly monotonic for any value of R_{on}.

3. Consider the two nominally-equal capacitors shown below. The initial condition at node X is zero.

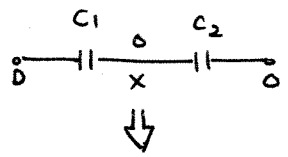
(a) Assuming each capacitor can be expressed as $C = C_0(1 + \alpha_1 V)$, determine the value of V_X after the transitions shown in the figure occur.

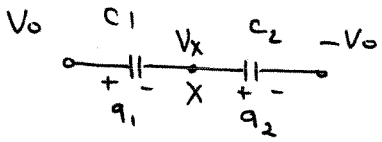
(b) Repeat part (a) if $C = C_0(1 + \alpha_1 V + \alpha_2 V^2)$.

(5)



(a)





$C = C_0(1+\alpha_1 V)$

from conservation of charge $\rightarrow$ $q_1 = q_2$

$$\therefore \int_0^{V_0 - V_x} C_1\, dv_1 = \int_0^{V_x - (-V_0)} C_2\, dv_2$$

$$\therefore C_0\left((V_0 - V_x) + \frac{\alpha_1}{2}(V_0 - V_x)^2\right) = C_0\left((V_x + V_0) + \frac{\alpha_1}{2}(V_0 + V_x)^2\right)$$

$$\therefore 2(\alpha_1 V_0 + 1) V_x = 0 \rightarrow \boxed{V_x = 0}$$

(b) if $C = C_0(1 + \alpha_1 V + \alpha_2 V^2)$

similarly,

$$\therefore C_0\left[(V_0 - V_x) + \frac{\alpha_1}{2}(V_0 - V_x)^2 + \frac{\alpha_2}{3}(V_0 - V_x)^3\right] = C_0\left[(V_x + V_0) + \frac{\alpha_1}{2}(V_x + V_0)^2 + \frac{\alpha_2}{3}(V_x + V_0)^3\right.$$

$$\therefore V_x\left(1 + \alpha_1 V_0 + \alpha_2 V_0^2 + \frac{\alpha_2}{3} V_x^2\right) = 0$$

$$\therefore \boxed{V_x = 0} \quad \text{or} \quad V_x^2 = -\frac{3}{\alpha_2}(1 + \alpha_1 V_0 + \alpha_2 V_0^2)$$

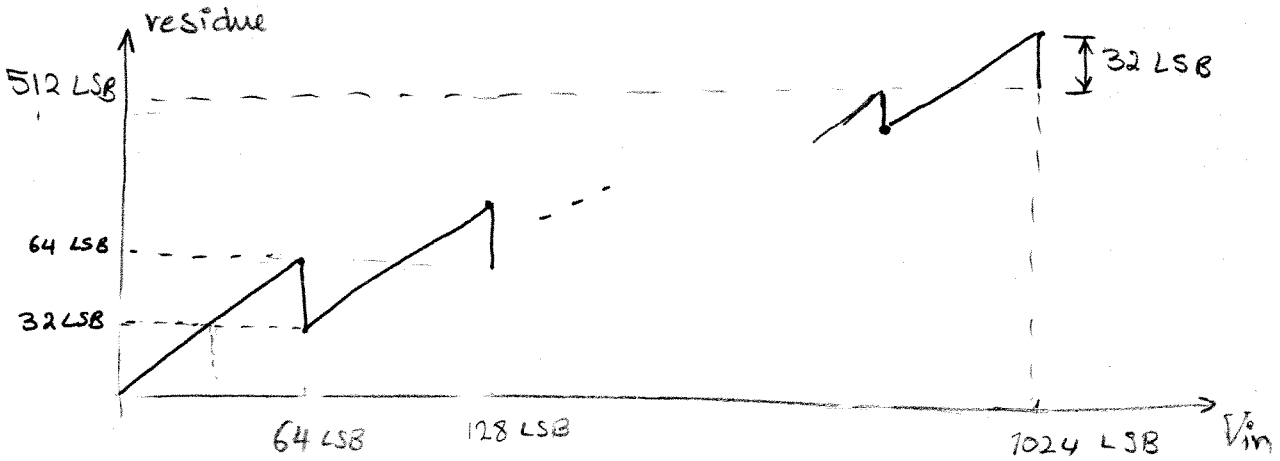
4. Consider a 10-bit two-step ADC similar to that in Homework #4. Each stage resolves 5 bits and the subtractor has a voltage gain of unity. The reference voltage for the first-stage ladder is nominally equal to 1024 LSB and that for the second-stage ladder equal to 32 LSB.

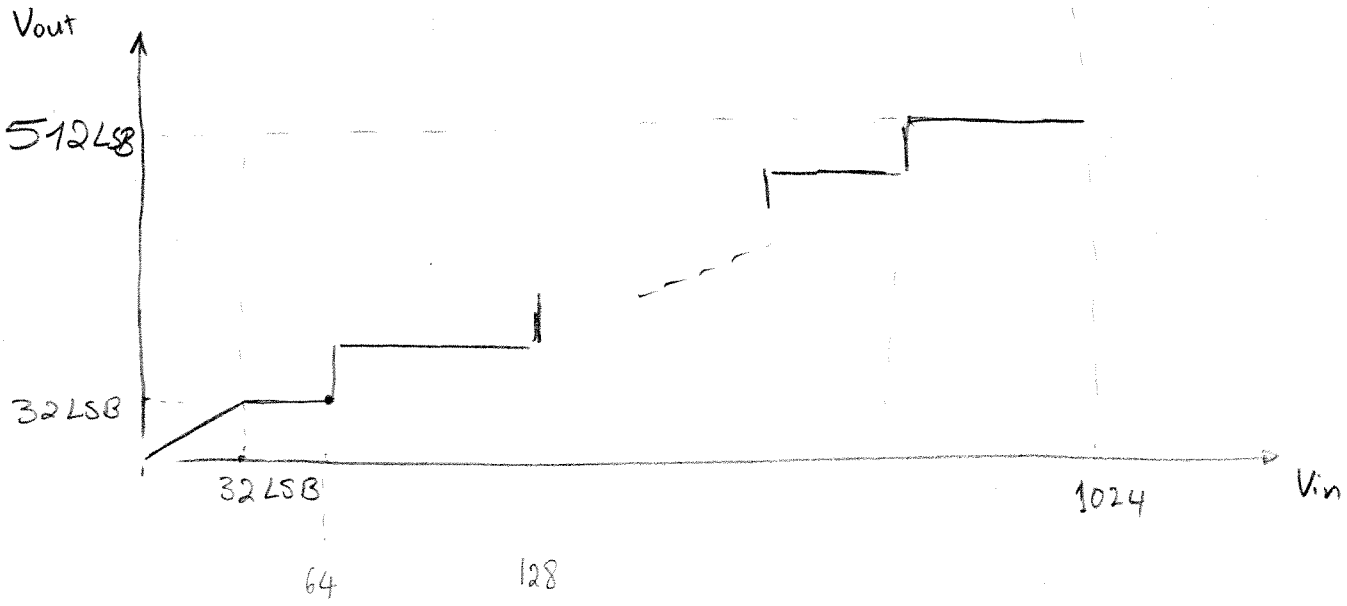
(a) Suppose the reference voltage for the first-stage ladder is accidentally chosen to be 2048 LSB but that for the second stage is still equal to 32 LSB. Plot the residue and the overall input-output characteristic and determine critical errors. Assume DAC output varies between 0 and 1024 LSB.

(b) Suppose the reference voltage for the second-stage ladder is accidentally chosen to be 64 LSB but that for the first stage is still equal to 1024 LSB. Plot the residue and the overall input-output characteristic and determine critical errors.

(5)

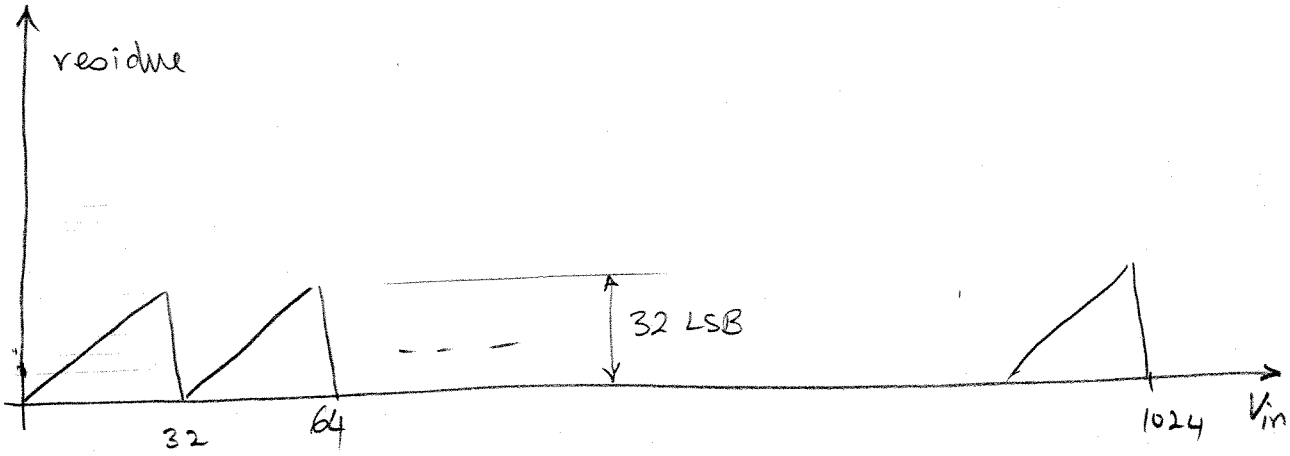
(a) If the reference voltage of 1st stage is 2048 LSB





DNL = 32 LSB

(b) ref. voltage of the 2nd stage ladder = 64 LSB



DNL = 1 LSB