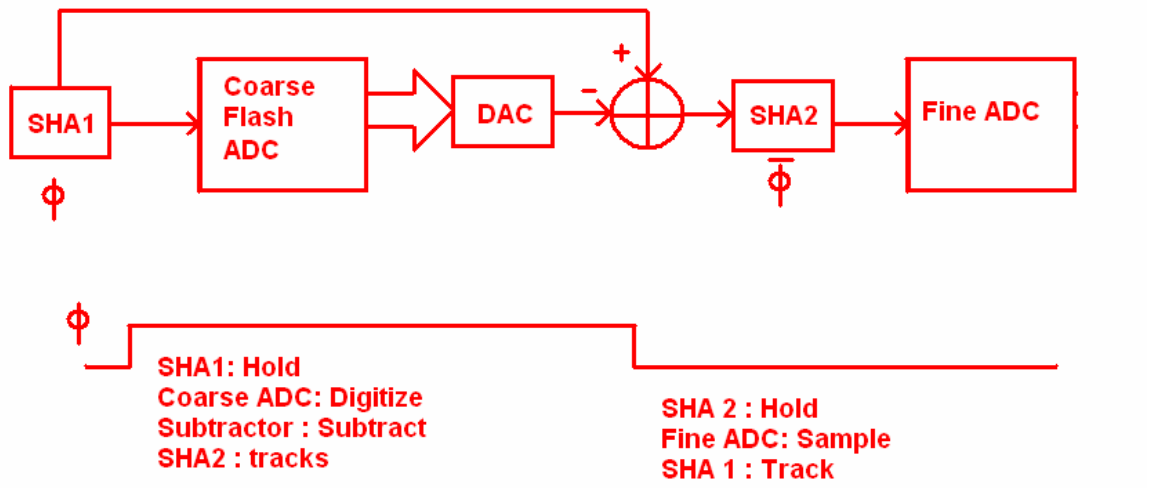
Pipelined ADC Architectures

General Pipelined System

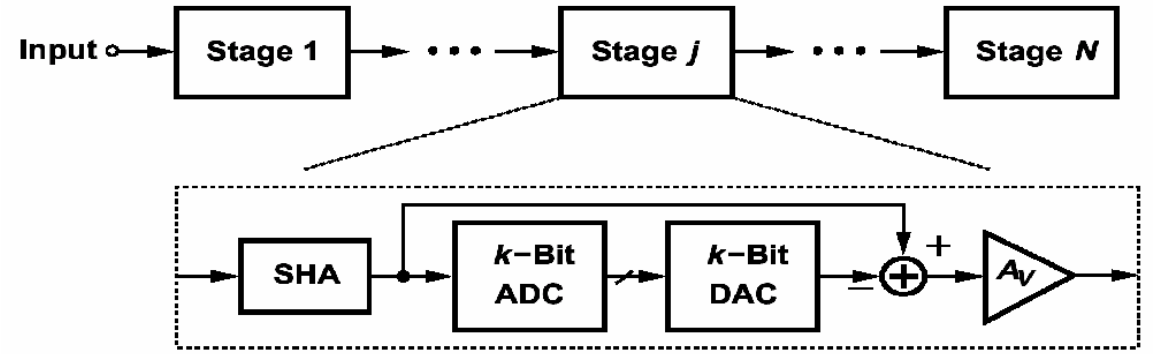
Each stage performs an operation on the signal, provides the output for the following sampler, and, once the sampler has acquired the data, begins the same operation on the next signal.

- **Different stages process different samplers concurrently.**
- **Throughput rate depends on only the speed of each stage (and the acquisition time of the next sampler).**

Example: Two-Step Pipelined ADC



General Pipelined ADC

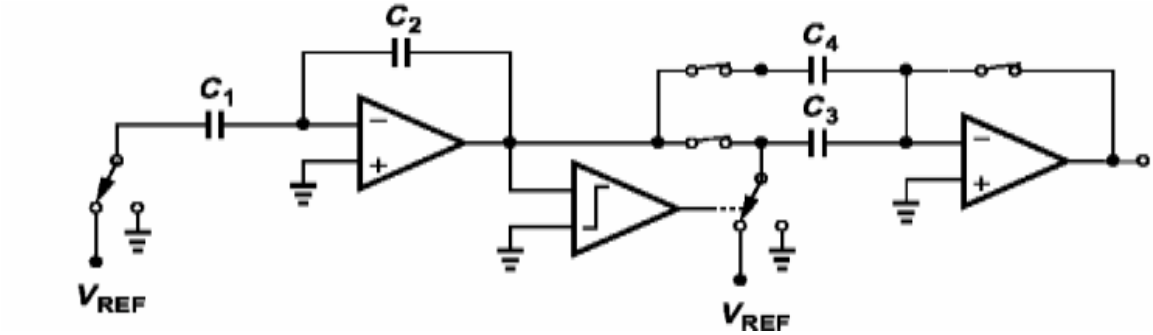


Important Notes:

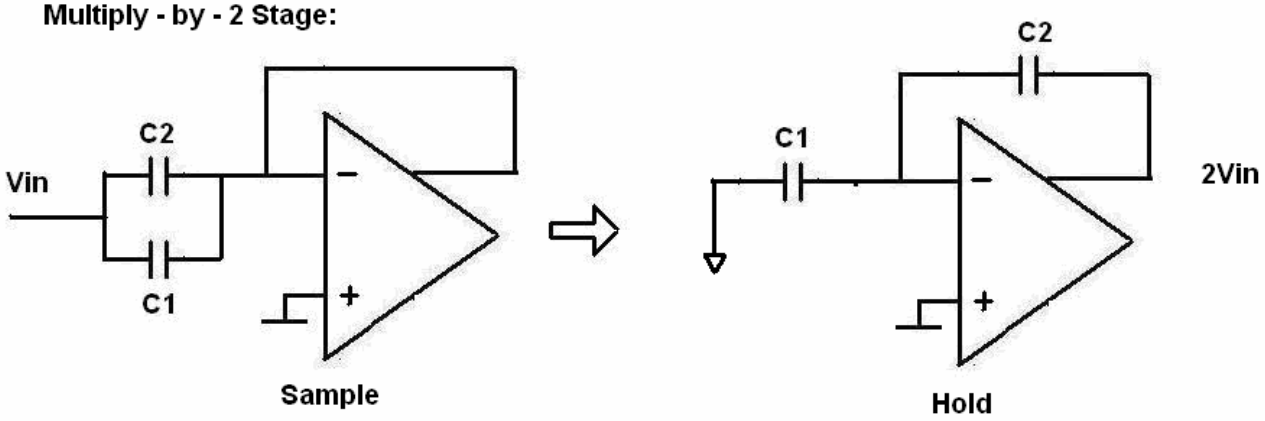
1. **Pipelined architectures are especially efficient if several of these operations can be combined.**
2. **Old wisdom has it that their area and power dissipation grow almost linearly with the number of bits:**

3. **Need gain between stages to avoid corrupting the data.**
4. **Actual implementations vary from cascaded flash stages to one-bit-per-stage sopologies.**

Example: One-bit-per-stage Architecture



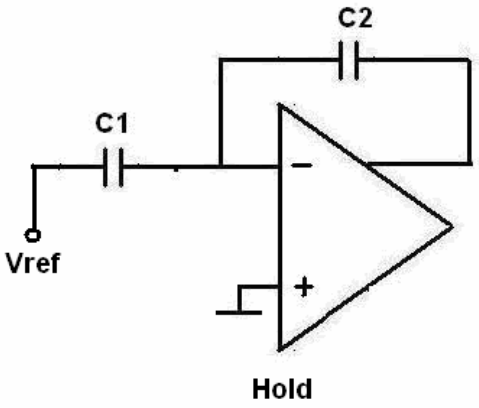
Multiply - by - 2 Stage:



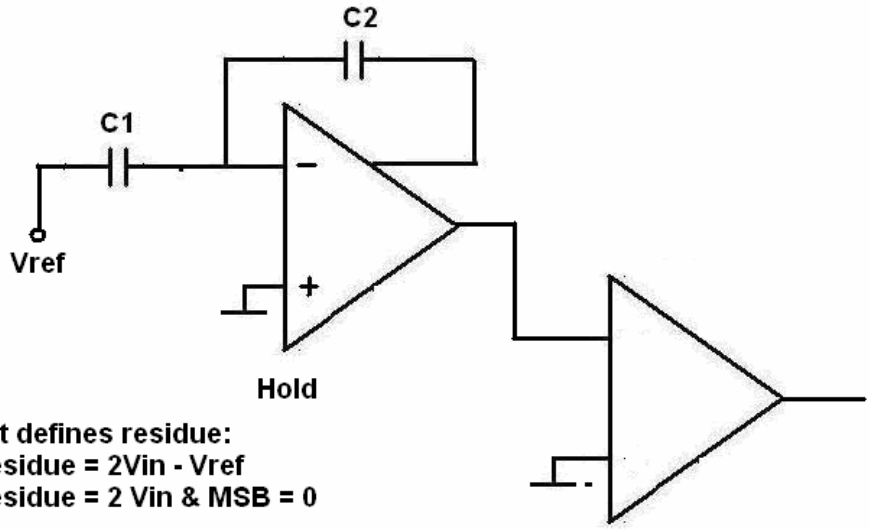
C1 will carry its own charge and charge of C2
Faster than earlier circuit because of higher loop gain

Subtract:

Bringing C2 to Vref instead of to ground during Hold. (i.e. instead of (2Vin - 0), we have (2Vin - Vref))



Add a comparator:



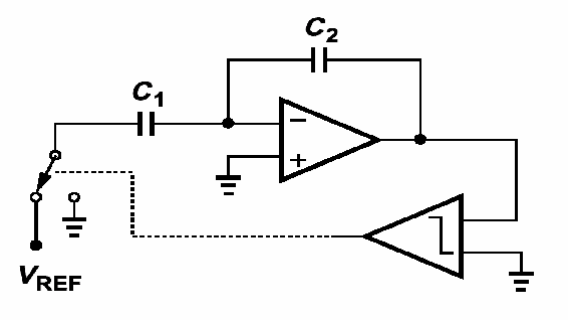
Comparator output defines residue:
If 2Vin - Vref > 0, residue = 2Vin - Vref
If 2Vin - Vref < 0, residue = 2 Vin & MSB = 0

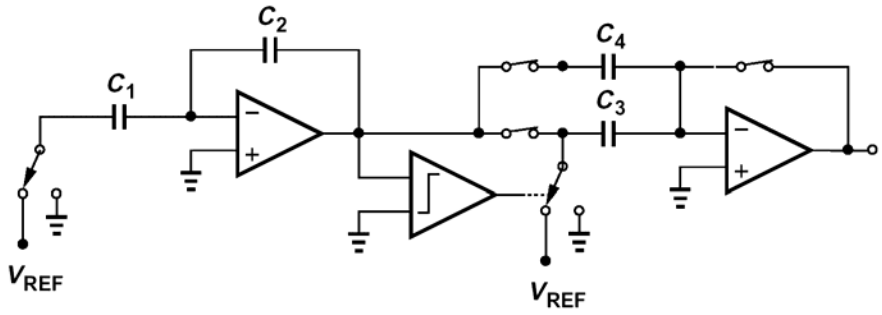
Note: Rather than subdivide the reference by means of DAC, here we amplify the input by a factor of 2.

Pros and Cons:

- Simple and modular design: one op amp, one comparator
- Gain of two relaxes design of subsequent stages.
- But comparator offset must be small.
- Speed limited by op amp design.

Feedback vs. Feedforward:





(Song, JSSC, Dec. '88)

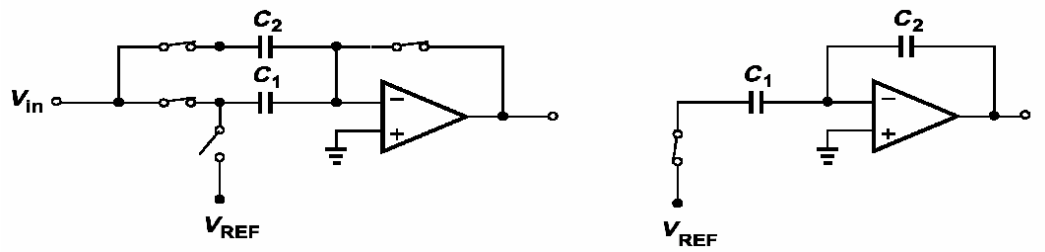
Effect of Nonlinearities:

All the sources of error discussed for two-step architectures are significant here as well. Analyzing multi-step ADCs becomes more difficult when all of these effects must be taken into account.

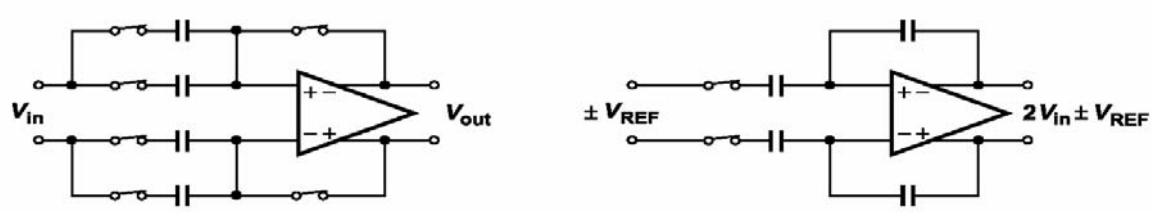
Particularly important are: op amp gain, offset, kT/C noise, nonlinearity, capacitor matching, and switch charge injection mismatch. Comparator offset is also important in the first few stages, but we often use overlap and digital correction (Ch. 8) to relax this constraint.

Residue Plot for Fully-Diff. Realization:

Op Amp Offset:

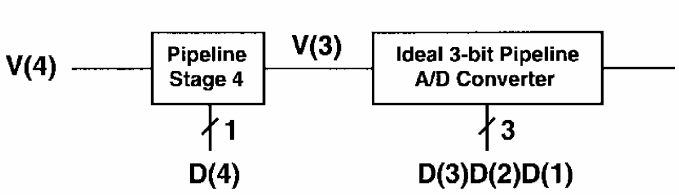


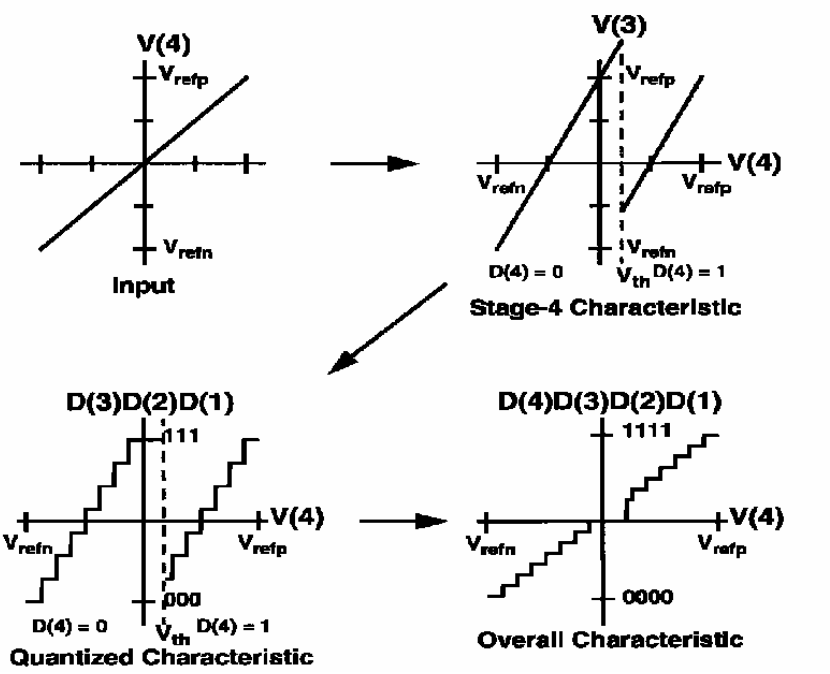
Charge Injection Mismatch:



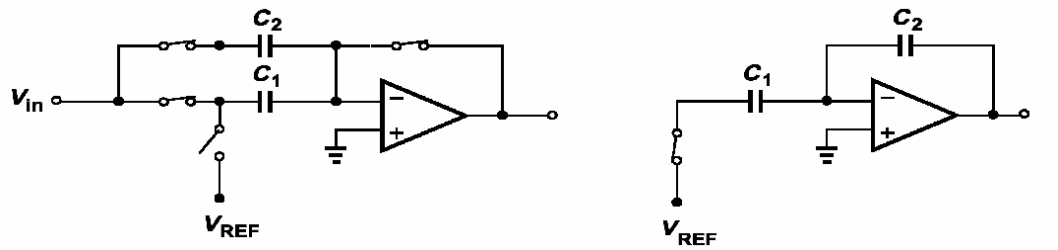
Residue Behavior:

Detailed View: [Ingino, JSSC, Dec. 98]

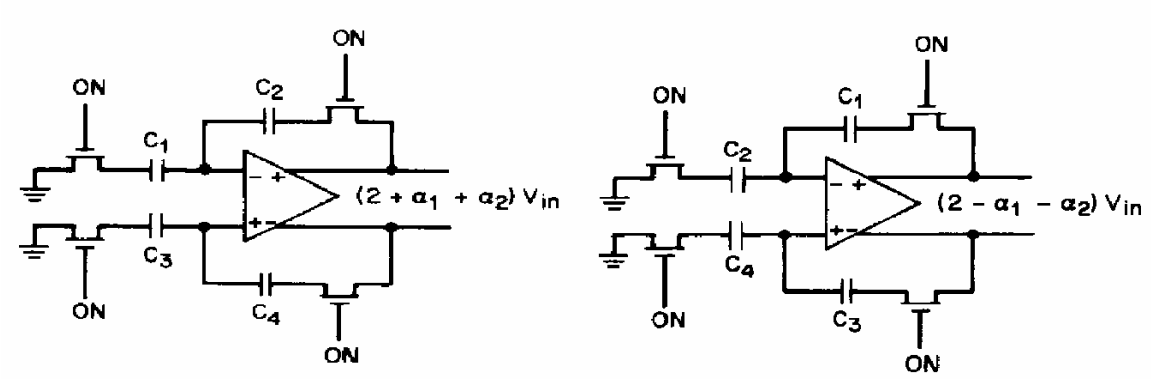




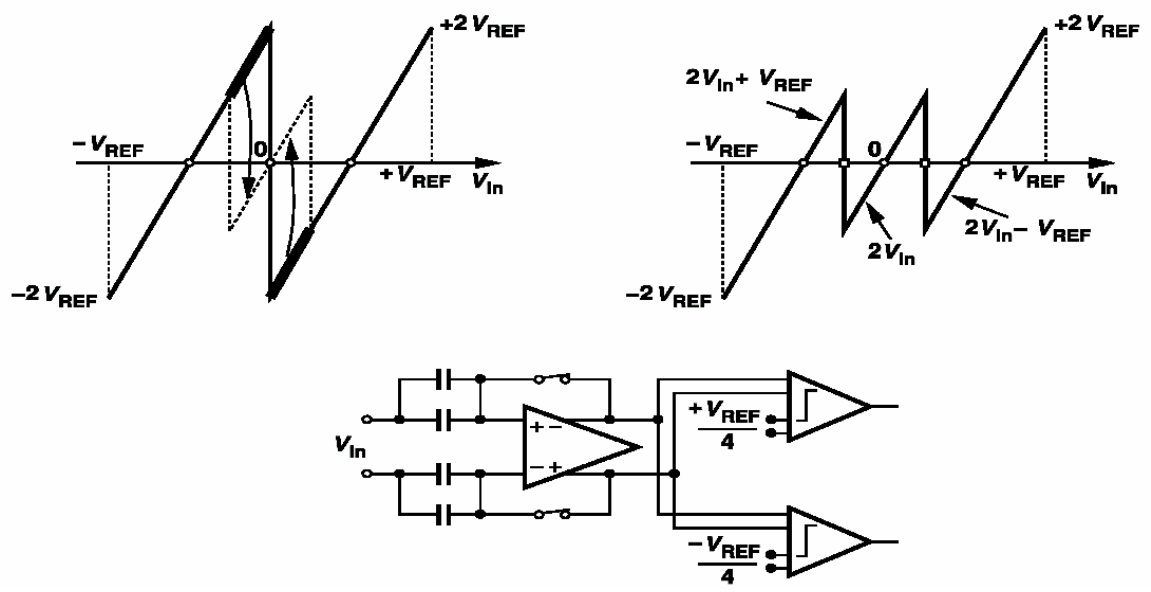
Effect of Capacitor Mismatch:



Capacitor Averaging: [Song, JSSC, Dec. 88]



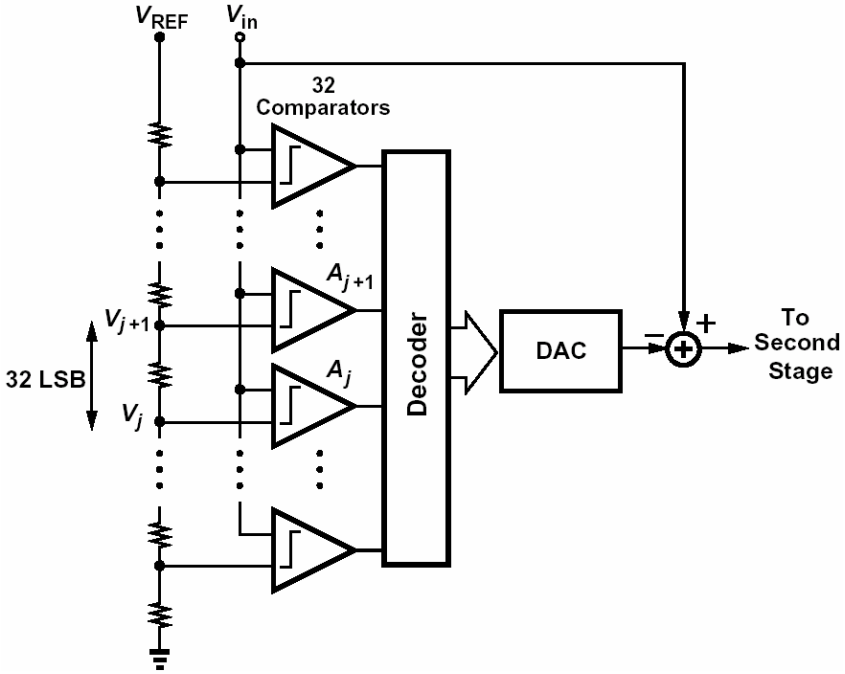
1.5-Bit-Per-Stage Architecture



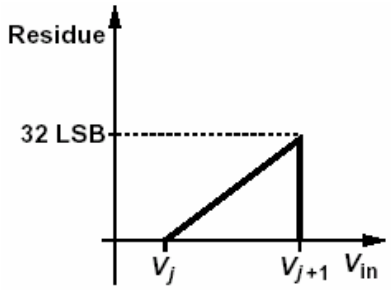
- Corrects for comparator offset, op amp offset, and charge injection mismatch.

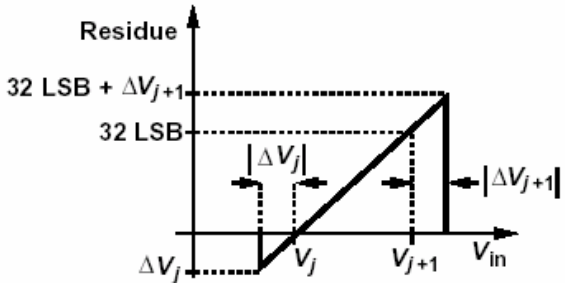
Overlap and Digital Correction

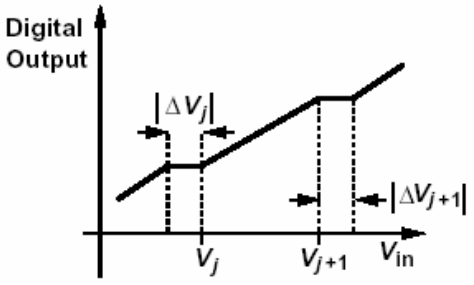
In analyzing two-step ADCs, we noted that almost every nonideality had to be less than 0.5 LSB if the overall DNL were to remain < 0.5 LSB. (In practice, many of these errors add up. Each one must be even less.)



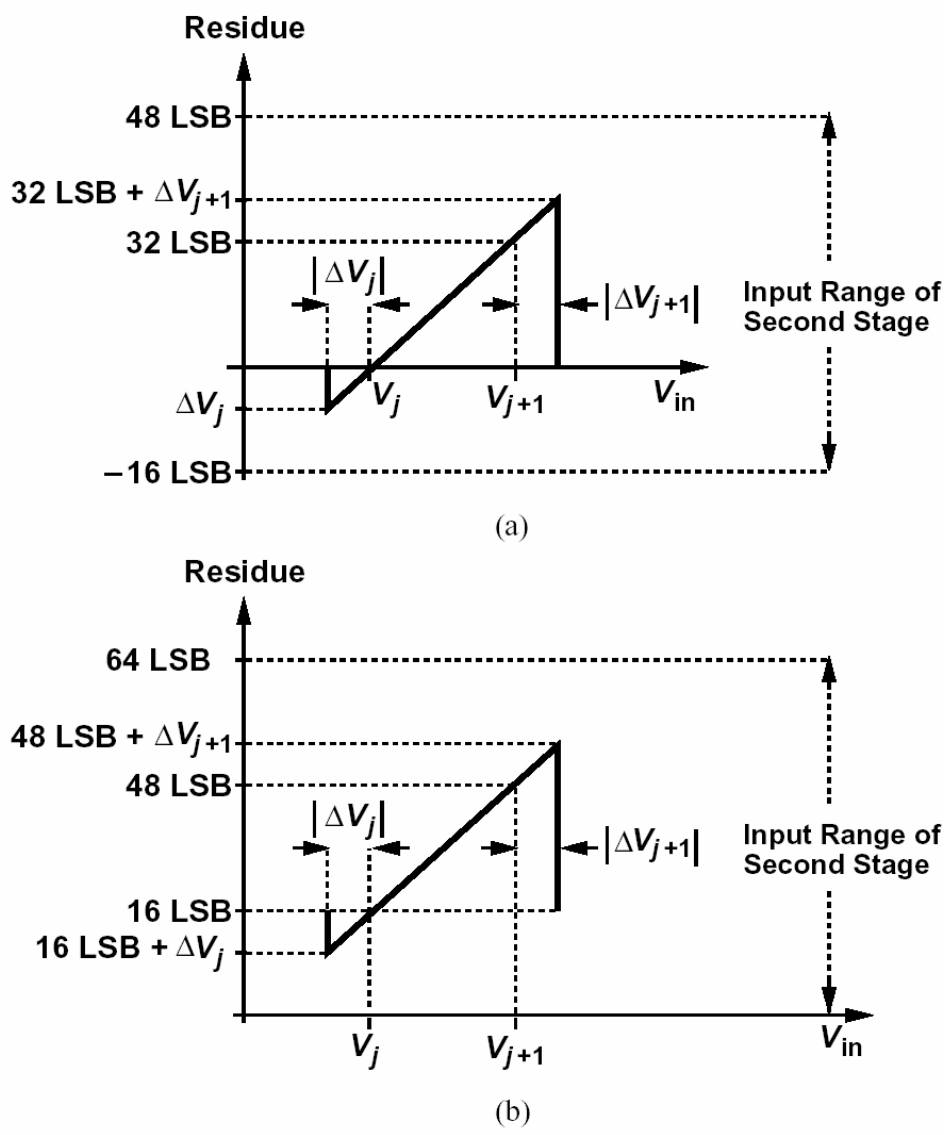
To avoid these errors, we design the second stage so that it accommodates both the underrange and the overrange. In other words, we add redundancy to the second stage.







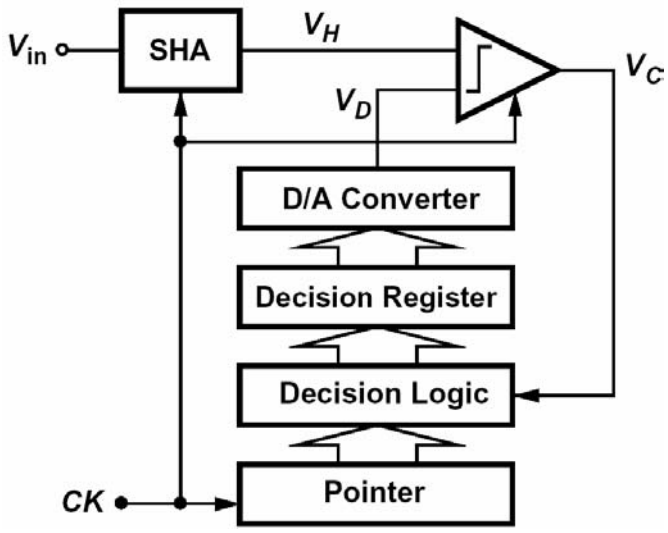
This can be accomplished in two ways:



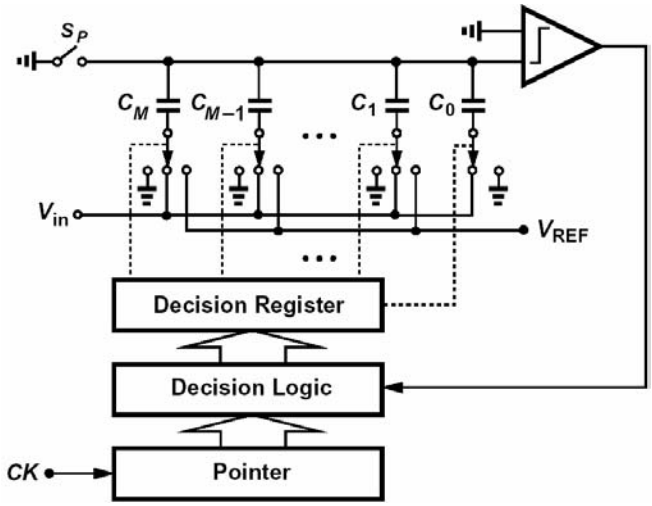
Which errors cannot be corrected with the above technique?

SAR ADCs

Successive Approximation



SAR with Charge Redistribution:



Reduction of Capacitor Spread: