EE 215D B. Razavi

Spring 12 HO #9

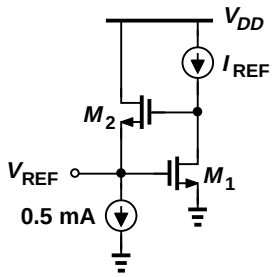
Homework #3

Due Tue., May 1, 2012

1. In this problem, we study the effect of a nonideal voltage reference upon the settling behavior of a 4-bit segmented capacitor DAC. The circuit topology is as shown in Fig. 4.23 of the text. Assume each switch has a $W/L = 8\ \mu$m$/0.18\ \mu$m, each capacitor is 0.4 pF, and the supply voltage is 1.8 V. Instead of the reset switch, simply set the initial condition to zero.

(a) If the reference voltage is ideal and equal to 0.9 V, what is the worst-case simulated settling time to 0.5 LSB in a 10-bit system?

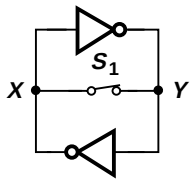
(b) Suppose the reference is generated using the following circuit. (This is not a good way because the output depends on the temperature and process.) Assume $(W/L)_{1,2} = 40\ \mu$m$/0.18\ \mu$m and calculate I_{REF} such that $V_{REF} = 0.9$ V. What is the small-signal output impedance of the circuit? What would this suggest about the worst-case settling time of the above DAC if it uses this reference?



(c) Simulate the DAC with the above reference generator and measure the settling time. Explain the discrepancy between this result and the estimate in (b).

(d) Suppose V_{REF} is provided externally from an ideal source but with 2 nH of series inductance. What is the settling time in this case? Add a resistor in series with the inductance and see how much you can improve the settling.

2. Consider the cross-coupled CMOS inverters shown below. The supply voltage is 1.8 V and for all the MOS devices, $W/L = 12\ \mu$m$/0.18\ \mu$m. To simplify the problem, model S_1 as an ideal switch with an on-resistance of 800 Ω.



(a) Calculate the small-signal regeneration time constant, τ_R, of the circuit after S_1 turns off.

(b) Simulate the circuit with $V_{XY}(t = 0) = 2$ mV and 4 mV. What is τ_R? Explain how you measure it. What is the time required for each output to reach within 0.2 V of the supply rails?

(c) Repeat (b) with $W/L = 24\ \mu$m$/0.18\ \mu$m. What is the percentage change in τ_R? What is the percentage change in the power dissipation when S_1 is on?