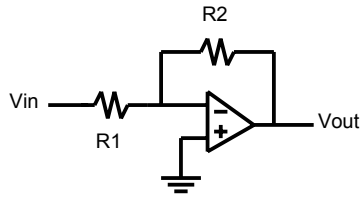
Introduction to Sampled-Data Circuits

Motivation

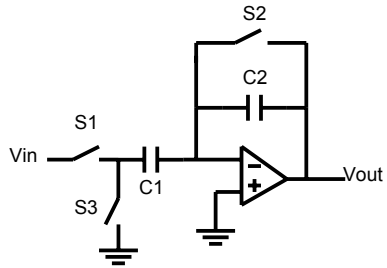
In the resistive feedback circuit shown below:



- **R_1 loads preceding stage;**
- **R_2 loads the op amp;**
- **R_1 introduces substantial thermal noise;**
- **Can't "freeze" (sample) the input.**

Furthermore, in continuous-time filters the location of poles and zeros depends on the absolute value of resistors and capacitors.

Now consider the following circuit:



- **At the instant when S_1 turns off, the value of V_{in} is sampled.**

CMOS is especially suited to sampled-data applications because it provides:

- **"zero-offset" switches**
- **High input impedance.**

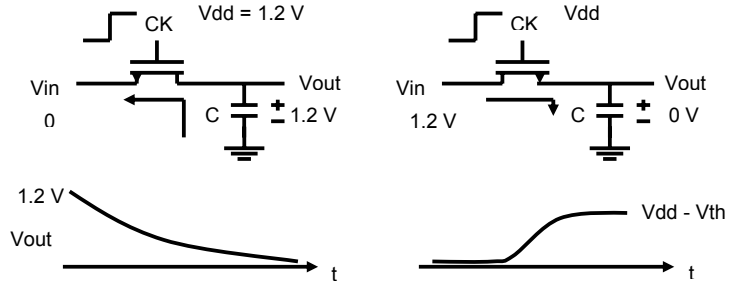
Sampling Switches

An NMOS or PMOS transistor can operate as a switch because:

- **It can be <u>on</u> with <u>zero current</u>.**
- **Its source and drain voltage is not "pinned" to the gate voltage.**

A bipolar transistor is simply not a good sampling switch if used in saturation.

Now consider two cases:



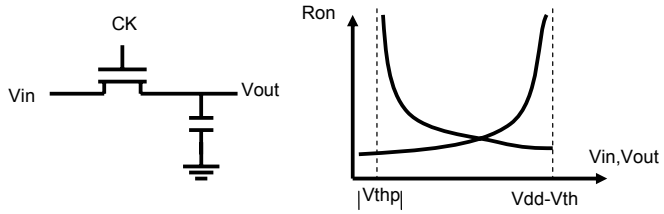
The switch can pass current in <u>both</u> directions. In the steady state, V_{out} "tracks" V_{in} (and the switch acts as a resistor).

What is the on-resistance of the switch?

Switch Nonidealities

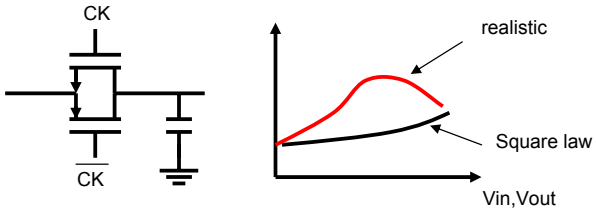
- **On-Resistance**

What happens as the input and output voltages become more positive?



Note that unlike in cascode stages, V_{TH} limits the swing here.

➔Use complementary switches:



The mid-supply range is still troublesome at low supply voltages.

- **Clock Feedthrough and Charge Injection**

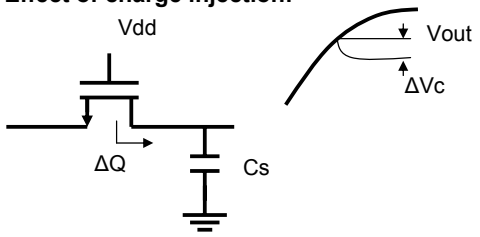
When a MOSFET is on, it carries charge in the inversion layer"

$$Q_{ch} \approx WL_{eff} C_{ox} (V_{GS} - V_{TH})$$

Upon turnoff, this charge exits the channel.
How does the charge split between source and drain?

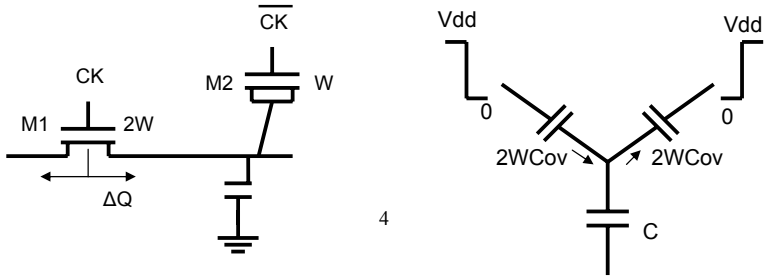
Important Note: Since it is difficult to calculate or control the amount of channel charge that does either way, we must design the circuit to be immune to this effect.
Also, most versions of SPICE have a very poor model of charge injection.

Effect of charge injection:



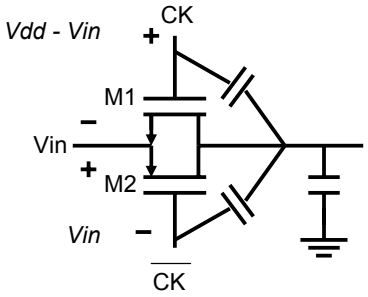
➔To reduce the effect of clock feedthrough and charge injection, need to make the switch <u>smaller</u> or the sampling capacitor <u>larger.</u> ➔ Trade-off between speed and precision

- **Cancellation Techniques**
  1. **Dummy Switch: M_1: 2W/L M_2:W/L**



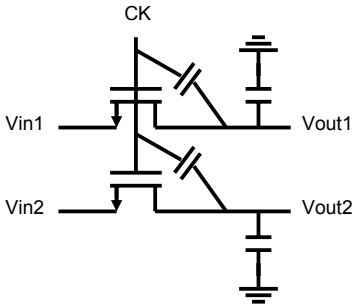
With perfect matching, clock feedthru is cancelled. But charge injection may not be.

2. Complementary Switches

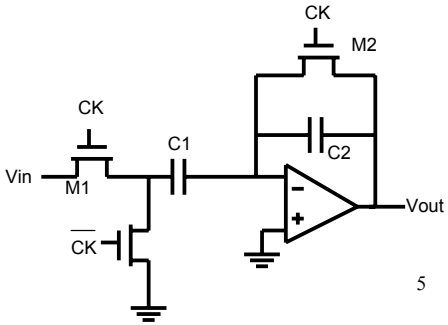


Neither feedthrough nor charge injection is fully cancelled.

3. Differential Sampling

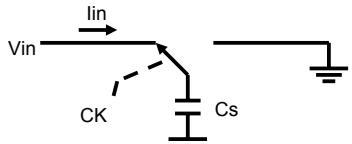


4. "Bottom Plate" Sampling

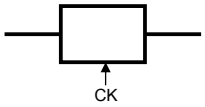


Other Examples of SC Circuits:

1. "Resistor"

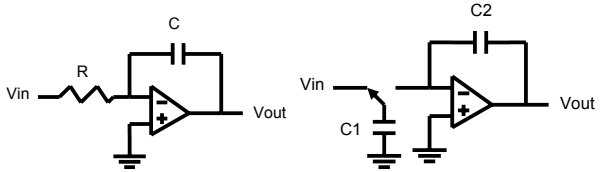


If every T seconds, C_s charges to V_{in} and discharges to ground, the average current is: $I_{in} = C_s V_{in}/T$. Thus, the circuit can be viewed as a resistor equal to:



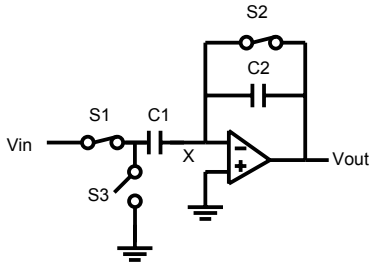
2. Integrator

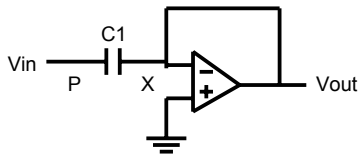
Continuous-Time **Discrete-Time**

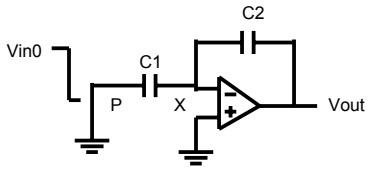


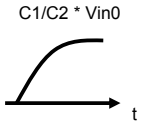
Better discrete-time integrators will be described in the context of oversampling converters.

Noninverting Amplifier

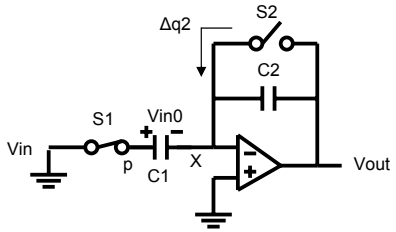




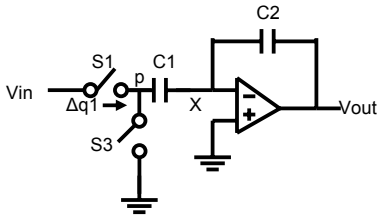


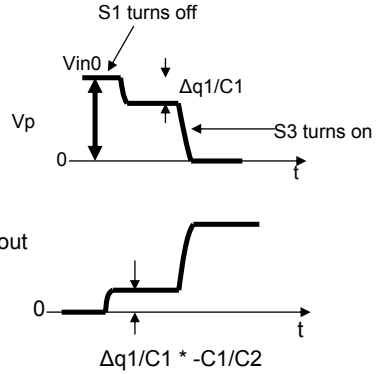


Charge Inj. of S_2:

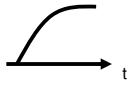


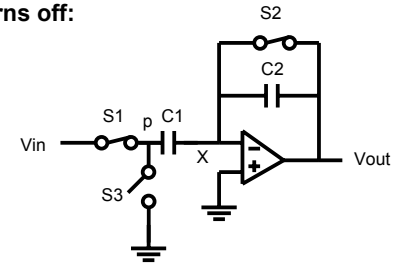
Charge Inj. of S_1:





Effect of change in V_{in} after S_2 turns off:

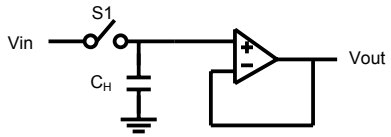




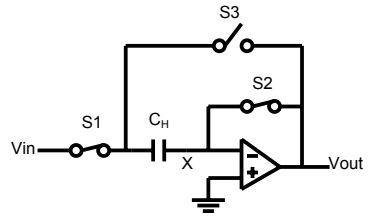
Typical cap. Structure:

Unity-Gain Sampler

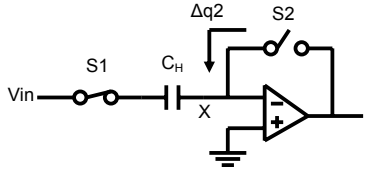
Simple Unity-Gain Sampler

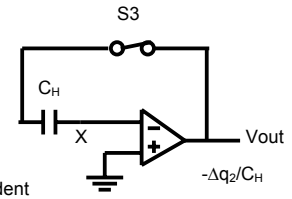


Better Unity-Gain Sampler



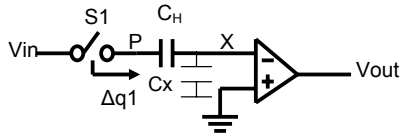
Charge Injection of S_2:



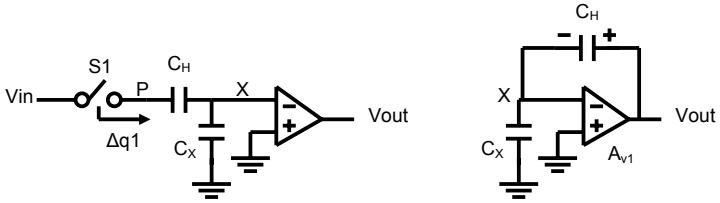


No input dependent

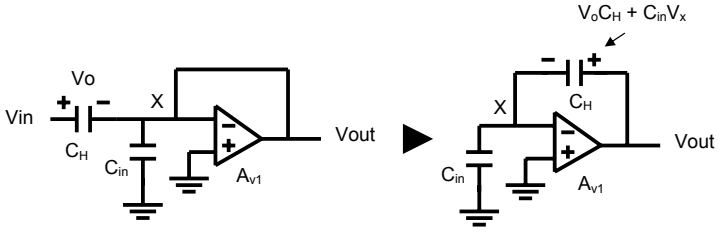
Charge Injection of S_1:
Method I:



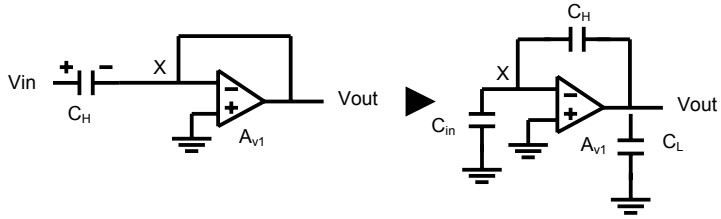
Method II:



Precision Considerations



Speed Considerations



$$\frac{\mathbf{Vout}}{\mathbf{Vs}}\mathbf{(s)} = \mathbf{Ro}\frac{\mathbf{(Gm + C_{in}*s)}}{\mathbf{Ro(C_LC_{in} + C_{in}C_L + C_HC_L)*s + GmRoC_H + C_H + C_{in}}} \quad (12.48)$$

Note that for s = 0, (12.48) reduces to a form similar to (12.41). Since typically $GmRoC_H >> C_H$, C_{in}, we can simplify (12.48) as

$$\frac{Vout}{Vs}(s) = \frac{(Gm + C_{in}*s)\,C_H}{(C_LCin + CinC_L + C_HC_L)*s + GmC_H} \quad (12.49)$$

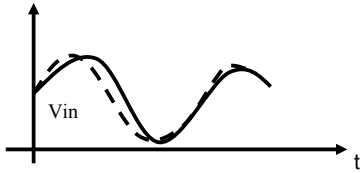
Thus, the response is characterized by a time constant equal to

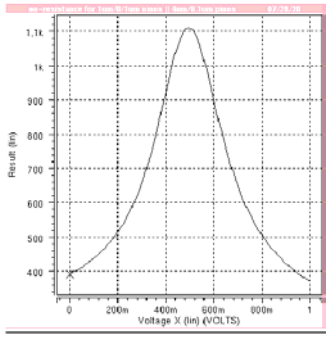
$$T_{amp} = \frac{(C_LCin + CinC_L + C_HC_L)}{GmC_H} \quad (12.50)$$

Other Sampling Nonidealities

MOS Switches

- **Variation of On-Resistance with Input**

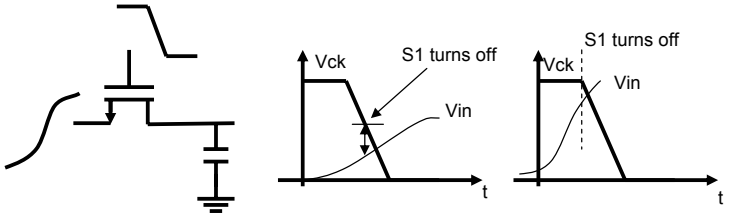




➔ **Creates harmonic distortion.**

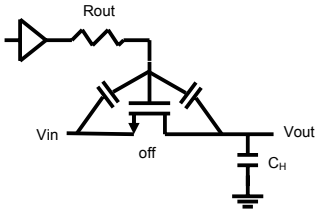
- **Input-Dependent Sampling Instant**

A MOS device turns off when $V_{GS} < V_{TH}$. If the clock transition time is nonzero, then the exact time at which the switch turns off depends on the input level:



➔ **Creates harmonic distortion.**

- **Hold-Mode Feedthrough**

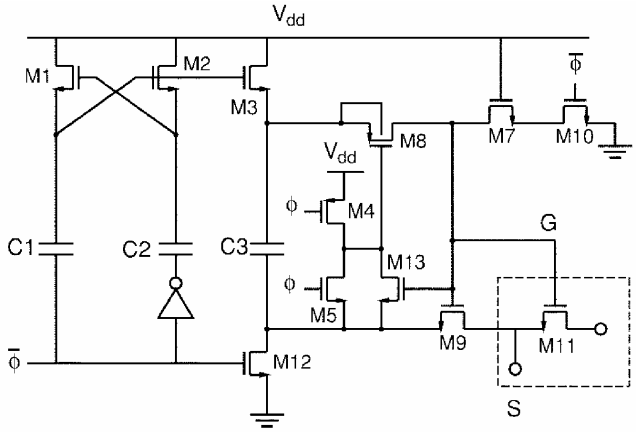


$$\left.\frac{V_{out}}{V_{in}}\right|_{hold} = \frac{C_{ov}}{C_H}\frac{R_{out}C_{ov}s}{2R_{out}C_{ov}s+1}$$

Switch Bootstrapping

Basic Idea:

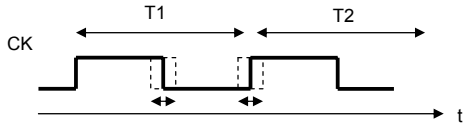
Realization (Abo, JSSC, May 99):



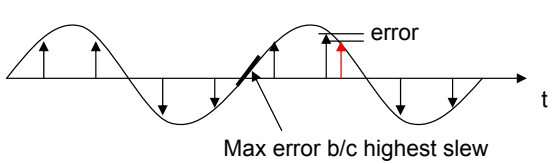
Operation Details:

Clock Jitter

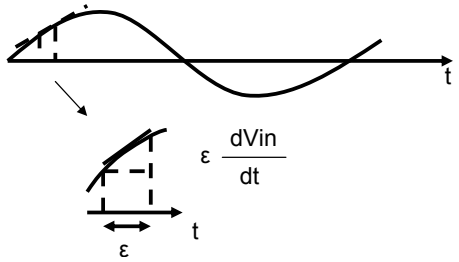
- **Jitter is the random time variation in the clock transitions.**



- **Effect of Jitter on SNR**



Jitter makes uniform sampling non-uniform.



$$Vin = A \sin 2\pi f_{in} t$$

$$n(t) = \varepsilon \frac{dVin}{dt}$$

Since ε is random, ε d V_{in} / dt appears as additive noise at the output.

Correction: In Eq. (2.29), change T_s to $T_{in} = 1/f_{in}$.

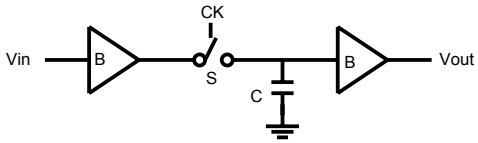
Example

What is the jitter requirement for Bogner's 14-bit 100-MHz A/D converter?

For an ideal 14-bit converter: SNR ≈ 86 dB. Let's say the SHA has the same SNR (which means the overall system will have an SNR of 83 dB). Then:

Sample-and-Hold Architectures

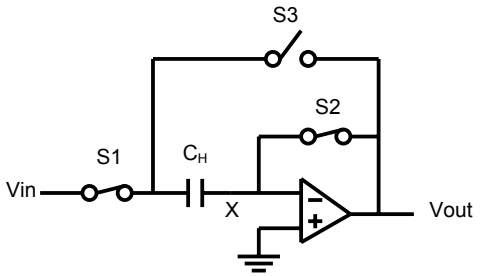
Conventional Open-Loop Architecture



- **Most suitable for high-speed applications with S implemented as a diode bridge**
- **B_1 and B_2 directly contribute nonlinearity.**

Example: Source-Follower Buffers:

Switched-Capacitor Architecture



(2)

Acq. Mode **Hold Mode**

- **The dominant sample-and-hold technique in CMOS technology. Simple and relatively efficient.**
- **S_1 introduces input-dependent delay ➔ its on-resistance must be small.**
- **In CMOS, op amp A is actually a transconductance amplifier G_m.**
- **Linearity of op amp determines the overall linearity, and its open-loop gain sets the gain error.**