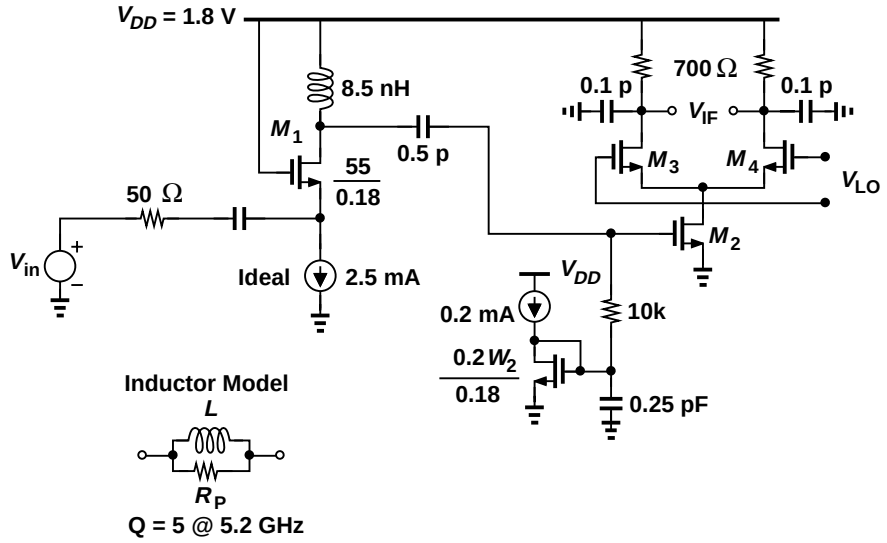
Homework #3

Due Mon., Feb. 1, 2010

In this homework, we study the front end of a simple heterodyne receiver. Part of the circuit is similar to the cascade studied in previous homeworks. All transistors have a channel length of 0.18 μm. For the LO, assume a frequency of 5.13 GHz, a common-mode level of 1.7 V, and a peak-to-peak differential amplitude of 0.9 V.



(a) Determine the width of M_2 to obtain resonance at 5.2 GHz.
(b) Determine the width of M_3 and M_4 to achieve maximum conversion gain, defined as the magnitude of the IF component divided by $V_{in}/2$. What is the voltage conversion gain of the mixer under this condition?
(c) Determine the LO leakage to the antenna and show the leakage path.
(d) Compute the output dc offset if M_3 and M_4 suffer from a threshold mismatch of 15 mV and the LO contains an 6% second harmonic.
(e) Calculate the IP_3 of the first stage and the overall circuit. Which stage would you consider as the IP_3 bottleneck?