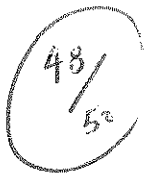
EE 215C
RF Circuits & Systems

H.W. 3



Joung Won Park

(a) Determine the width of M_2 to obtain resonance at 5.2GHz.

Given width of M1, the total parasitic capacitance at the drain of M1 is $C_{ptot} = 41.93fF + 49.16fF = 91.09fF$.

$$5{,}2GHz = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{8.5\times10^{-9}\cdot\left(91.09fF + C_{gs2}\right)}}$$

Therefore, $C_{gs2} = 19.11fF$.

By Cadence simulation, the width of M2 is obtained as 7um for 5.2GHz resonance frequency as shown in figure 1.

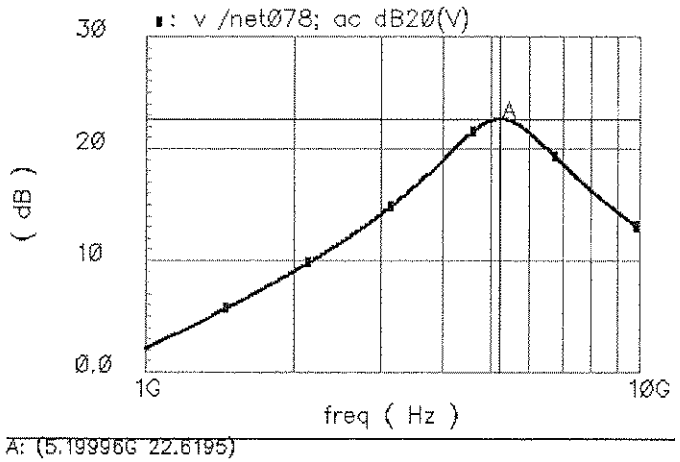


Figure 1. Resonance at 5.2GHz with W_2=7um

With W_2=7um, DC operating point simulation shows that $C_{gs2} = 17.21fF$ which is similar to the hand calculation. The voltage gain is 22.62dB under this condition.

(b) Determine the width of M_3 and M_4 to achieve maximum conversion gain, defined as the magnitude of IF component divided by V_{in}/2. What is the voltage conversion gain of the mixer under this condition?

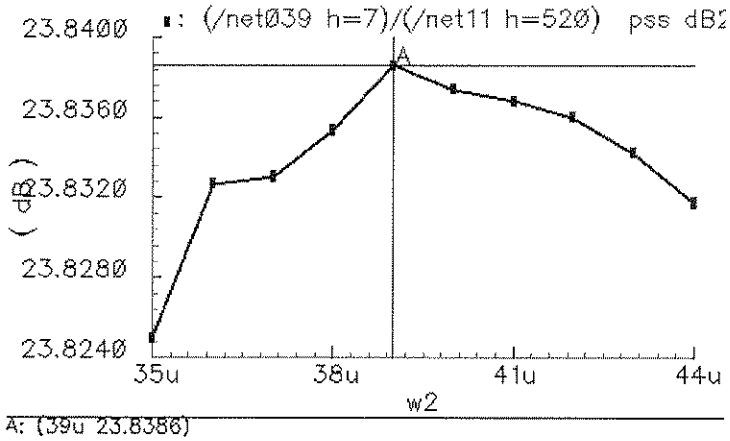


Figure 2. W_3 & W_4 vs. Conversion Gain

Sweeping the size of M_3 and M_4, we can find the optimum width that shows the highest total conversion gain. If the sizes are too small, M_3 and M_4 are not switching completely. That is, M_3 and M_4 are turned on at the same time. Now, one part of the small signal current generated by M_2 goes to M_3 and the other goes to M_4. Since this signal is common mode, they are cancelled at the differential output. This is why we have a small conversion gain when W_3 and W_4 are small.

In the other hand, if W_3 and W_4 are too big, the drain node of M2 suffers from larger capacitance. Thus, we lose a part of the small signal current and it results smaller conversion gain. By sweeping W_3 and W_4, we can find the optimum width is 39um. The voltage conversion gain is 23.84dB

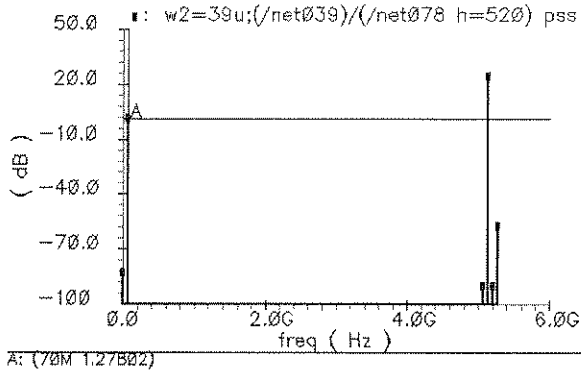


Figure 3. Mixer Conversion Gain

Under this condition, the measured mixer gain is 1.278dB, as shown in figure 3.

(c) Determine the LO leakage to the antenna and show the leakage path

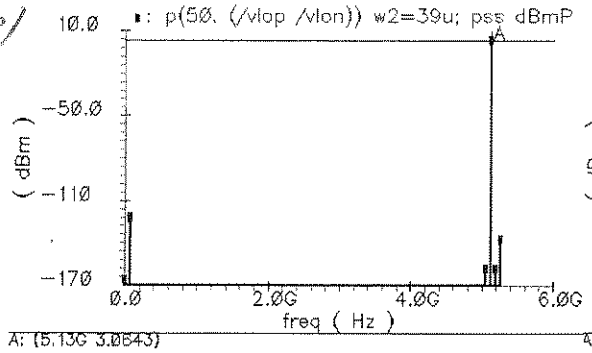


Figure 4. LO power at LO port

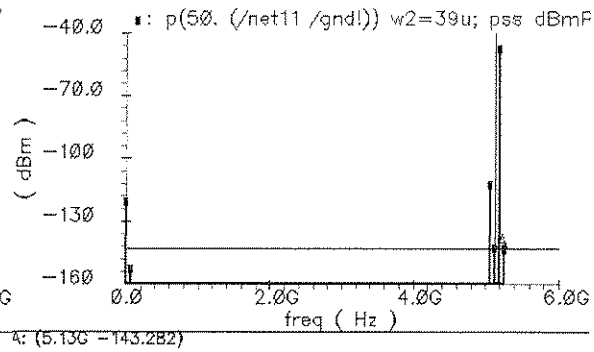


Figure 5. LO power at the input port

Figure 4 and figure 5 represent LO power at the LO port and at the input port respectively. LO power is around 3dBm. It leaks to the input port and shows -143.28dBm power. It is attenuated by -146.3463dB from the LO port to the input port. The high impedance provided by M_1 gives high isolation between LO port and input port. The leakage path is shown in figure 6.

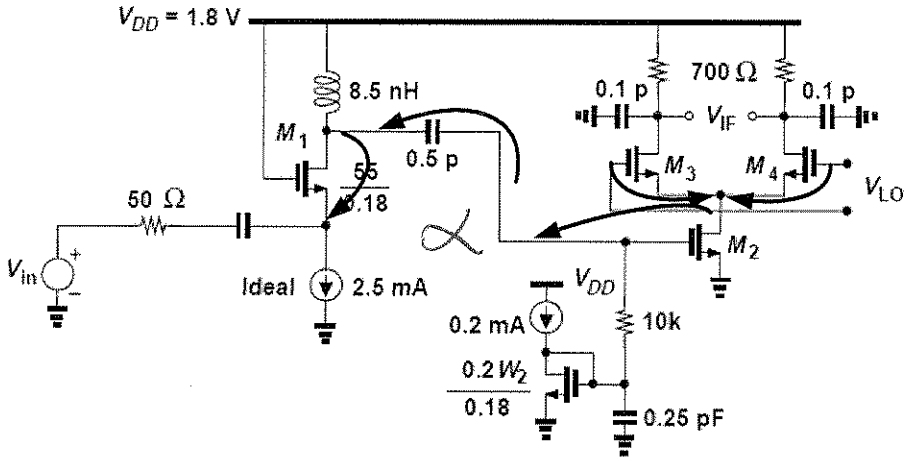


Figure 6. LO leakage path

(d) Compute the output dc offset if M_3 and M_4 suffer from a threshold mismatch of 15 mV and the LO contains a 6% second harmonic.

6% second harmonic means that we have second harmonic power which is 6% of the power of fundamental.

$V_{2nd} = \sqrt{0.9^2 \times 0.06} = 220mV_{p-p}$

2nd harmonic voltage source is attached one side of LO signal. 15mV DC voltage source is attached the other side of LO signal. 15mV and -15mV for the input voltage offset are tested to find the worst case.

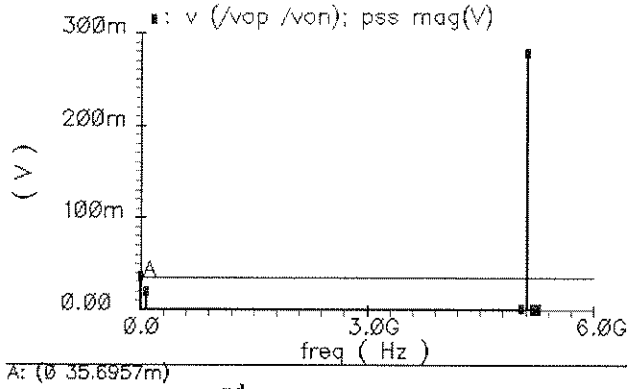


Figure 7. Output DC offset with 2nd harmonic voltage source and 15mV input DC offset

As figure 7 describes, 35.69mV DC offset is generated. 2nd harmonic signal at the LO port is multiplied by the 2nd harmonic at the drain of M_2 to generate DC voltage. Input DC offset 15mV also generates output DC offset at the output.

Interestingly, LO leakage is also increased by a large amount. Since the conditions of M_3 and M_4 are asymmetric, LO leakage from the LO port to the drain of M2 increased. Consequently, a large power of LO leaks to the input port.

(e) Calculate the IP3 of the first stage and the overall circuit. Which stage would you consider as the IP3 bottleneck?

Figure 8 and figure 9 represent the two tone test for the first stage and the total circuit respectively. From figure 8, we can calculate IIP3 of the first stage.

$$P_{IIP3,1} = \frac{P_{out} - P_{IP3}}{2} + P_{in} = \frac{73}{2} - 40 = -3.15dBm$$

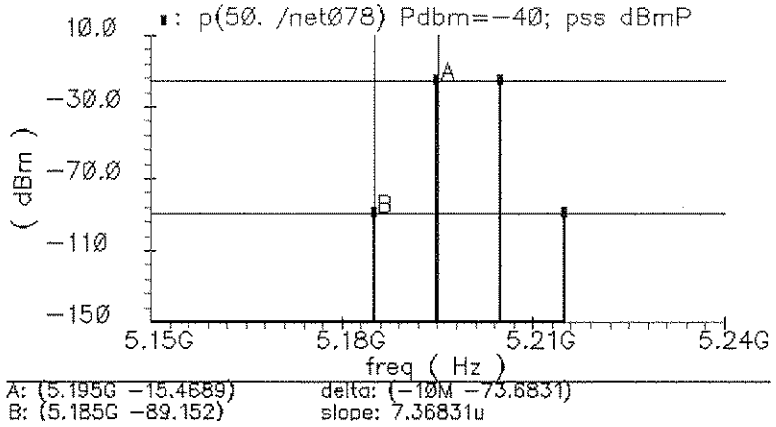


Figure 8. IIP3 of the first stage

Similarly, from figure 9, IIP3 of the total circuit can be calculated.

$$P_{IIP3,total} = \frac{P_{out} - P_{IP3}}{2} + P_{in} = \frac{53}{2} - 40 = -13.5dBm$$

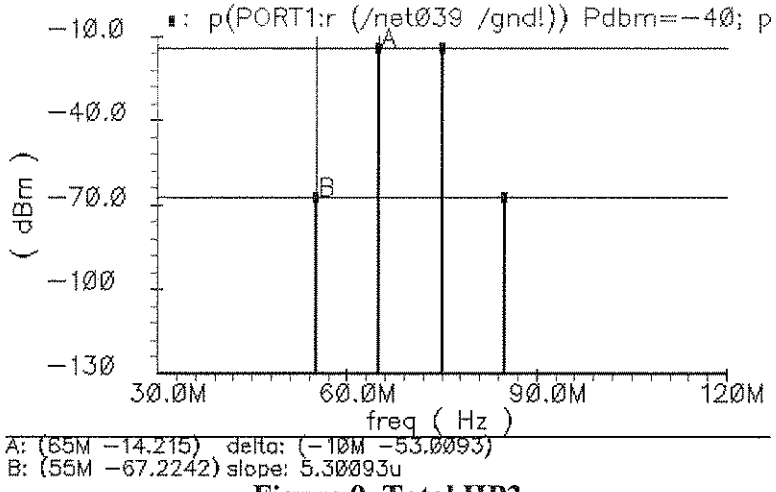


Figure 9. Total IIP3

The bottleneck is the second stage. Since the signal is amplify by 22dB at the first stage, the voltage applied to the gate of M2 is large. While M2 converts the voltage to current, it generates non-linear terms and these terms dominate IIP3 of the total system.