Low-Noise Amplifiers

Design Specs

- **Noise Figure: requires very low noise in the input device. For a simple CS stage, the transistor gm must exceed 1/(25 ohms) if the noise figure is to remain below 2 dB.**

Exercise: calculate the NF if the metal line connecting to the gate has a resistance of Rm.

→ Only one device should dominate NF. → limited number of topologies to choose from.

- **Gain: Must be large enough to minimize noise contributed by mixer. Trades with IP3.**

- **Input Matching:**
  - Do we need conjugate matching at the input?

- Do these concerns pertain to the other stages in the RX chain?

- How do we quantify the matching? The input return loss is defined as 10 log $|\Gamma|^2$, where

$$\Gamma = \frac{Z_{in} - R_0}{Z_{in} + R_0}$$

A return loss of better than 10 dB is considered adequate.

- **Stability: Since the LNA interfaces with the outside world, it must remain stable with almost any source impedance and at <u>all</u> frequencies.**

Traditional microwave design uses the Stern factor to measure stability:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad \Delta = S_{11}S_{22} - S_{12}S_{21}$$

If K>1 and Δ<1, the circuit is unconditionally stable.

- Complications: Since the LNA output is not matched, S22 becomes rather irrelevant

Example: Determine K for a simple CS stage at low frequencies.

Conclusion: We design LNAs with high reverse isolation.

- **Linearity: In most systems, LNAs do not limit the RX linearity. One exception is CDMA.**

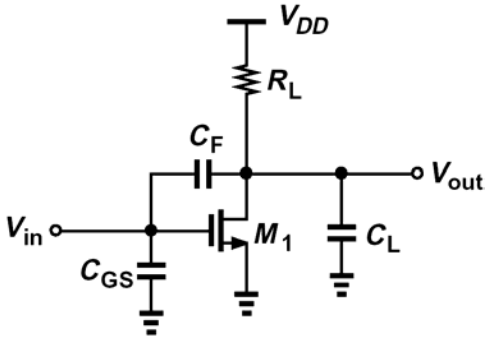
- **Bandwidth: The bandwidth must accommodate the entire band specified by the standard.**

Exercise: An 11a LNA has a 3-dB bandwidth from 5 to 6 GHz. If the LNA load is an inductor, determine the maximum tolerable Q.

Problem of Input matching

- As explained earlier, the input match cannot be created by tying a physical 50-ohm resistor from input to ground.

Exercise: How about tying a parallel inductor that resonates with the input capacitance and also provides a 50-ohm match?



- With Cf, the input resistance does have a real part:

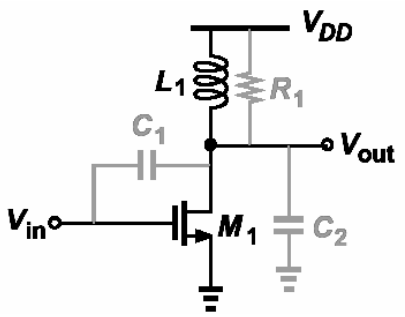
$$Re\{Y_{in}\} = R_L C_F \omega^2 \frac{C_F + g_m R_L (C_L + C_F)}{R_L^2 (C_L + C_F)^2 \omega^2 + 1}$$

$$Im\{Y_{in}\} = C_F \omega \frac{R_L^2 C_L (C_L + C_F)\omega^2 + 1 + g_m R_L}{R_L^2 (C_L + C_F)^2 \omega^2 + 1}$$

But hard to meet other specs.

LNA Topologies

- **CS Stage with Inductive Load**



- Inductor consumes little headroom and resonates with load capacitance.

- The input impedance is given by:

The real part can be obtained as:

$$Re\{Z_{in}\} = \frac{L_1\omega^2[(1+g_mR_1)(C_1+C_2)-C_1]-g_mR_1}{D^2}$$

- Can choose the values to set the real part to 50 ohms. But it goes negative at lower frequencies.

- **CS Stage with Resistive Feedback**

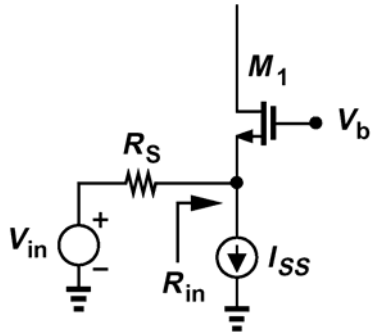
Can obtain an input resistance of 50 ohms, but the input transistor may be very large and its input capacitance cannot be canceled easily.

Exercise: Calculate the noise figure at low frequencies if input is matched.

- **Common-Gate Stage**

The low input impedance proves useful here.

Let's find the NF:

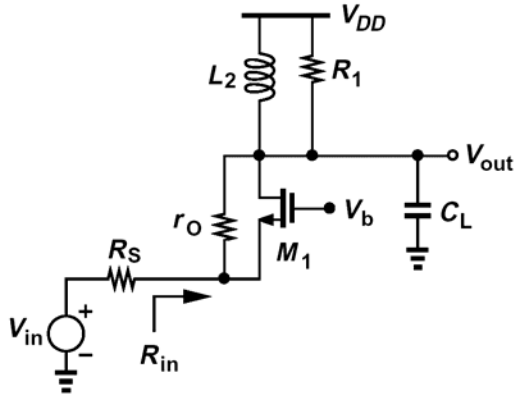


Exercise: Compute the NF including the noise of the current source.

The tight relationship between the input matching and NF in the CG stage is problematic. If the input resistance were higher than 1/gm, we could have a higher gm to get a lower NF.

- In deep submicron technologies, the situation changes:

Sketch the input resistance vs. freq.



$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_1} R_1$$

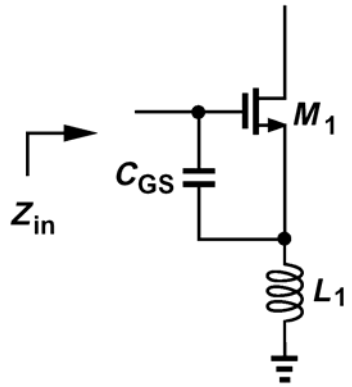
$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{2(1 + r_O/R_1)}$$

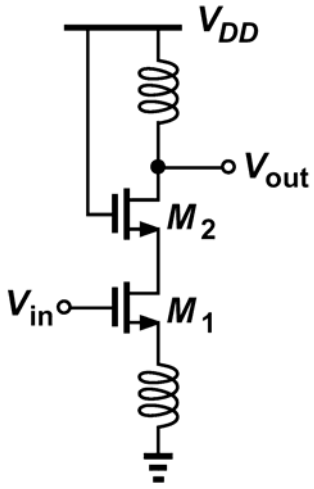
Remedy: Add a cascode:

But the cascode device contributes some noise and consumes headroom → the tail bias has less headroom and more noise.

- Design Procedure:
(1) Using simulations, plot gm vs. Id for a given W. Pick the Id that gives 80-90% of saturated gm. ("~optimum Id-W combination")
(2) Scale W and Id to obtain 1/(gm + gmb)=50 ohms.
(3) Compute necessary value of source inductance. → its Rp must be high enough.
(4) As a guess, select width of cascode equal to width of input device.
(5) Find load inductance to resonate with total output cap.

- **Cascode CS Stage with Inductive Degeneration**





- We often need to <u>reduce</u> f_T of the transistor to obtain 50 ohms!

- But Cgd and the input pad capacitance also lower the real part:

It can be proved that the real part falls to:

- Also need a series inductor at input:

Exercise: A 5-GHz LNA requires an Lg of 2 nH. If the Q is 5, can we build this on-chip?

→ In most cases, both inductors are off-chip.

- Computation of Noise Figure

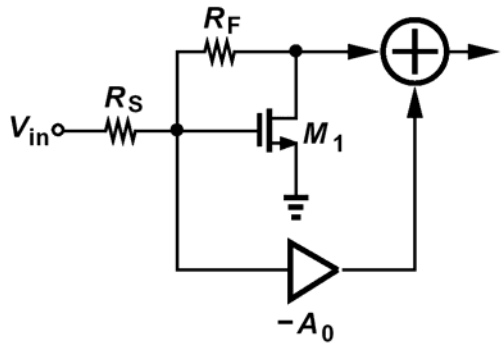
- Design Procedure: Start with three knowns: center freq., value of deg. Inductance, value of input series inductance. The following two equations govern the design:

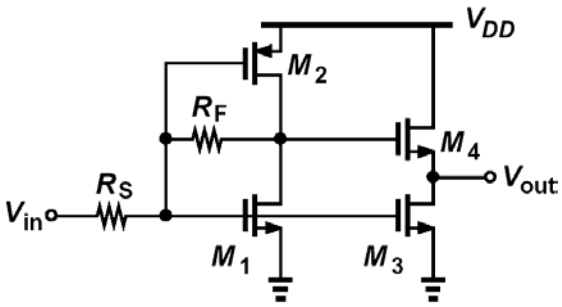
(1) Compute Cgs1. and gm1, and ω_{T1}
(2) May need to reduce ft.
(3) As a guess, choose width of cascode device equal to width of input device (with minimum length).
(4) Choose load inductance to resonate with the load cap.
(5) Reexamine input match.

Or we can begin with a known NF.

- **Noise-Canceling LNAs**

Identify two nodes at which signal appears with opposite polarities and noise of input devices with the same polarity. [Bruccoleri, JSSC, Feb.04]





Exercise: Find the NF of the circuit on the left including the input-referred noise voltage of the additional amplifier.

Differential LNAs

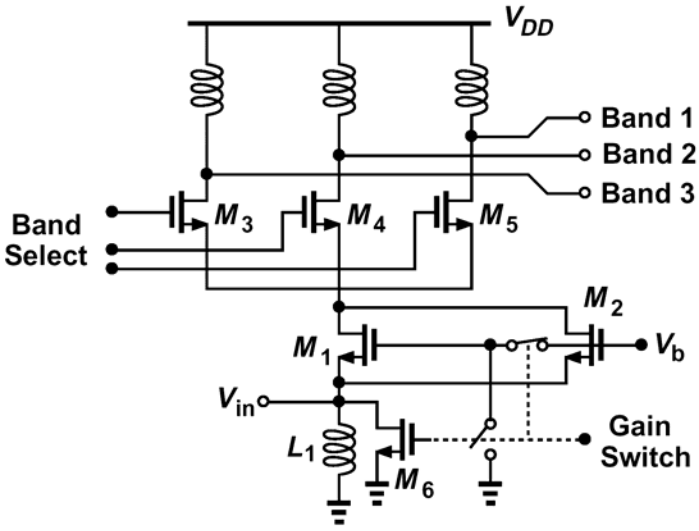
To achieve a high IP2, direct-conversion receivers may incorporate differential LNAs:

But now a "balun" is required:

Gain and Band Switching

Often need to lower the gain of the LNA for large inputs. But the input match must remain intact.

Band switching may be necessary for broadband applications:



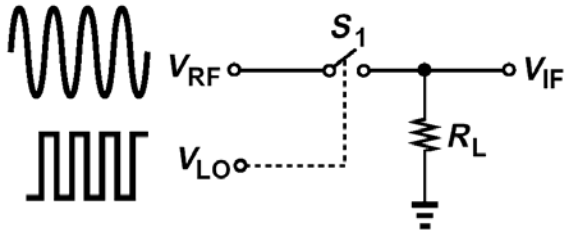
RF Mixers

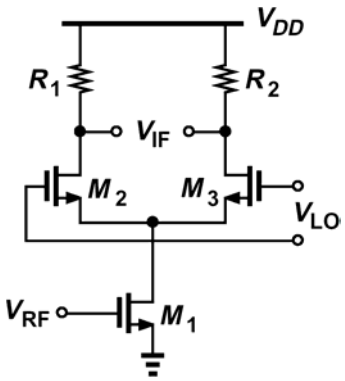
General Considerations

- **Performance Parameters**

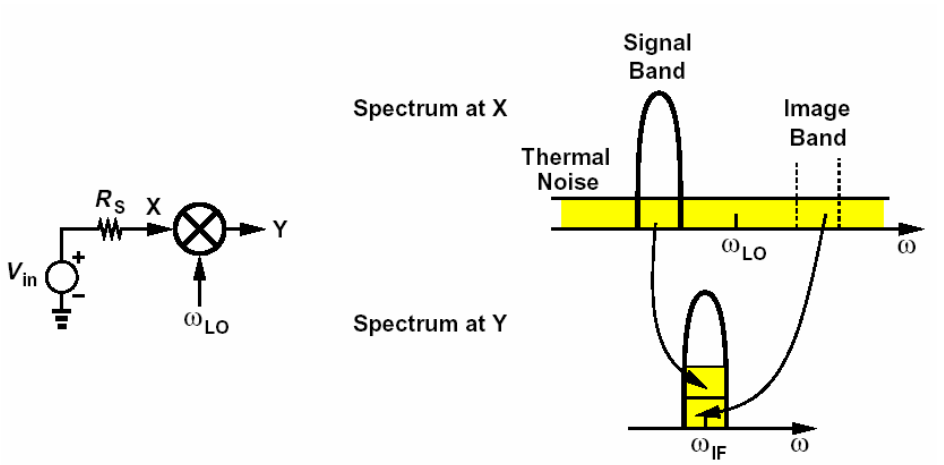
- Noise
- Linearity: IP3, IP2
- Voltage Conversion Gain
- Supply Voltage
- Power Dissipation

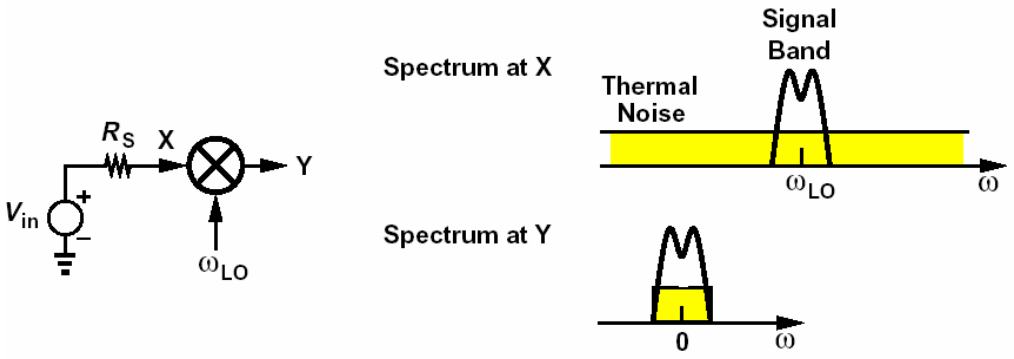
- **Passive and active Mixers**





- **SSB and DSB Noise Figures**





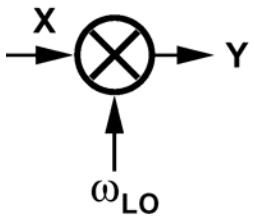
- **Port-to-Port Isolation**

The leakage from each port to the other may degrade the performance:

- LO-RF Feedthrough

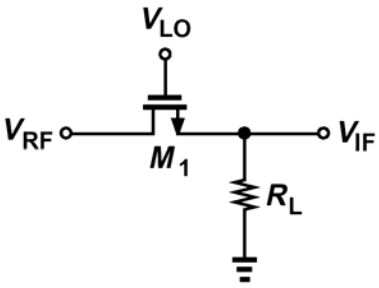
- RF-LO Feedthrough

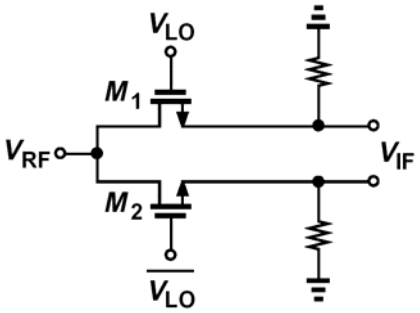
- LO-IF Feedthrough

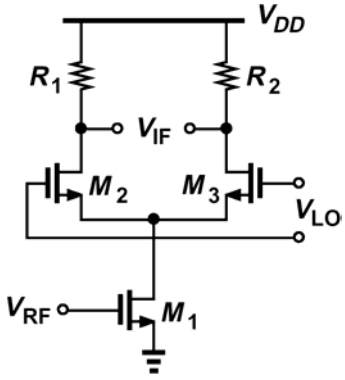


And all other combinations …

- **Single-Balanced and Double-Balanced Mixers**



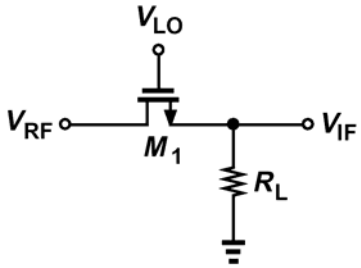


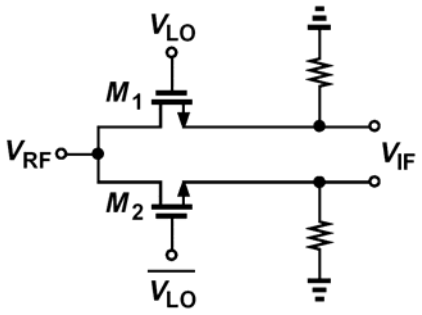


What is the ideal LO waveform?

Passive Mixers

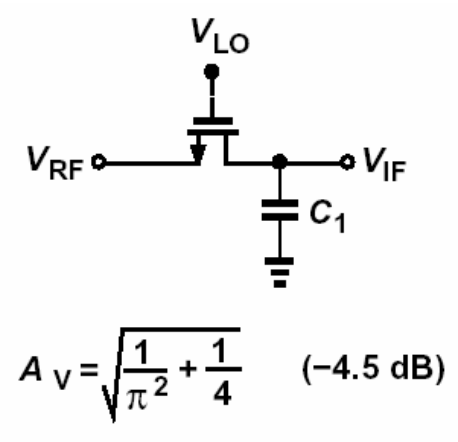
- "Return-to-Zero" Implementations:

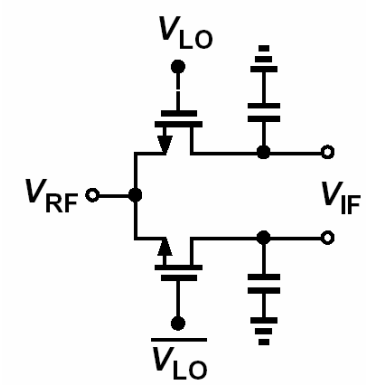




Conversion Gain:

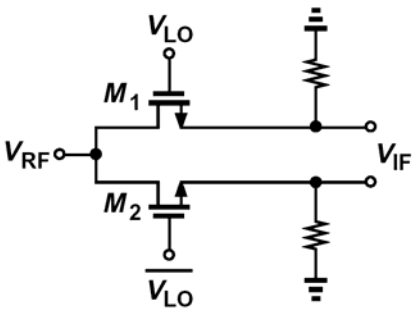
- Sampling Mixers

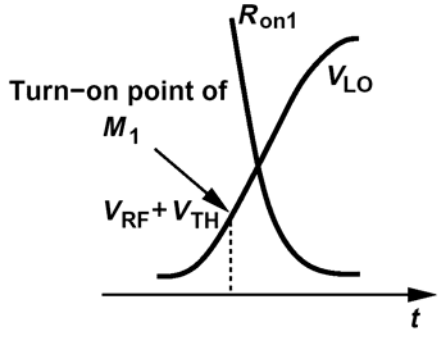




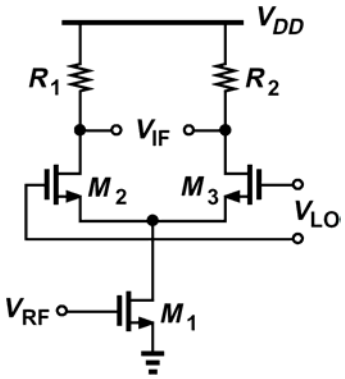
- Flicker Noise: Passive mixers generate little flicker noise in the baseband output if the transistors do not enter saturation at any point during the cycle and carry no dc current.

- Linearity: Passive mixers with rail-to-rail LO swings can achieve a high linearity, e.g., IP3 ~ 10-15 dBm.





Active Mixers



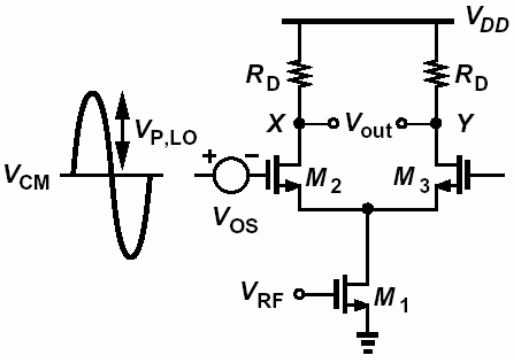
- Calculate the voltage conversion gain:

- What limits the gain?

- What limits the linearity?

IP3:

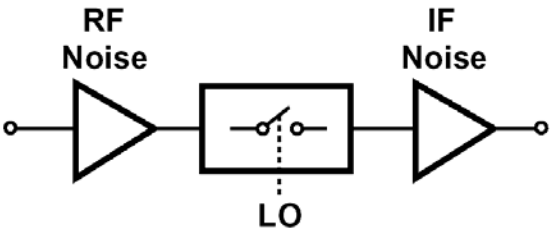
IP2:

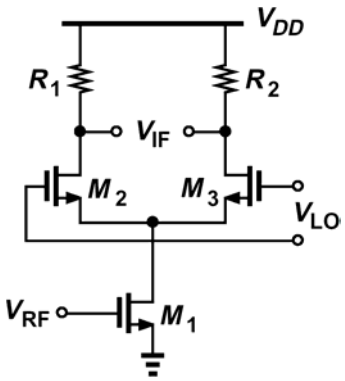


$$V_{IIP2} = 4(V_{GS1} - V_{TH1})\frac{V_{P,LO}}{V_{OS}}$$

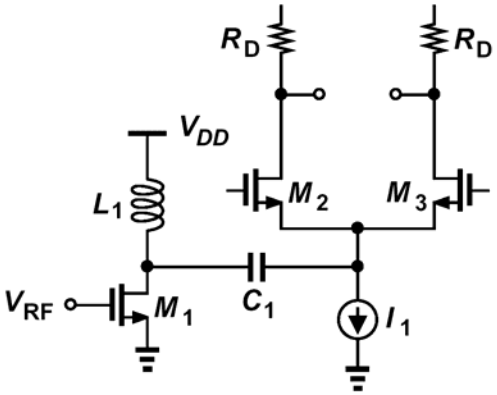
Flicker Noise:

Thermal Noise:

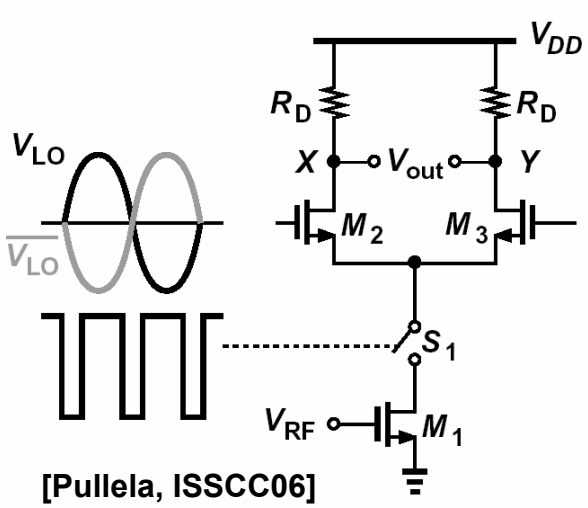




Improved Active Mixers:

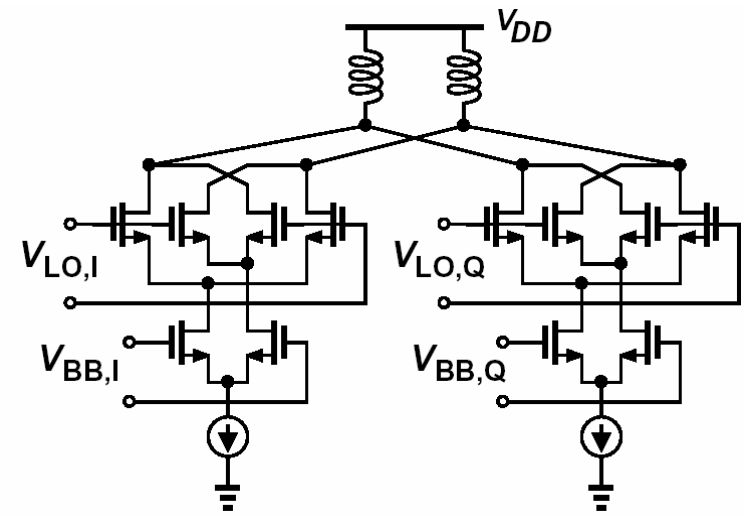


[Razavi, VLSI Symp. 97]



[Pullela, ISSCC06]

Upconversion Mixers



Folded Baseband Input: