RF Synthesizer Design

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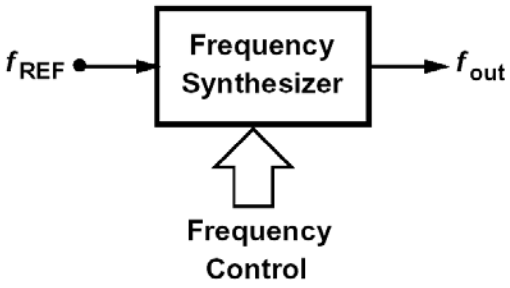
Outline

- **Synthesizer Issues**
- **Integer-N Synthesis**
- **Fractional-N Synthesis**

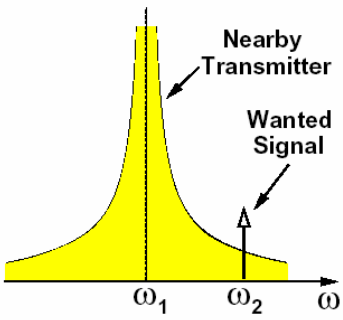
General Issues



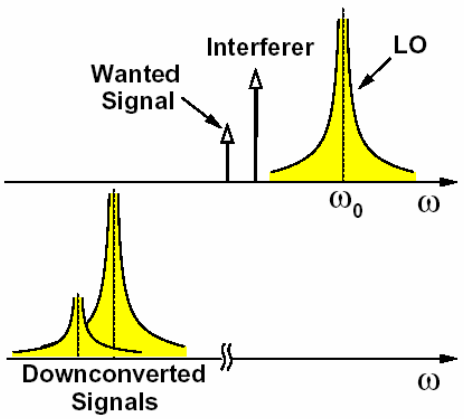
- Frequency Accuracy
- Phase Noise
- Sidebands
- Switching Time
- Output Swing
- I/Q Generation

Phase Noise

Transmitter

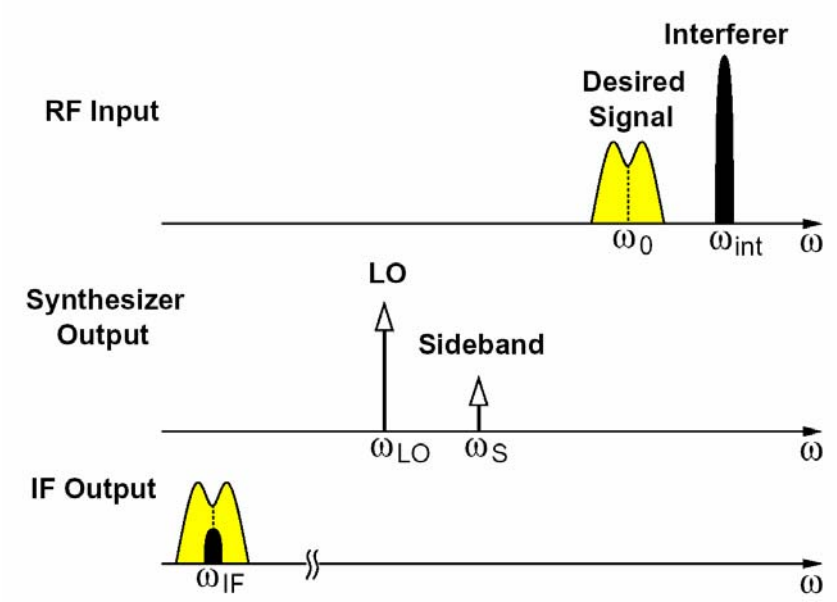


Receiver

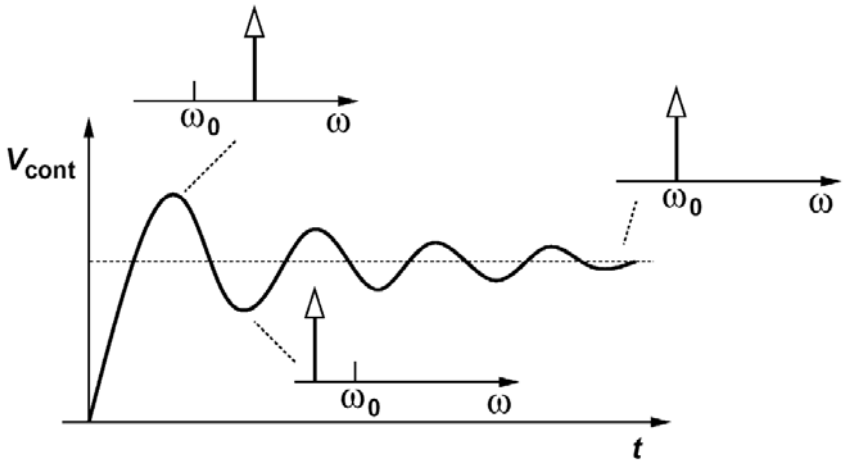


- Phase Noise in Receive Path:
  - Reciprocal Mixing
  - Signal Phase Corruption

Sidebands

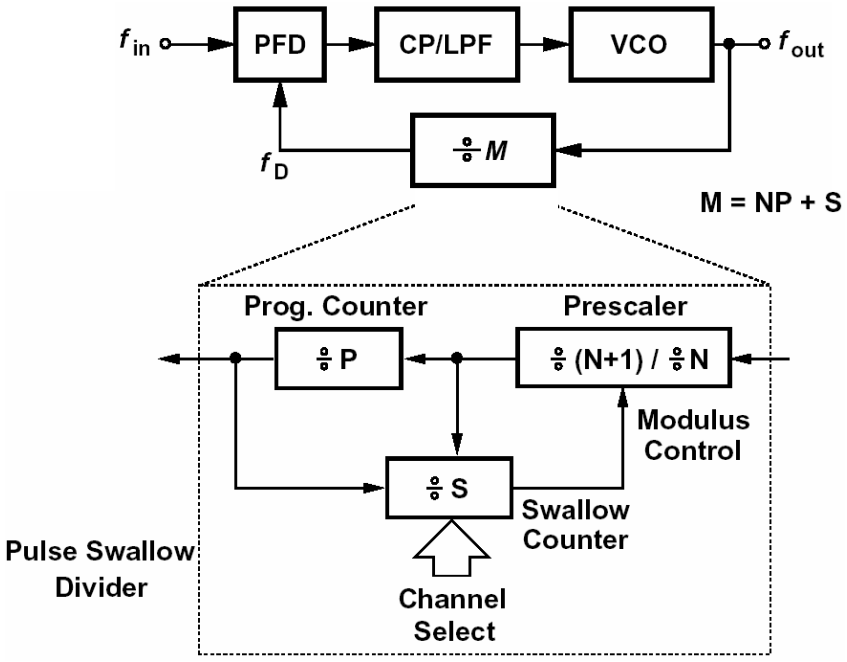


Settling Time



- Settling time usually trades with sideband magnitude.

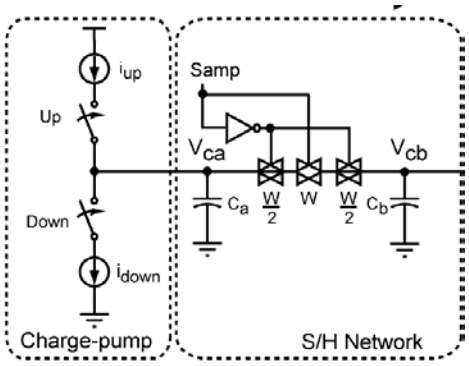
Integer-N Architecture



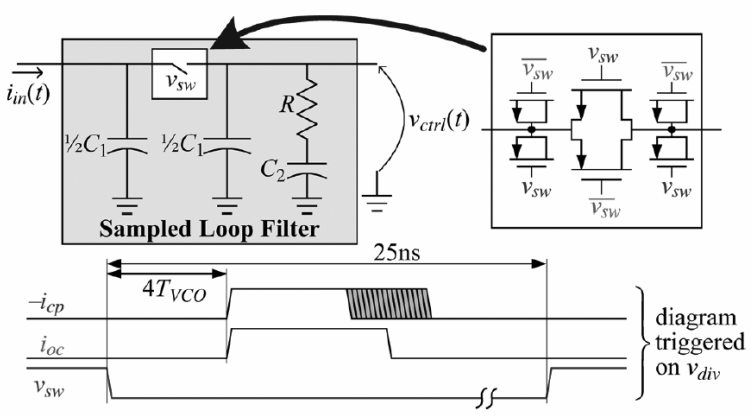
Integer-N Synthesis Issues

- Settling time: ~100 input cycles
- Frequency spacing = reference frequency → slow settling; e.g., 100 us for 1-MHz channel spacing.
- Narrow loop bandwidth → VCO phase noise not suppressed much.
- Large divide ratio amplifies reference phase noise.
- Loop filter requires large caps.

Spur Reduction

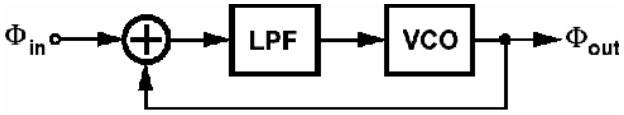


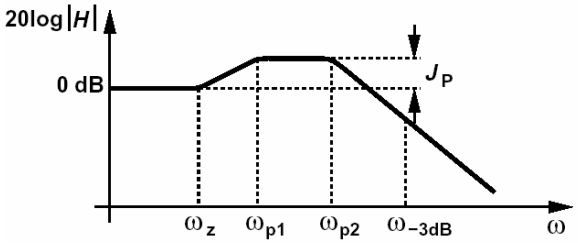
[Meninger&Perrott, JSSC, April 06]



[Wang et al, JSSC, Dec. 08]

Effect of Input Phase Noise



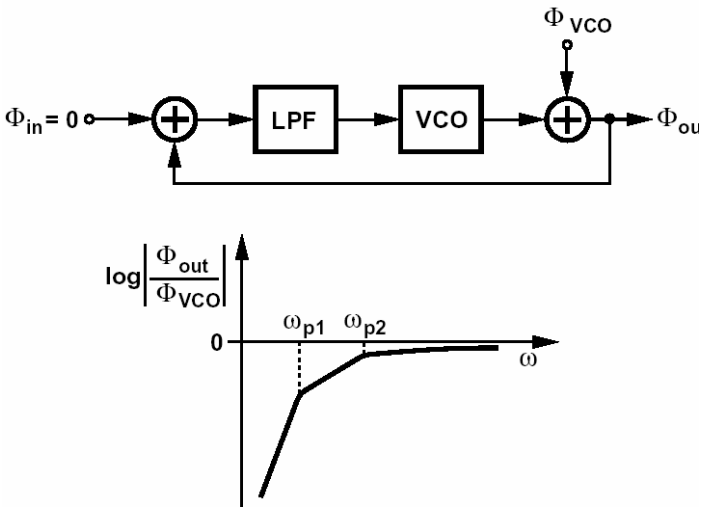


$$x(t) = A\sin[\omega_c t + \phi_{in}(t)]$$
$$y(t) = B\sin[\omega_c t + \phi_{out}(t)]$$

$$\Rightarrow H(s) = \frac{\omega_n^2(1 + s/\omega_z)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

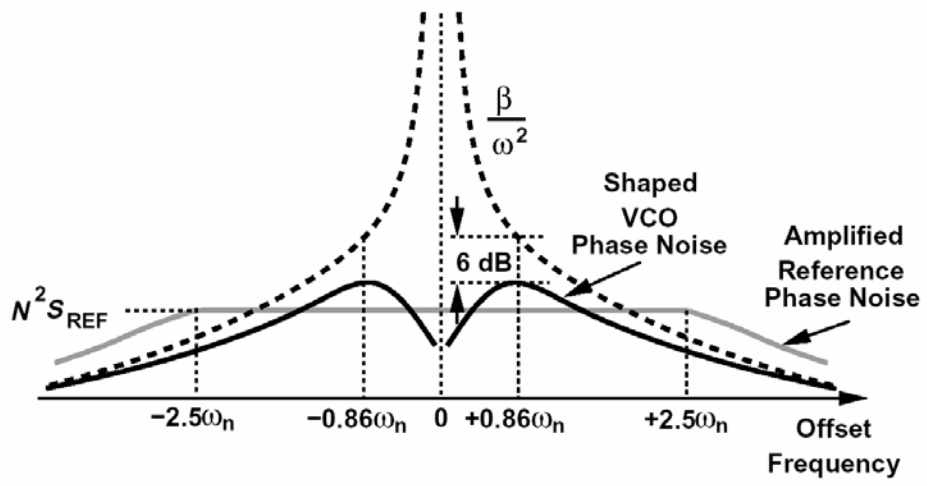
- **Frequency multiplication amplifies input phase noise.**

Effect of VCO Phase Noise



$$\frac{\Phi_{out}(s)}{\Phi_{VCO}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

PLL Output Noise Due to VCO

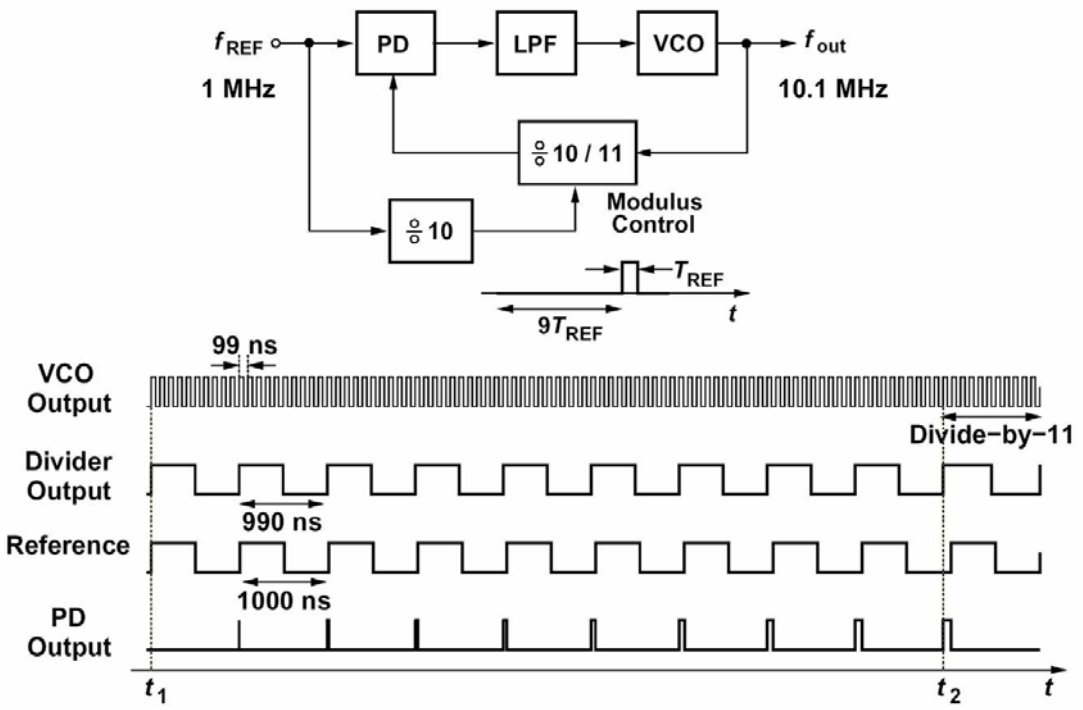


$$S_{out} = \frac{\omega^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2} \cdot \frac{\beta}{\omega^2} \qquad \zeta = 1 \Rightarrow \qquad S_{out,peak} = \frac{\sqrt{3}-1}{3}\frac{\beta}{\omega_n^2} \approx \frac{1}{4.1}\frac{\beta}{\omega_n^2}.$$

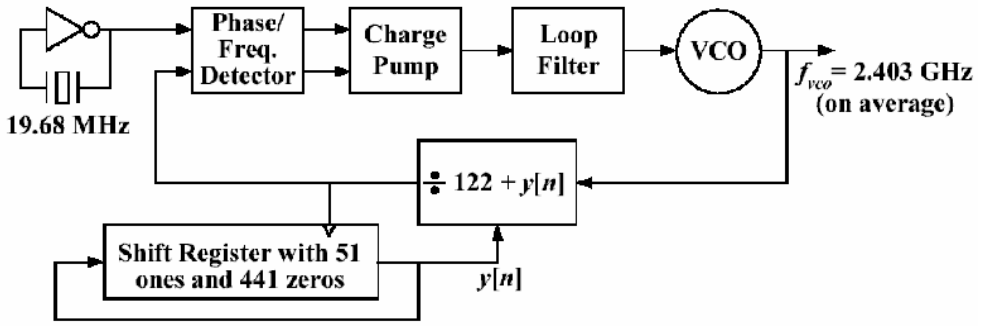
$$\omega_{peak} = \sqrt{-\zeta^2 + \sqrt{\zeta^4 + 2}}\,\omega_n$$

[Razavi, TCAS I, Aug. 09]

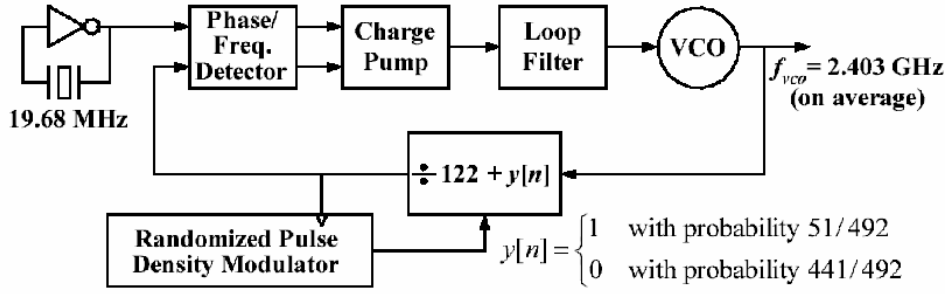
Fractional-N Architecture



Evolution of Frac-N

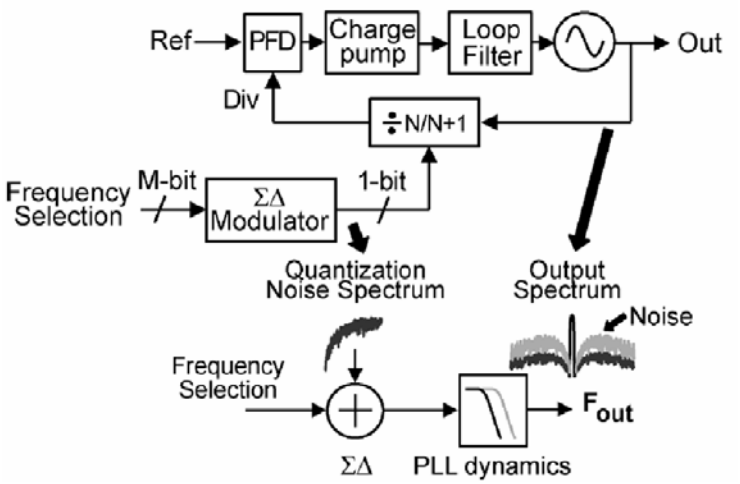


- Periodically switch modulus between 122 and 123 such that the average modulus is 122+51/492.



[Galton, *High-Performance Phase-Locking*, Razavi, Ed., 03]

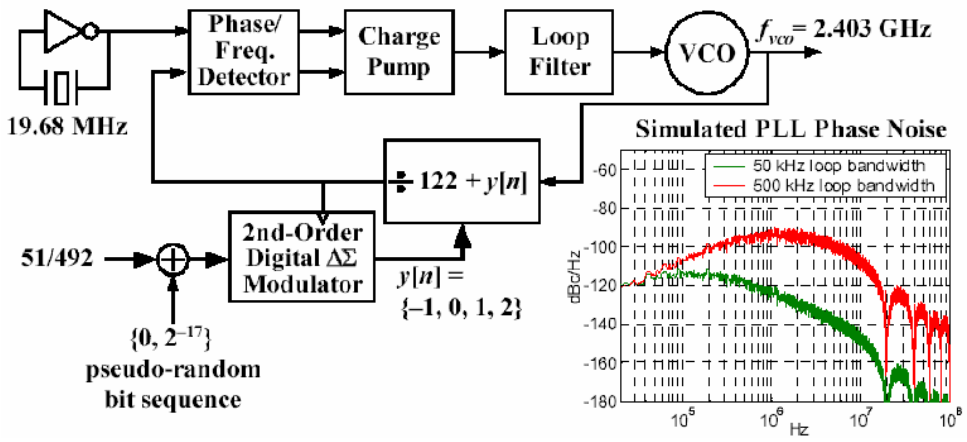
ΣΔ Frac-N



[Meninger&Perrott, JSSC, April 06]

- The ΣΔ modulator generates the required average, x[n], with a quantization noise that is shaped to move to high frequencies.
- Frequency spacing ≠ reference frequency
- Smaller divide ratio
- Wide loop bandwidth?

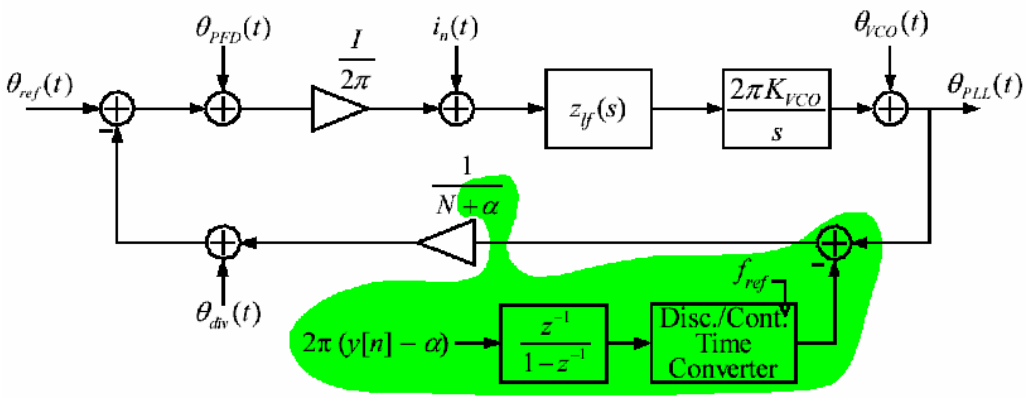
Problem of Quantization Noise



- Large PLL bandwidth lets in too much quantization noise.

[Galton, *High-Performance Phase-Locking*, Razavi, Ed., 03]

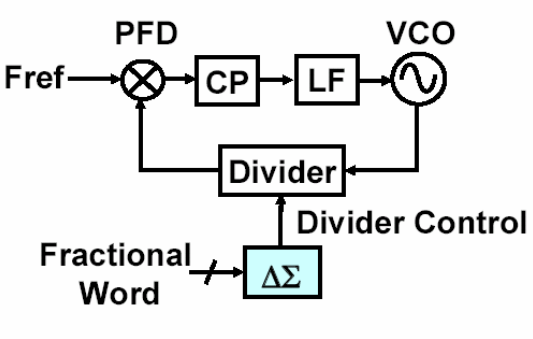
Comparison of Integer-N and Frac-N

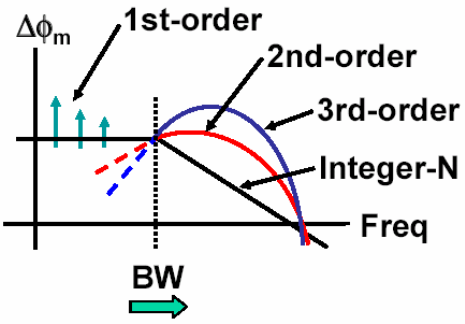


- **Approximately same loop equations, stability issues, noise transfer functions**

[Galton, *High-Performance Phase-Locking*, Razavi, Ed., 03]

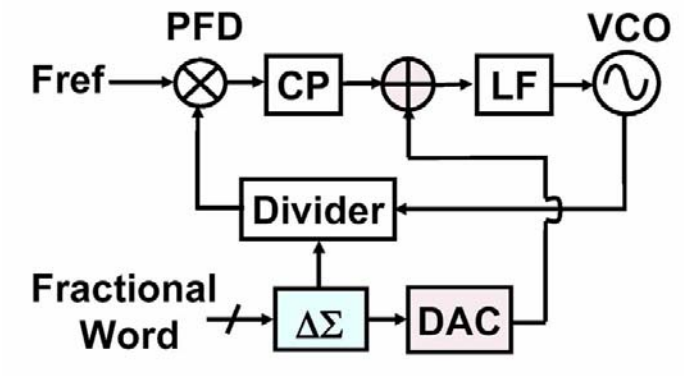
Effect of ΣΔ Order

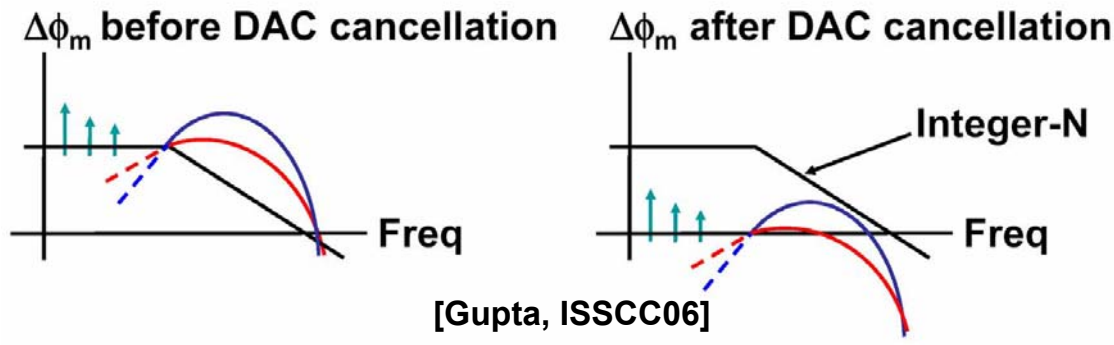




[Gupta, ISSCC06]

Reduction of Quantization Noise





[Gupta, ISSCC06]