

EE 215A

HO#1

Fall 2008

Analog Integrated Circuit Design

Instructor: Behzad Razavi
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Office Hours (Tentative): Tue., Thur., 2:00-3:30 pm

Time: Tue., Thur., 10:00-11:50 am

Place: Boelter 2444

Prerequisites: Undergraduate electronics courses, e.g., EE 115B

Credit: 4 Units

Grading: Midterm 30%
Final 30%
Homeworks 20% (Late HW Policy: 25% deduction per day)
Final Project 20%

Course Textbook:

B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

Recommended Books:

P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Edition, 2001, Wiley.

D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1997.

Important Dates:

Thur. Oct. 2,	HW#1 Due
Tue. Oct. 14	HW#2 Due
Thur. Oct. 23	HW#3 Due
Tue. Nov. 4	HW#4 Due
Thur., Nov. 6	Midterm Exam
Fri. Dec. 5	Final Project Due
Thur. Dec. 11, 3:00-6:00 pm	Final Exam

Outline

- MOS Device Structure and Circuit Models
- Single-Stage and Differential Amplifiers
- Passive and Active Current Mirrors
- Frequency Response of Amplifiers
- Noise
- Feedback
- Op Amp Design
- Stability and Frequency Compensation
- Bandgap References
- Introduction to Switched-Capacitor Circuits

Simulation Platform: HSPICE or Cadence. The device models for 0.18-um technology are posted at <http://www.ee.ucla.edu/~brweb/teaching.html> and called 215D.sp (for HSPICE) and 215D.scs (for Cadence). The minimum device width is 0.6 um. The source/drain area is given by $W \times 0.6 \text{ um}$, and the perimeter by $2W + 1.2 \text{ um}$.

For a Cadence tutorial, visit http://www.ee.ucla.edu/~dejan/ee115c/ee115c_flow.htm. You need 4-5 hours to learn the basics; so be patient!