

A Computationally Efficient ASIC Implementation for the decoding of Space-Time Block Codes

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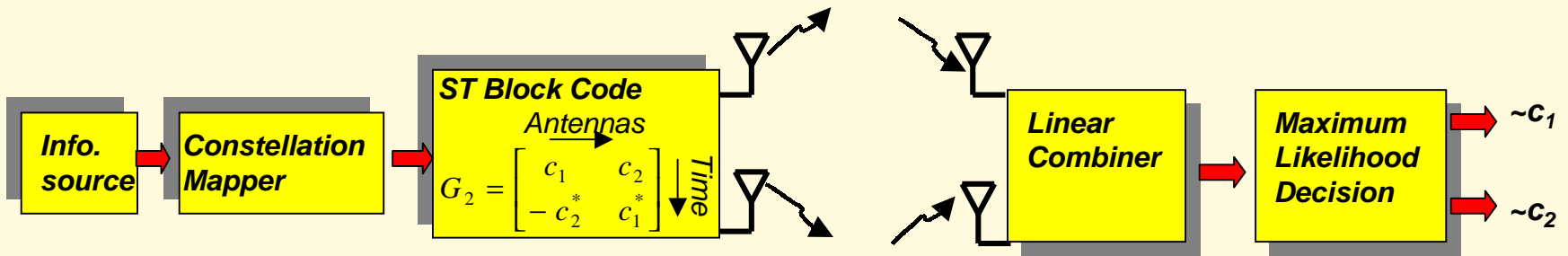
Wireless Integrated Systems

Research Group

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ST BLOCK CODES

- **A transmit diversity scheme with simple decoding complexity at the receiver**
 - ◆ Orthogonal structure of provides de-coupling of signals from different antennas
 - ◆ Decoding complexity is linearly dependent on the constellation size



r_1^j : Received signal at antenna j at time slot 1
 p_k : Symbol from the constellation signal set

$\alpha_{i,j}$: Channel coeff. from Tx ant. i to Rx ant. j
 c_i : Transmitted symbol

$$M_{G_2}(c_1, p_k) = \left| \left[\sum_{j=1}^m (r_1^j \alpha_{1,j}^* + (r_2^j)^* \alpha_{2,j}) \right] - p_k \right|^2 + \left(-1 + \sum_{j=1}^m \sum_{i=1}^2 |\alpha_{i,j}|^2 \right) |p_k|^2$$

$$M_{G_2}(c_2, p_k) = \left| \left[\sum_{j=1}^m (r_1^j \alpha_{2,j}^* - (r_2^j)^* \alpha_{1,j}) \right] - p_k \right|^2 + \left(-1 + \sum_{j=1}^m \sum_{i=1}^2 |\alpha_{i,j}|^2 \right) |p_k|^2$$

Sign Approach for BPSK and QPSK

$$M(c_m, p_k) = \min_{p_k} \left\{ \left| (a + jb) - p_k \right|^2 + \beta \left| p_k \right|^2 \right\}$$



$$M(c_m, p_k) = \min_{p_k} \left\{ a^2 + b^2 + p_{kx}^2 + p_{ky}^2 - 2(a p_{kx} + b p_{ky}) + \beta (p_{kx}^2 + p_{ky}^2) \right\}$$

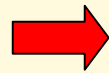
p_k^2 is same for BPSK & QPSK
 $a^2 + b^2$ is common for all comparisons



$$M(c_m, p_k) = \min_{p_k} -2(a p_{kx} + b p_{ky})$$



$$\max_{p_k} (a p_{kx} + b p_{ky})$$



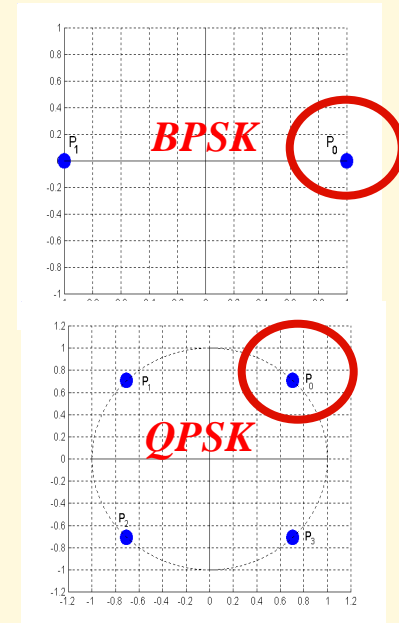
$$\begin{aligned} \text{sign}(a) &\equiv \text{sign}(p_{kx}) \\ \text{and} \\ \text{sign}(b) &\equiv \text{sign}(p_{ky}) \end{aligned}$$



48 Mult & 47 Add



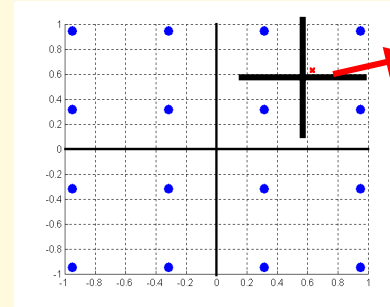
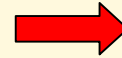
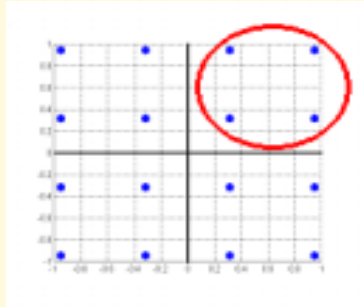
sign(a), sign(b)



16-QAM-Variable Bias Point Approach

$$M(c_m, p_k) = |(a + jb) - p_k|^2 + \beta |p_k|^2 \quad \beta = -1 + 2 \sum_{j=1}^m \sum_{i=1}^2 |\alpha_{i,j}|^2$$

$sign(a)$
 $sign(b)$



$(0.6325, 0.6325)$ for $E_{ave} = 1$

$$bias = 0.6325 (\beta + 1)$$

$$bias = 1.265 \left(\sum_{j=1}^m \sum_{i=1}^2 |\alpha_{i,j}|^2 \right)$$

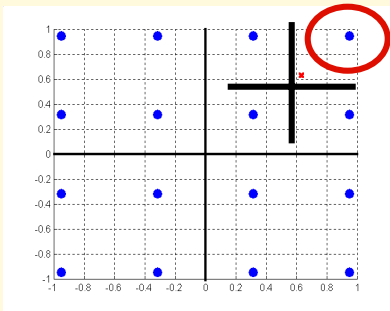


$$a' = a - bias$$

$$b' = b - bias$$



$sign(a')$
 $sign(b')$



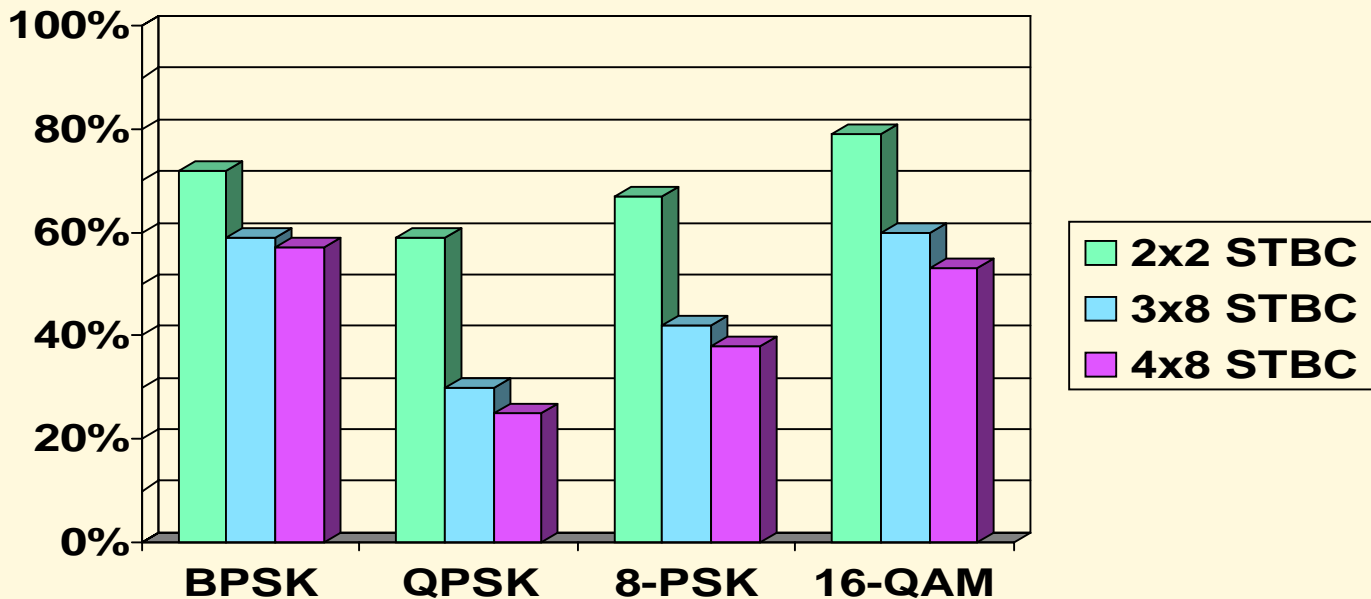
96 Mult & 76 Add



1 Mult & 2 Subt

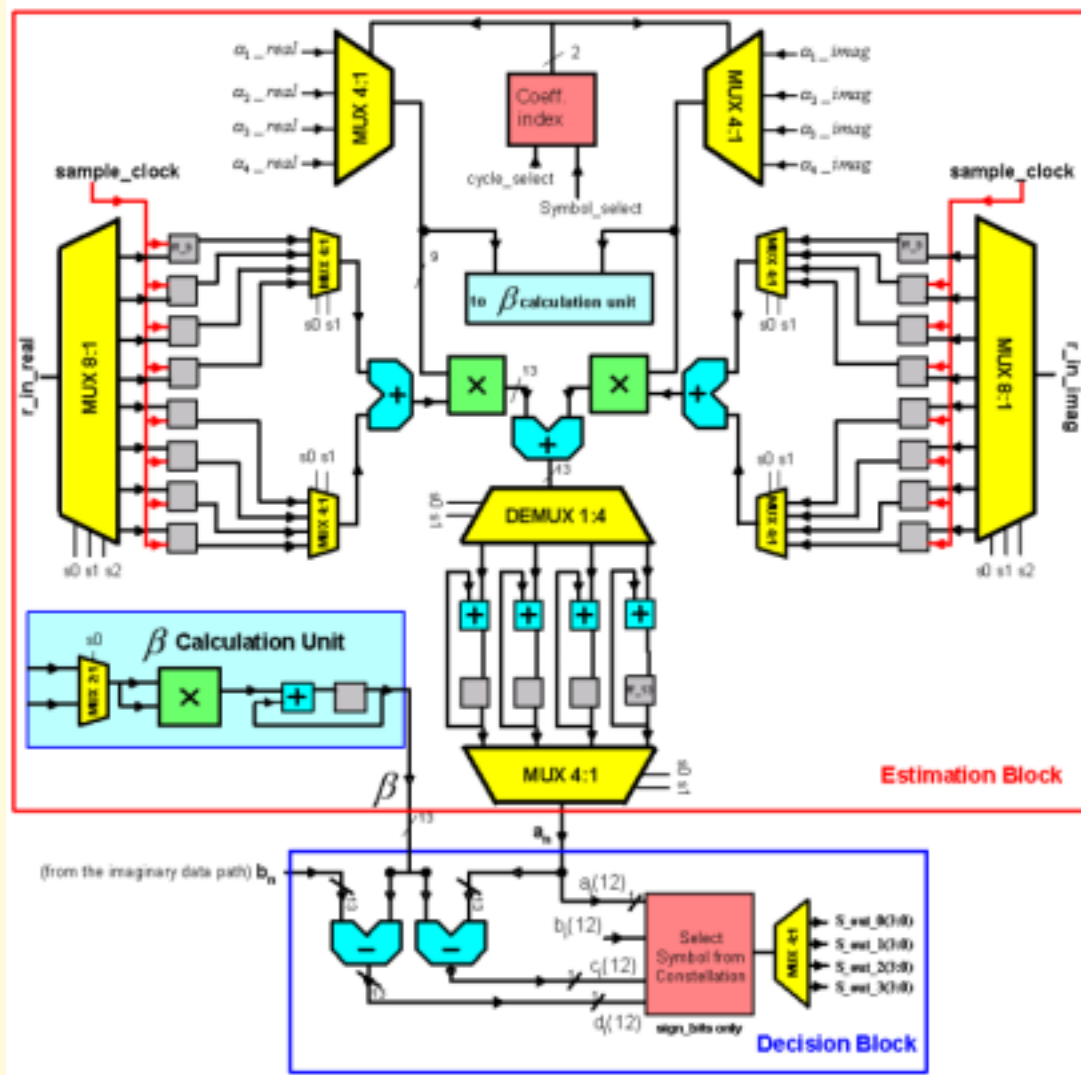
Computation Reductions

Percentages of the computation reductions using New Algorithm



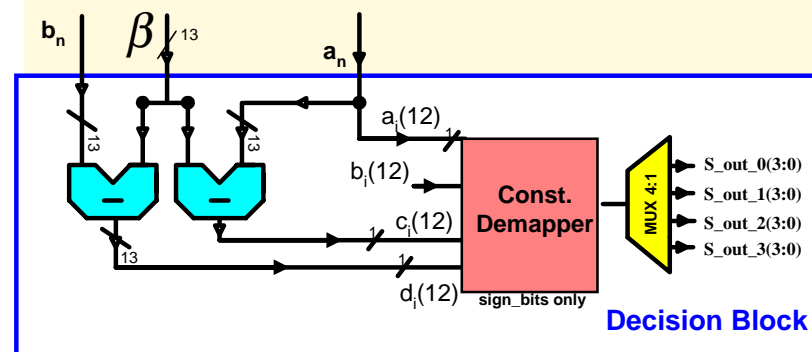
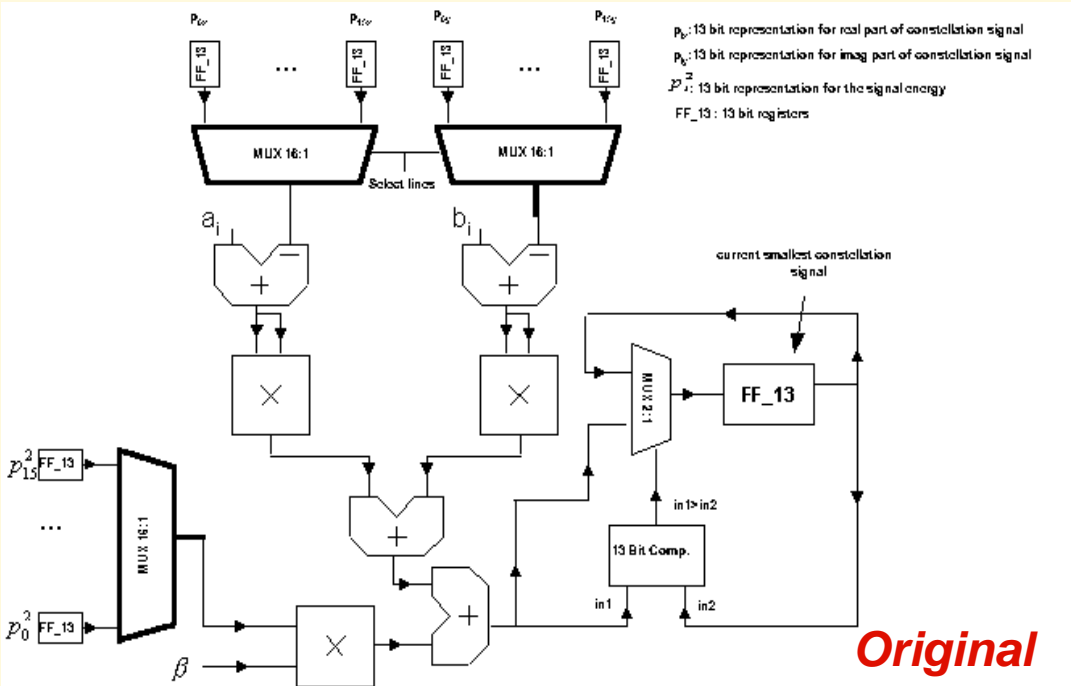
- **Same performance with up to 80% computation reduction**
- **In most cases more than 50% reduction in computation complexity**

Proposed Estimator Block for a & b variables



- **Benefits from the symmetry and common terms in decision metrics**
- **Halves the total number of operations for estimation of a & b variables**
- **Two sides are symmetric**
- **Same control signals**
- **Store @ f_{symbol}**
- **Wait till the arrival of r_8**
- **Process @ $f_{clk} > 4 \times f_{symbol}$**

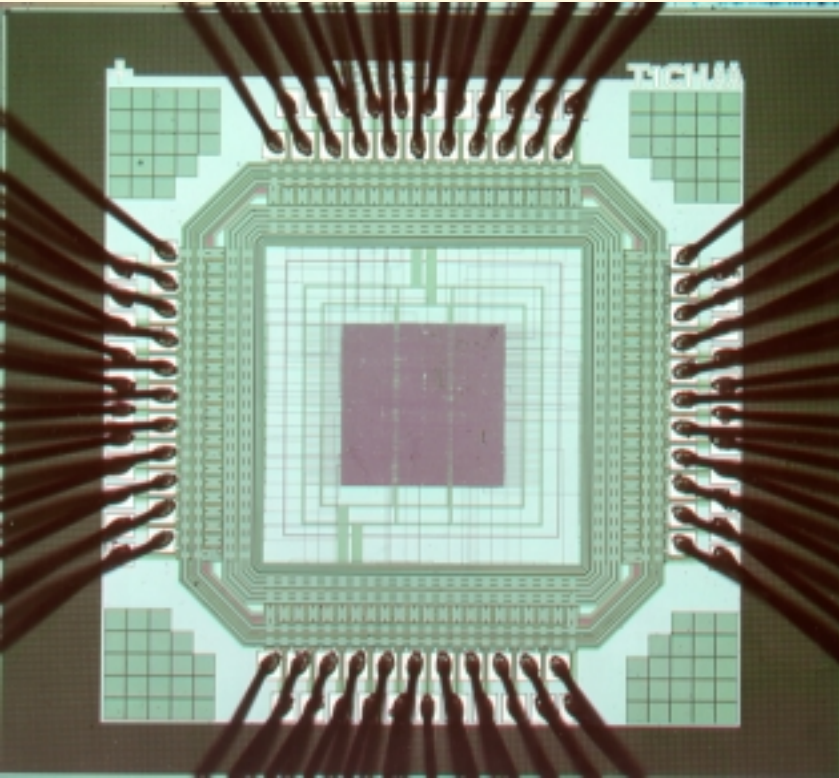
Hardware Complexity of Decision Blocks



■ **Direct implementation of original block needs additional:**

- ◆ 49 (13-bit) registers
- ◆ 3 Multipliers + 4 Adders + 3 (16:1) Muxes + 1 (2:1) Mux + 1 comparator
- ◆ 4 parallel instances of the above figure !!!

STBD ASIC



■ Features

- ◆ Variable symbol rates with up to 75 MBaud
- ◆ Variable modulation
 - ✦ BPSK, QPSK, 8-PSK, 16-QAM
- ◆ 3.3/1.8V TSMC 0.18 μ process
- ◆ 5.5 mW core power
- ◆ Core area: 0.5 mm x 0.5 mm
- ◆ Chip area: 1.7 mm x 1.7 mm
- ◆ 5208 Gates

	Power	Cell Area	# of Cell
Proposed	5.5 mW	0.16 mm ²	5208
Original	20.33 mW	0.82 mm ²	28018

- Up to 80% computation reductions
- A symmetrical low computation approach for estimation of a & b variables
- Substantially simplified decision block architecture
- %75 area & power savings compared to a direct implementation of original algorithm