Local epitaxial growth of ZrO_2 on Ge (100) substrates by atomic layer epitaxy

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High-k dielectric deposition processes for gate dielectric preparation on Si surfaces usually result in the unavoidable and uncontrolled formation of a thin interfacial oxide layer. Atomic layer deposition of ~55-Å ZrO_2 film on a Ge (100) substrate using $ZrCl_4$ and H_2O at 300 °C was found to produce local epitaxial growth [(001) Ge//(001) ZrO_2 and [100] Ge//[100] ZrO_2] without a distinct interfacial layer, unlike the situation observed when ZrO_2 is deposited using the same method on Si. Relatively large lattice mismatch (~10%) between ZrO_2 and Ge produced a high areal density of interfacial misfit dislocations. Large hysteresis (>200 mV) and high frequency dispersion were observed in capacitance–voltage measurements due to the high density of interface states. However, a low leakage current density, comparable to values obtained on Si substrates, was observed with the same capacitance density regardless of the high defect density. *© 2003 American Institute of Physics.* [DOI: 10.1063/1.1613031]

As the continued scaling of Si complementary metal-oxide-semiconductor (MOS) devices approaches its fundamental limits, various methods are being investigated to increase the saturation current by improving carrier mobility in the channel region. Improvements of carrier mobility have been obtained by replacing Si channel with strained Si;[1] however, a major breakthrough may be achieved if the conventional Si substrate is replaced by alternative semiconductor materials, such as Ge, which have high intrinsic carrier mobilities. Because of its higher low-field carrier mobility and smaller mobility band gap for supply voltage scaling, there have been many attempts to use Ge as a channel material in high-speed field-effect transistors.[2,3] Although, during device manufacturing, the lack of a sufficiently stable native oxide poses problems in obtaining a high quality surface passivation, the possibility of Ge-based MOS capacitors and transistors showing superior electrical properties using high-k dielectrics was demonstrated recently.[2,4]

Among many possible deposition techniques for high-k gate dielectrics, atomic layer deposition (ALD) has drawn attention as a method for preparing ultrathin metal-oxide layers with excellent electrical characteristics and near-perfect film conformality because of the layer-by-layer nature of the deposition kinetics.[5] This technique is promising from the perspective of deposition rate control and conformality compared to other techniques, especially for proposed future devices with vertical transistor channels.[6]

In this letter we demonstrate ZrO_2 high-k dielectric deposition onto a pure Ge (100) substrate by ALD. We observed local epitaxial growth of ZrO_2 films without any distinct amorphous interfacial layer. This behavior stands in contrast to that observed in ZrO_2 deposition onto Si, which produces a low-k SiO_2-containing layer. Microstructural and electrical properties of ALD ZrO_2 on Ge were investigated using transmission electron microscopy (TEM), x-ray photoelectron spectroscopy (XPS), and basic MOS electrical characterizations.

As a substrate, 4-in.-diameter n-type ⟨100⟩ Ge wafers having 0.25 (Ω cm) resistivity were used and the native oxide (GeO_x) was removed by exposing the wafers to HF vapor before ZrO_2 ALD. After cleaning, the Ge wafers were immediately transferred to a cold wall-type high vacuum ALD system within an hour, and deposition of ~55-Å ZrO_2 was performed at 300 °C using alternating surface-saturating reactions of $ZrCl_4$ and H_2O. Each precursor was pulsed for 2 s and N_2 purging was followed for 30 and 60 s after each H_2O and $ZrCl_4$ pulse, respectively. The base pressure of the system was around 5×10^{-8} Torr and the process pressure was maintained at 0.5 Torr during ALD. Various sizes of Pt gate electrodes for electrical measurements were deposited by the room temperature e-beam evaporation through shadow mask and, subsequently, Al was deposited on the backside of the Ge wafers to reduce the contact and series resistance of the samples. $C-V$ measurements were performed after forming gas anneal (4% H_2/N_2, 400 °C, 30 min) using an HP4284A precision LCR meter. $I-V$ measurements were performed using a Keithley 230 programmable voltage source and 6512 programmable electrometer. The thickness and film microstructures of selected samples were analyzed by both cross-sectional and plan-view TEM (JEOL 3010 and Philips CM20 FEG-TEM). The compositional characterization of a ZrO_2/Ge structure was carried out by angle resolved-XPS using a Surface Science Instruments S-Probe (Al K_α x-ray source).

Figure 1 shows the cross-sectional and plan-view image of ALD ZrO_2 (~55 Å) grown on a HF-vapor-cleaned Ge substrate. In contrast to the deposition characteristics typi-

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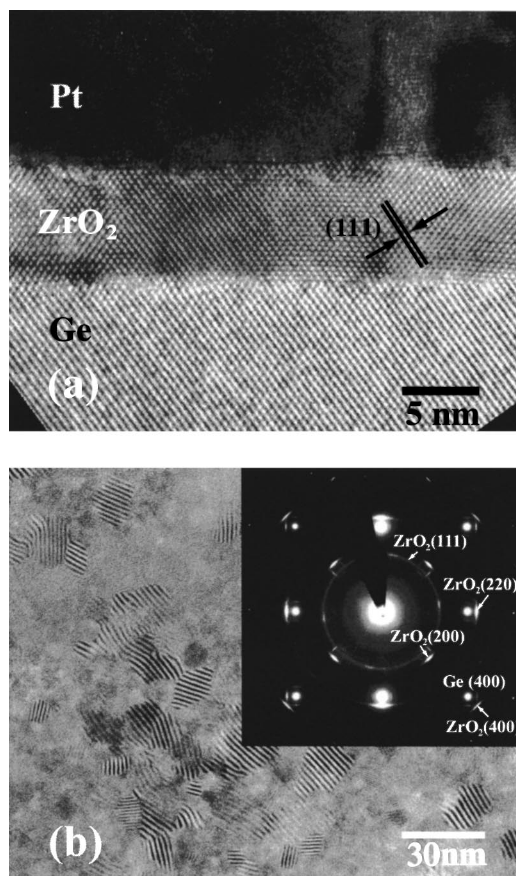

FIG. 1. (a) Cross-sectional high-resolution-TEM micrograph of Pt/55-Å ZrO_2/Ge (100) along the ⟨110⟩ zone-axis, and (b) bright-field plan-view image of 55-Å ZrO_2/Ge (100). Inset of the figure shows selected area electron diffraction pattern and corresponding epitaxial relationship.

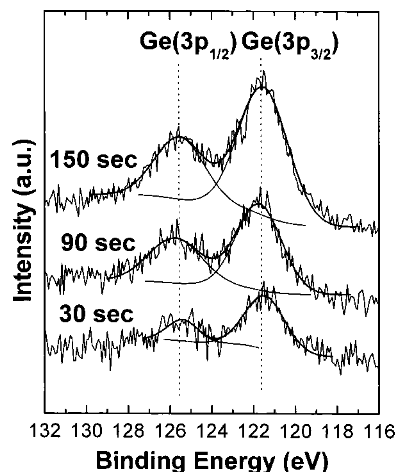

FIG. 2. X-ray photoelectron spectrum and peak fitting results for the Ge $3p$ feature of a 55-Å ZrO_2/Ge specimen for several sputter etch times and a 90° detection take-off angle.

cally observed on Si substrates, ALD deposition of ZrO_2 films on a Ge (100) showed local epitaxial growth without a distinct interfacial layer, as shown in Fig. 1(a). High-*k* dielectric deposition by ALD occurs readily on hydroxylated surfaces, such as chemical SiO_2, or a hydroxylated oxynitride passivation. Moreover, uncontrolled formation of a thin interfacial oxide layer is observed if the Si is not already passivated by such a layer prior to deposition.[7] High-*k* materials, such as ZrO_2 and HfO_2, are stable with respect to solid-state reactions with Si; however, because metal-oxide films are often deposited in an oxidizer-rich environment, some oxidation of the Si surface during high-*k* film deposition is almost unavoidable, and the growth of this low-*k* interface layer tends to reduce the possibility of scaling of equivalent oxide thickness (EOT). Considering the Gibbs free energy of formation for ZrO_2 (−1135 kJ/mol at 600 K) and GeO_2 (−610 kJ/mol at 600 K), it is plausible that ZrO_2 should be thermodynamically stable with respect to solid-state reactions with the Ge substrate, similar to the Si case.[8] On the contrary to the ZrO_2/Si case, ZrO_2 deposited by ALD onto Ge (100) consistently resulted in an interfacial layer-free interface structure. This was the case in spite of the fact that the Ge substrates were exposed to air after HF treatment to remove the native oxide, possibly resulting in some reformation of native oxide prior to ALD. However, it is well known that Ge oxides (GeO and GeO_2) are very unstable at moderately high temperatures (>400 °C) in vacuum and also are readily dissolved in H_2O.[9] During ALD deposition, it is possible that any interfacial native oxide which forms in one part of the deposition process may be dissociated and removed in a subsequent step.

Due to the large lattice mismatch (~10%) between ZrO_2 and Ge, a significant areal density of interfacial dislocations can be seen in the cross-sectional image in Fig. 1(a). The epitaxial relationship between film and substrate was verified using plan-view imaging and electron diffraction (ED) analysis, as shown in Fig. 1(b). Indexing of ED patterns obtained during electron microscopy indicates that the ALD-grown ZrO_2 film may be in either the tetragonal or cubic phase. It is difficult to distinguish *a*- or *b*-axis oriented tetragonal grains for the epitaxial orientation present in these films. However, careful investigation of electron diffraction patterns has verified that ZrO_2 films grown by ALD on to SiO_2/Si substrates are in the tetragonal phase.[10] Therefore, it is quite likely that ALD ZrO_2 on the Ge (100) substrate may also be tetragonal. Due to the large lattice mismatch, local epitaxial growth generated numerous distorted Moiré fringes, as shown in the plan-view image in Fig. 1(b). The mosaic spread of the epitaxial film orientation also manifests itself in a distortion of diffraction seen in the ED pattern that is inset in the same figure. The (001) Ge//(001) ZrO_2 and [100] Ge//[100] ZrO_2 epitaxial relationship is observed, as expected for this system, and the existence of one extra ZrO_2 (111) atomic plane per every 10 planes in the cross-sectional image indicates that the compressive misfit strain of the ZrO_2 film is almost fully relieved by misfit dislocations.

In order to verify the absence of an interfacial germanium oxide, XPS analysis using sputter depth profiling technique was performed, as shown in Fig. 2. A 90° take-off angle was used to maximize the information depth and Ge $3p$ feature was monitored because the Ge $3d$ signal overlaps with the Zr $4p$ signal. As the sputtering etch time increases, a significant increase of the peak associated with the Ge substrate was seen. Simultaneously, the Zr and O peaks from ZrO_2 decreased, and the metallic Zr (silicide) peak having lower binding energy appeared due to the sputtering artifact (not shown here). However, no higher binding energy peaks, which might correspond to Ge suboxide or $ZrGeO_x$ (zirconum germanate), were detected.

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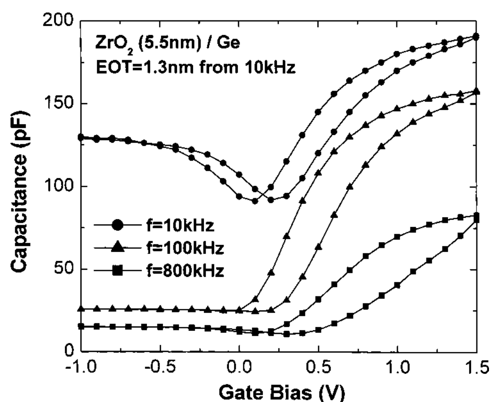

FIG. 3. $C-V$ characteristics of a Pt/55-Å ZrO_2/n-type Ge (100) structure measured at three different frequencies after forming gas anneal (4% H_2/N_2, 400 °C, 30 min).

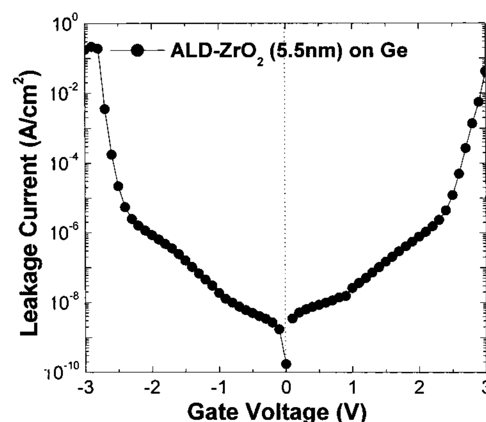

FIG. 4. Leakage current characteristics of a Pt/55-Å ZrO_2/n-type Ge (100) stack for both bias polarities. Applied voltage is defined as positive when the top Pt electrode is positively biased.

High-frequency $C-V$ measurements were performed after the forming gas annealing (400 °C, 30 min) using 7 090 μm^2 circular capacitor patterns. The capacitance was measured at various frequencies as a function of gate voltage and the capacitor was swept from inversion to accumulation and back to check the amount of hysteresis. As shown in Fig. 3, a significant amount of frequency dispersion was observed even after series resistance correction using the two-frequencies correction method,[11] and a very large hysteresis (>200 mV) was observed across the entire frequency range. After scanning from inversion to the accumulation condition, the $C-V$ curve shifted along the positive axis during reverse scan as a consequence of electron trapping from the n-type Ge substrate injection. This significant electron trapping $[3\times10^{12}\sim3.5\times10^{12}\ (/\mathrm{cm}^2)]$ and frequency dispersion are believed to originate either from the large areal density of interfacial dislocations $[\sim7\times10^{12}\ (/\mathrm{cm}^2)]$ due to the relatively large lattice mismatch or because of a very high density of interface states due to intrinsic differences in bonding corrdination across the chemically-abrupt ZrO_2/Ge interface. With decreasing measurement frequency, the inversion capacitance was observed to increase significantly. This may be attributed either to an increase in minority carrier generation due to the diffusion of impurities from the gate dielectric into the substrate, or, perhaps, to the interaction of interface slow states. Although the exact evaluation of the EOT is impossible due to the significant frequency dispersion, an EOT of ~13 Å can be extracted from the 10-kHz $C-V$ data, without quantum-mechanical corrections. For an expected ZrO_2 dielectric constant of ~25,[12] the EOT of a interfacial layer-free interface structure should be ~8 Å. This matches with $C-V$ measurement result reasonably well when quantum-mechanical effects are considered.

Figure 4 shows the room-temperature leakage current behavior of the ZrO_2 on Ge sample measured at both bias polarities. Although a large number of interface defects and low-angle grain boundaries exist in these films, a leakage current density that is significantly lower than that achieved using SiO_2 gate stacks with similar EOT[13] was measured. These excellent leakage current characteristics suggest that other crystalline high-k metal oxides with closer lattice match to Ge may be good candidates for epitaxial in high-k/Ge MOS devices. Moreover, optimization of the interface structure through process changes that may reduce the interfacial dislocation density is expected to improve the electrical properties of these high-k/Ge gate stacks.

In this letter, the microstructural and electrical characteristics of ALD-grown ZrO_2 dielectric layers on Ge (100) substrates were reported. Locally epitaxial growth of the ZrO_2 films was observed. Failure to obtain high-quality epitaxy over the entire film is attributed to the very large lattice mismatch in this system. No amorphous interface layer between the Ge substrate and crystalline high-k film was observed through TEM and XPS analyses, indicating that native germanium oxide and suboxides may be unstable under typical ALD growth conditions or they may be removed by HF-vapor treatment producing a chemical termination that is stable during subsequent ALD processing. Although large hysteresis and frequency dispersion were observed, very low leakage current densities are promising for the future potential of epitaxial metal-oxide/Ge gate stacks.

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